INTERNATIONAL WORKSHOP ON
IP BASED SYNTHESIS AND SYSTEM DESIGN

Design of an ARM Based System-on-a-Chip for Pay Phones

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Telefónica
Investigación y Desarrollo

Telefónica I+D Pay Phone System

TID Designed the Spanish Pay Phone System in 1990

The System is deployed mainly in Spain, South America and Australia.

In 1997 TID revised the design: The TMPLUS system

TID is now preparing the next version based on a SOC device: the uPP microcontroller.

TM terminals all over the World: 325.133 (June 1998)

Spain: 101.272

Croatia: 13.998

Malasia 20.805

Mexico: 12.673

Venezuela: 45.271

Perú: 31.234

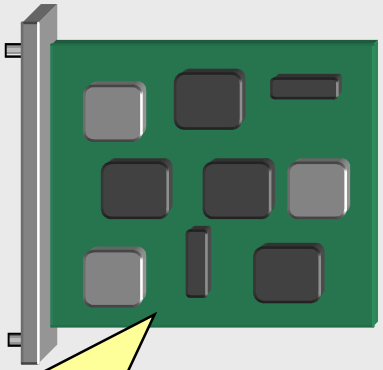
Chile: 16.250

Argentina: 46.118

Australia: 23.300

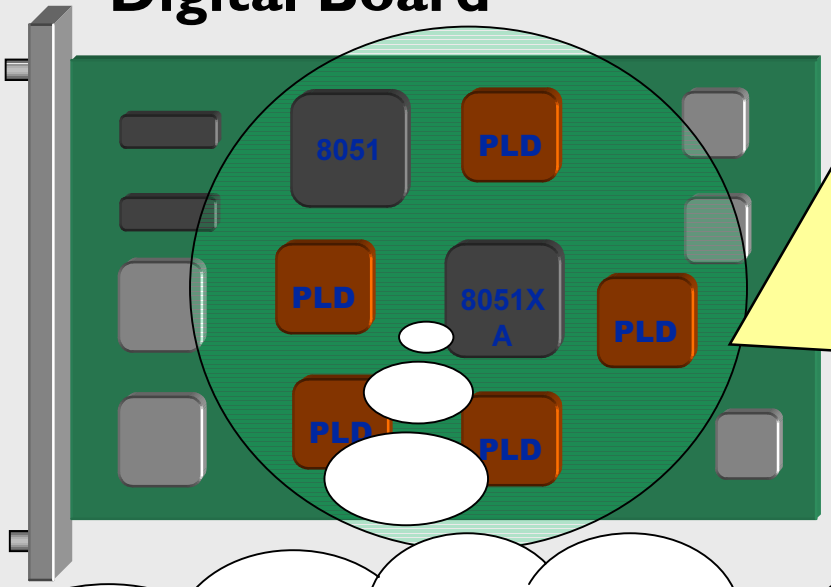
TM PLUS PAY PHONE SYSTEM

Analog Board



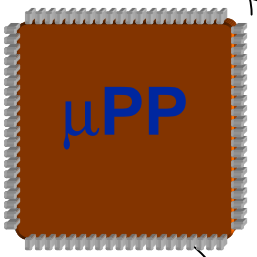
- Phone line interface
- Power supply:
  - Relays
  - Mechanical devices

Digital Board



- Two micros:
  - 8051 (supervisor)
  - 8051XA (main micro)
- Peripherals:
  - Keyboard
  - LCD
  - Real time Clock
  - Pay Systems
  - Comms.

System on a Chip Solution



ESPRIT Project 20724
TOMI

µPP CIRCUIT DESIGN CONSTRAINS

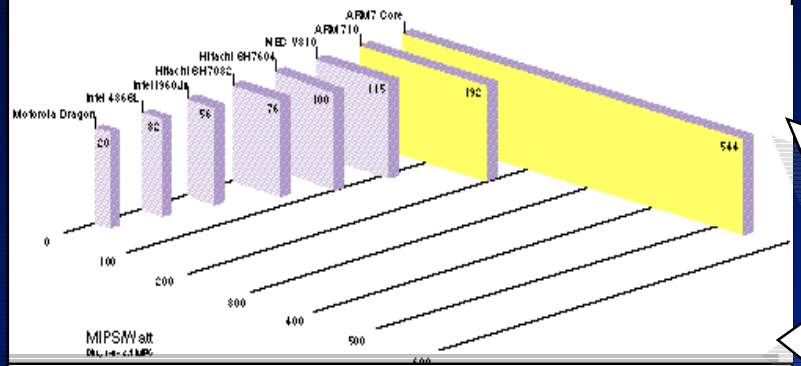
Modularity: Peripheral controllers included.

Low Power: battery supplied.

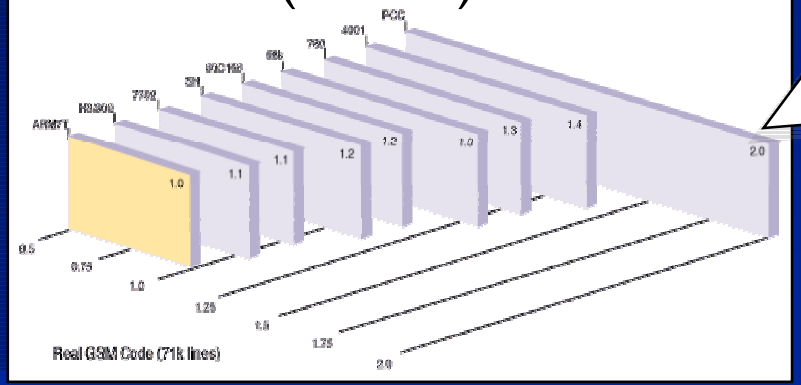
"Sleep" modes.

Reduced design time: based on IP reuse.

Best MIPS/Watt ratio

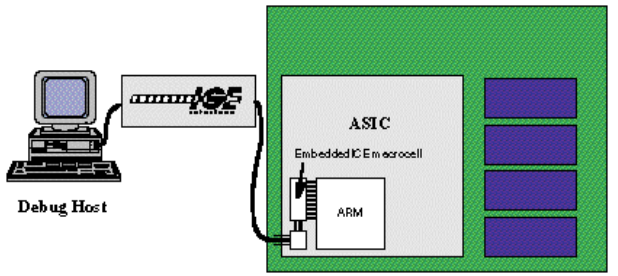


Smallest (Thumb) Code Size

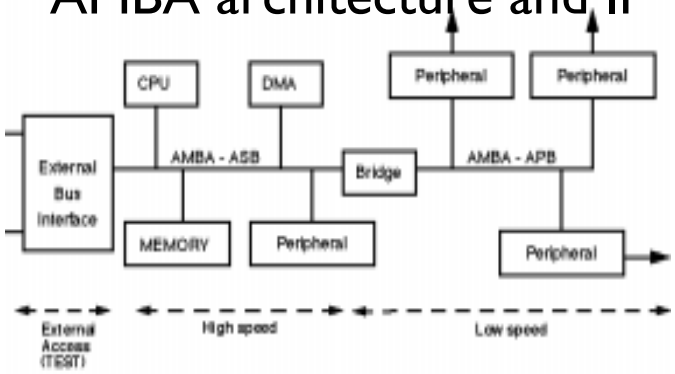


ARM7TDMI

Debugging using Embedded-ICE



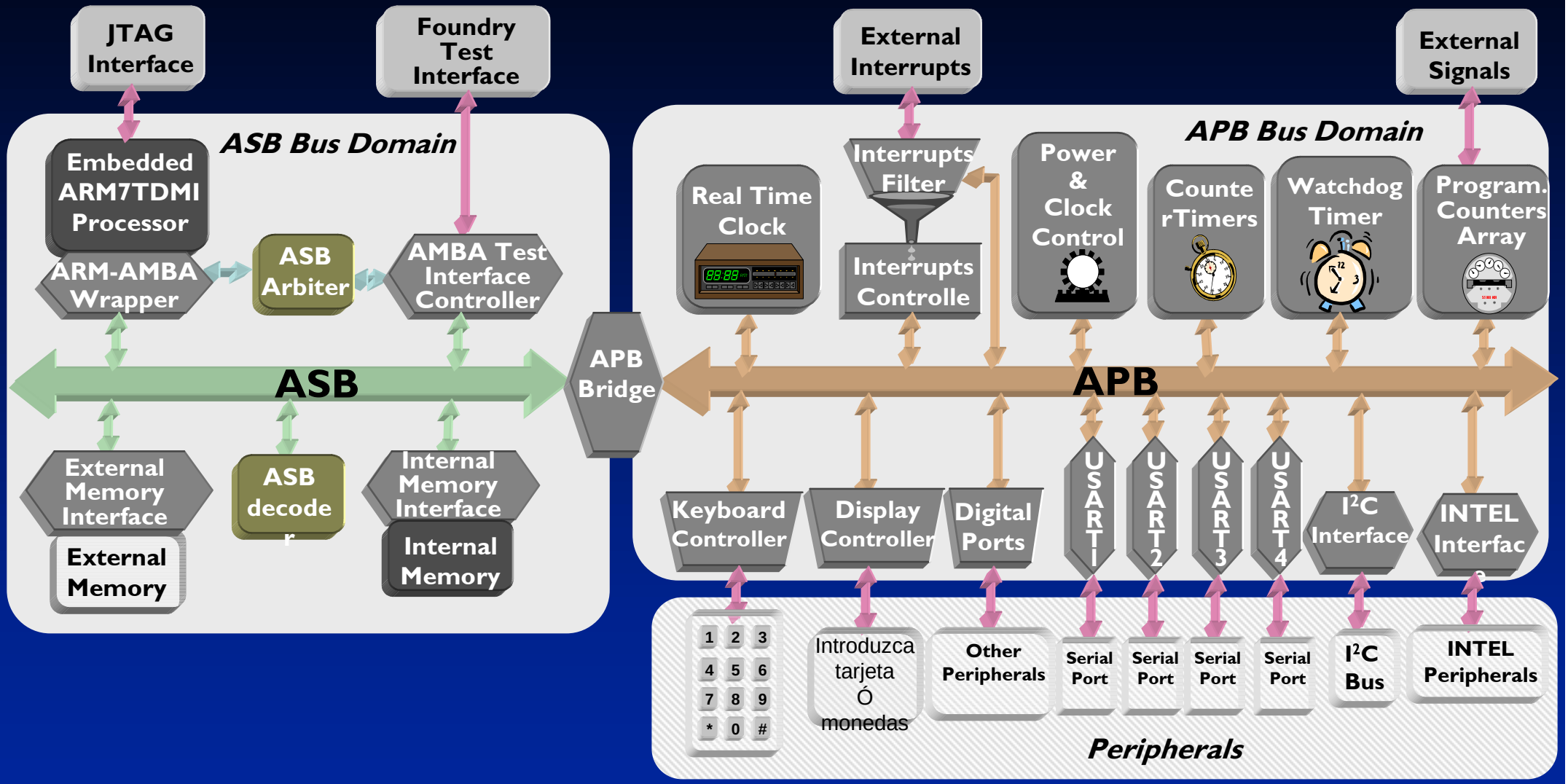
AMBA architecture and IP



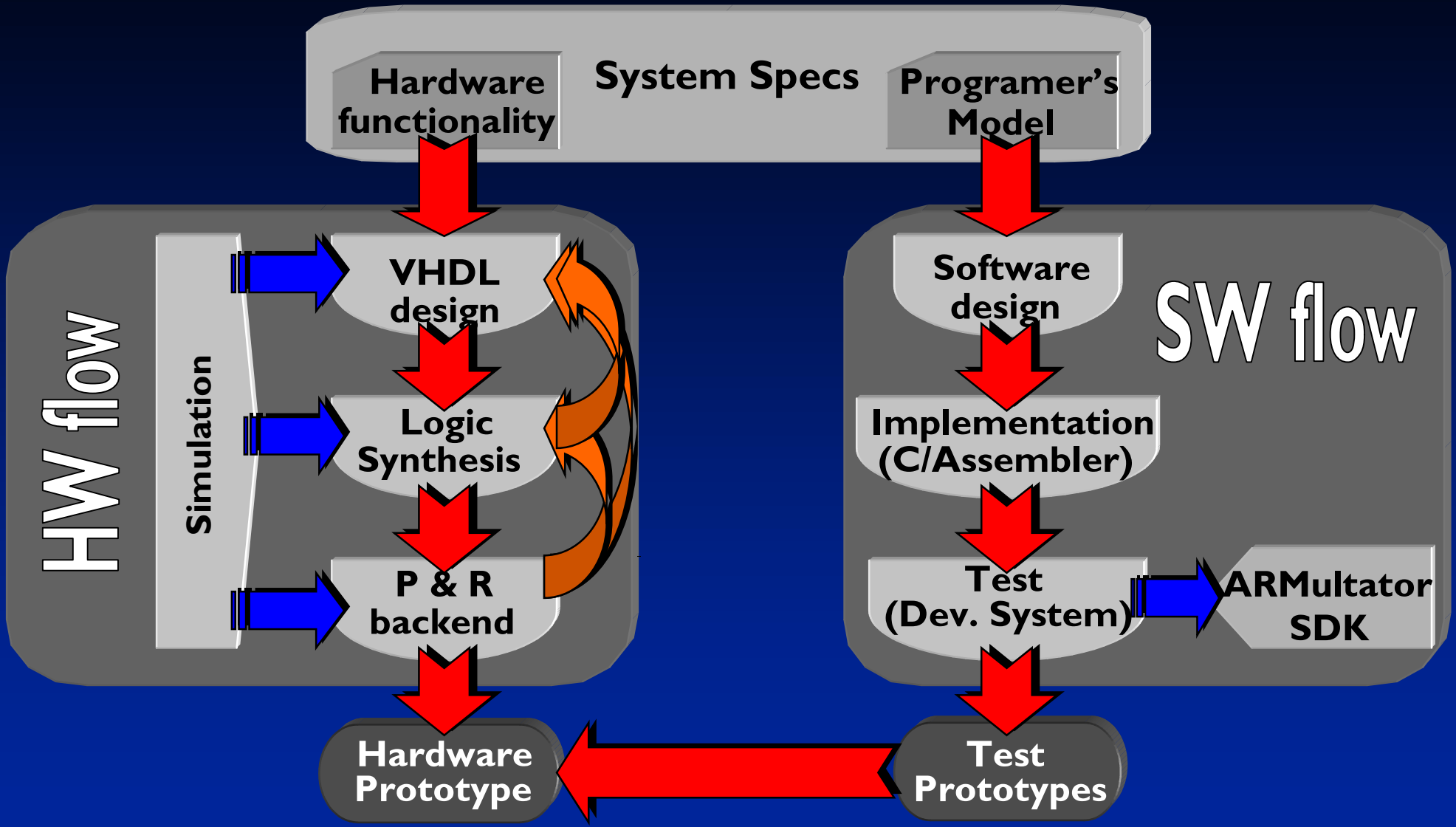
CIRCUIT ARCHITECTURE (I)

- BASED (*Advanced Microcontrollers Bus Architecture*) CONCEPT FROM ARM
- ADVANTAGES OF USING AMBA:
  - STANDARD ARCHITECTURE CONCEPT FOR EMBEDDED MICROCONTROLLERS.
  - EASY DIVISION BETWEEN HIGH AND LOW PERFORMANCE MODULES (APB AND ASB).
  - ARM *MICROPACK* PROVIDES:
    - Modules required to perform ASB functionality
    - Modules required to perform APB functionaly
    - Examples of APB and ASB peripherals
    - A proven architecture for designing new APB and ASB modules
  - EASY TECHNOLOGY RE-TARGETTING (HDL RTL SYNTHESISABLE CODE PROVIDED).

CIRCUIT ARCHITECTURE (II)



DESIGN METHODOLOGY



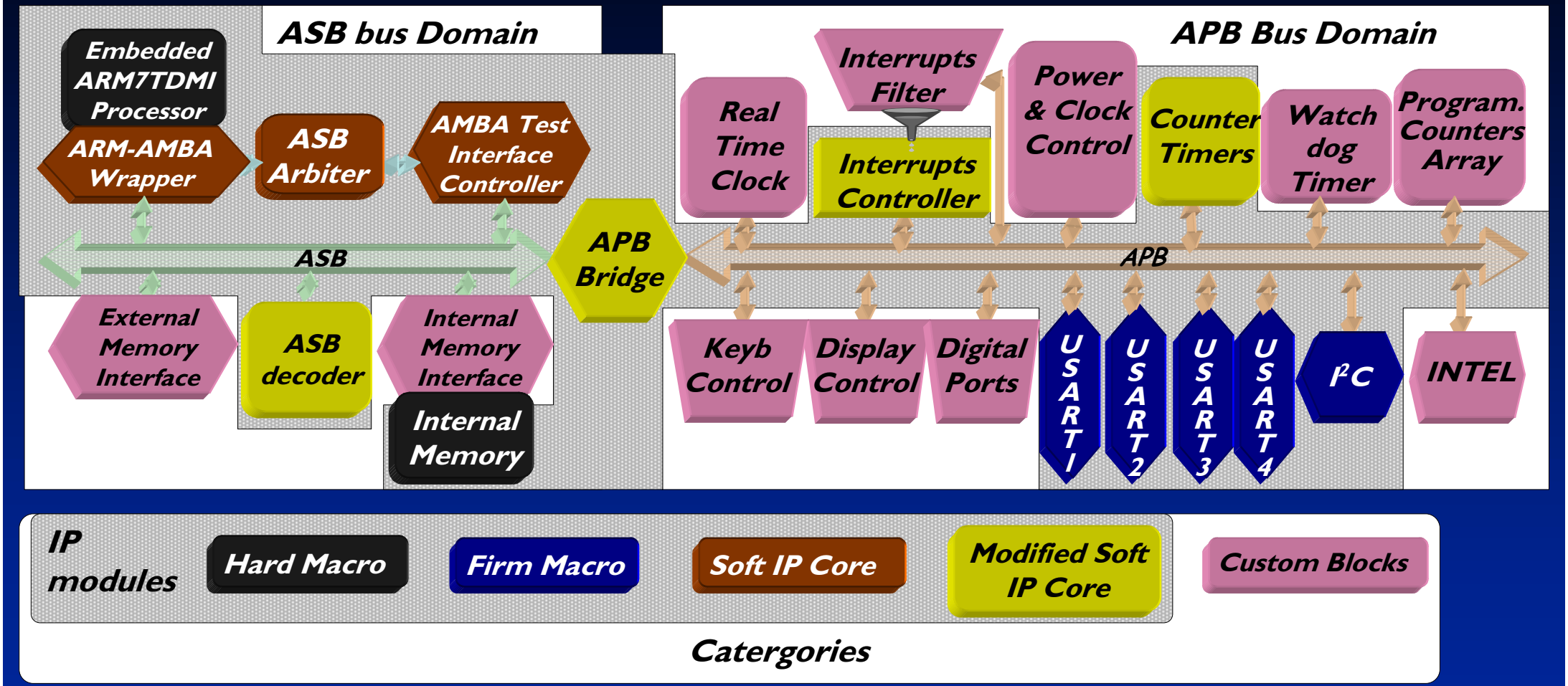
HARDWARE DESIGN FLOW

- HARD CORES (ARM7TDMI, MEMORIES):
  - MODEL (Simulation)
  - ABSTRACT (Floorplanning).
- FIRM BLOCKS (USART'S AND I^2C):
  - GATE NETLIST
  - STANDARD CELL P&R
- SOFT BLOCKS:
  - RTL HDL (Customization)
  - SYNTHESIS (Eased by *Micropack* Scripts)
  - STANDARD CELL P&R
- CUSTOM BLOCKS:
  - RTL Coding → SYNTHESIS (*Micropack* Scripts) → Standard Cell P&R
- HARDWARE/SOFTWARE COSIMULATION USING ARM MODEL

SOFTWARE DESIGN FLOW

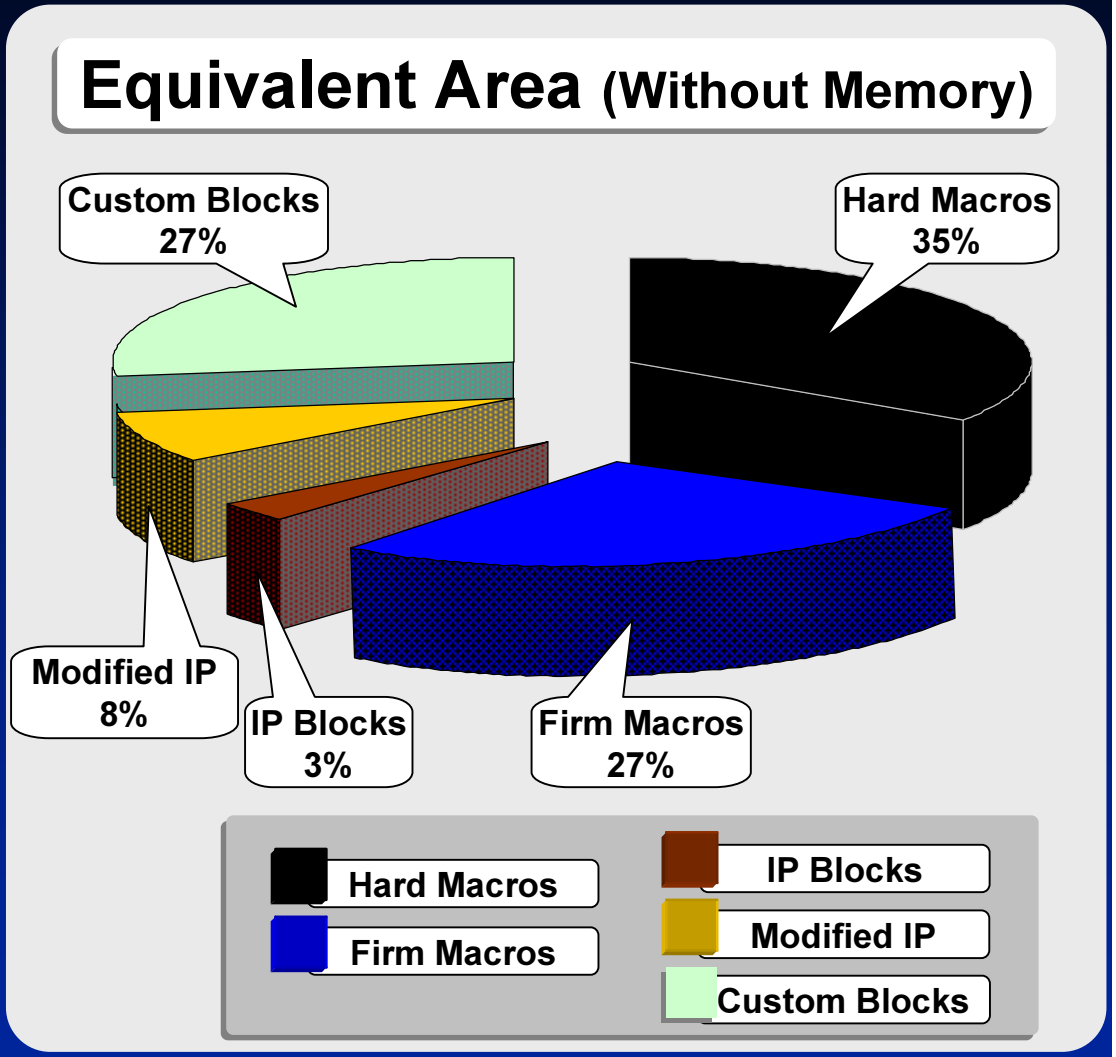
- RUN IN PARALLEL WITH THE HARDWARE DESIGN
- SOFTWARE DEVELOPMENT SYSTEM:
  - ARM Software Development Kit (including ARMulator)
  - ARM Development Board with Embedded-ICE
- SOFTWARE DESIGN:
  - Starting from existing Software (ANSI C) for 8051 Microcontroller
  - Using an "Open" Programmer's Model (Relative Addresses)
  - Coding device drivers in Assembler and C
- SOFTWARE DEBUGGING SYSTEM
  - ARM Software Development Kit
  - Final Application Board with Embedded-ICE Interface
- HARDWARE SOFTWARE COSIMULATION
  - Interrupts Service Routine simulated with HDL hardware model.

HARDWARE DESIGN REUSE (I)



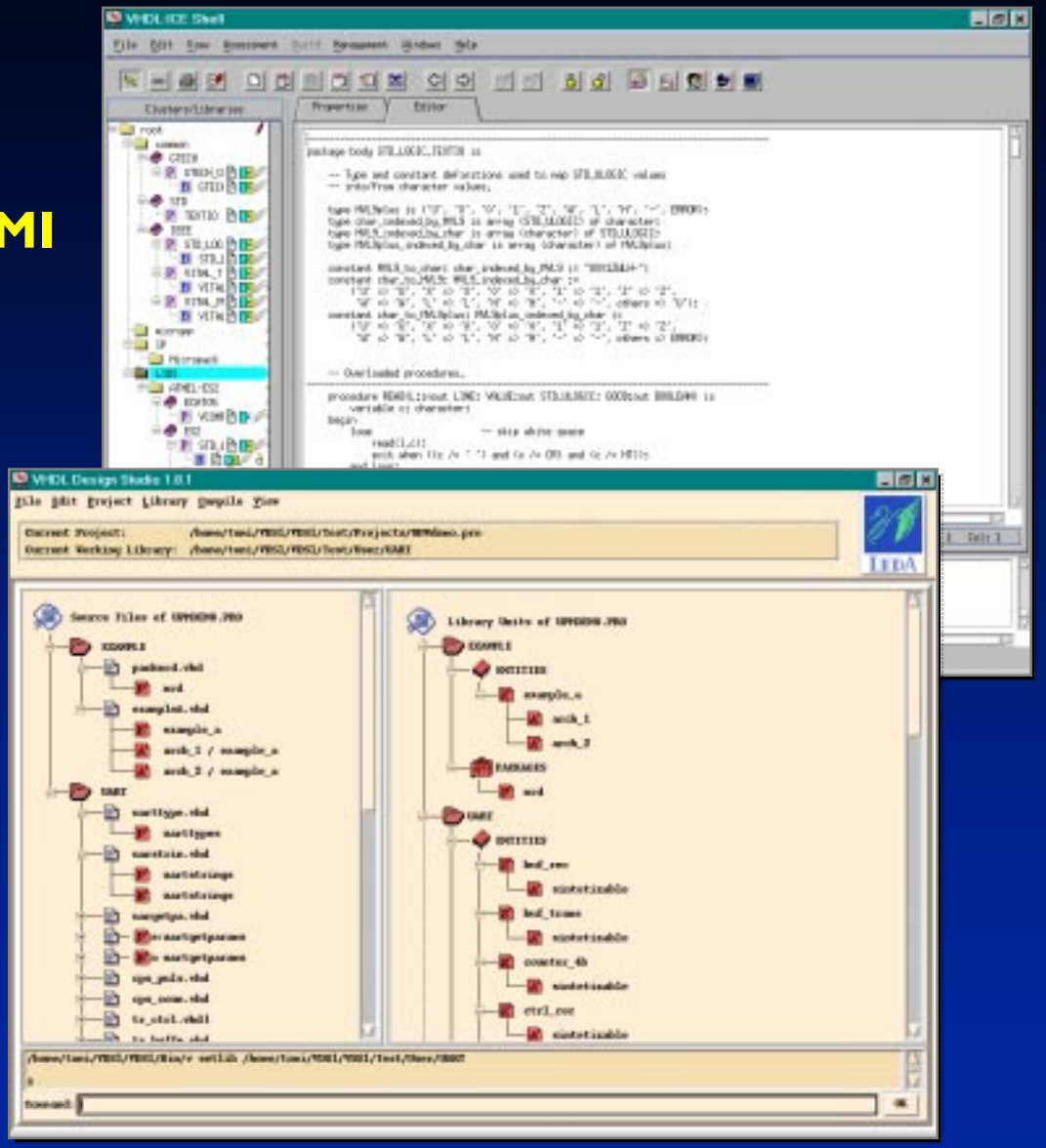
HARDWARE DESIGN REUSE (II)

- 65 % of the circuit area is occupied by IP cells without modification.
- Custom designed modules take only 27 % of the circuit area.
- Only 38% of the circuit area had to be synthesised.
- Standard Cell P&R has been performed over 65 % of the Area (memory excluded).



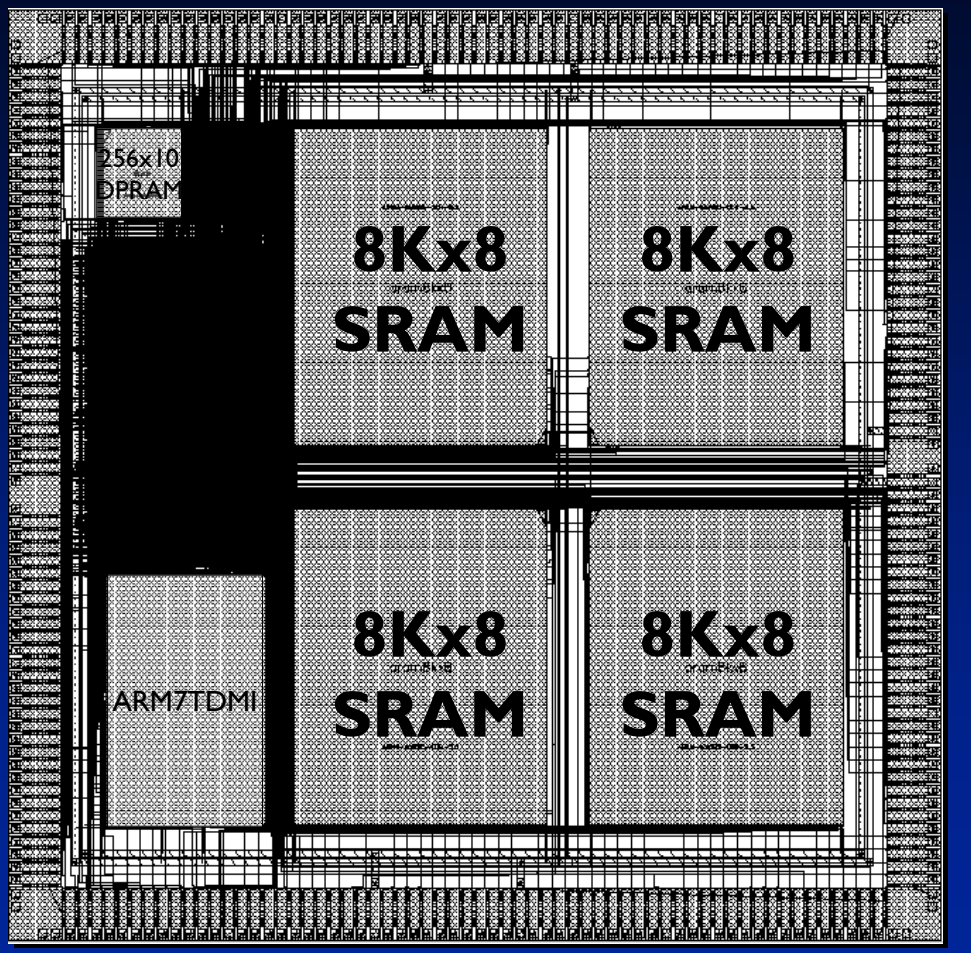
HDL DESIGN MANAGEMENT

- µPP is the result of ESPRIT 20724(TOMI: Tools for OMI).
  - "Providing missing methods and tools that makes practical the OMI concept of Supercells based system design"
- VHDL design management tools:
  - Management and Reuse for Supercell-based design.
- VHDL-ICE:
  - Client/Server
  - Multiplatform, distributed database.
  - Hierarchy, Units an Simulation navigators
- VHDL Design Studio:
  - TCL-TK based GUI.
  - VHDL87-93-Verilog
  - Script mode



µPP CIRCUIT FIGURES & FEATURES

- 68K equivalent gates (excluding memory).
- 256Kbits (4*8Kx8) of single port static RAM
- 2Kbits (256x10) of dual port RAM
- Embedded ARMTDMI
- 72.25 mm^2, ATMEL ECAT05 (0.5 µm Technology).
- CQFP 304 pins package:
  - 234 functional pins
  - 28 supply pins
- 1-16 MHz/32 KHz selectable clock
- 0.6 mW. (sleep mode) to 300 mW.



CONCLUSIONS

- Example of SOC solution for an existing System
  - Reducing final cost.
  - Increasing Reliability
  - Improving significantly system performance.
- Design Based on IP reuse
  - Reduction in design time
  - Confidence in the “First Time” success (IP modules proven in Silicon)
- Parallel development of Hardware and Software
  - Design interaction: Software needs are supported by Hardware
  - System “Ready to go” with the reception of circuit prototypes
- HDL Design Management tools:
  - Useful in IP based Designs