

# Reusing VHDL Soft-Cores by Means of Using Appropriate Workspace, Management and Navigation Tools

SIDA & TI+D

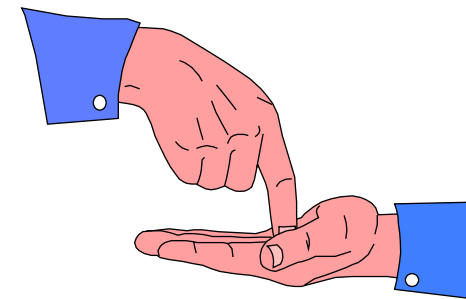
There is a clear need for:

- Standards, confidentiality and licensing terms and conditions, legal protection, vendor qualification and certification, customer support and a marketing channel.



and presented as a pure IP-Broker activity.

However, even solving all of these  
**NEGOTIATION-BLOCKING** issues,  
the business model can not be solved

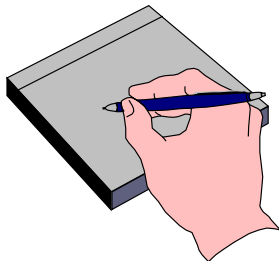


Reusing Soft-Cores implies a lot of engineering and Reengineering support.



Today, it's and Engineer-to-Engineer NEGOTIATION that requires technical experts on both sides of the negotiation, not just salespeople quoting prices and delivery.

This process demands a METHODOLOGY to be supported by



a new wave of specific TOOLS and the involved consulting services.

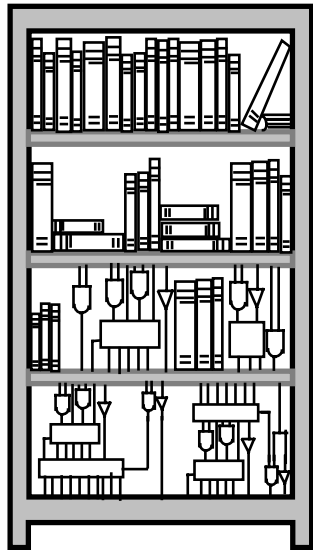


## Design Reuse IMPLIES Multiple Access:

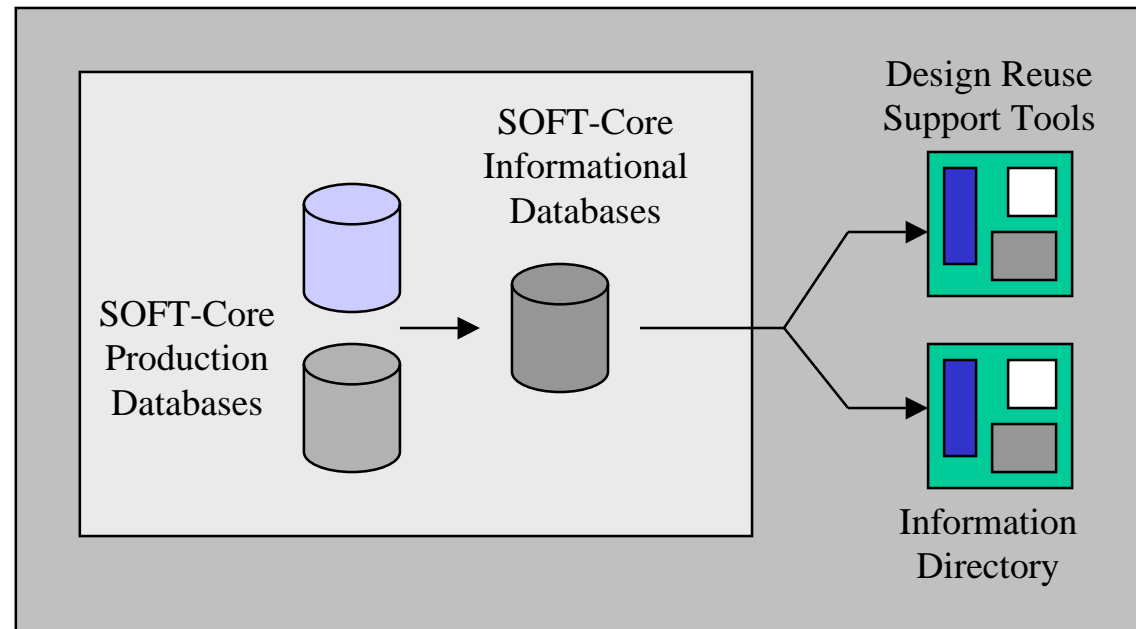
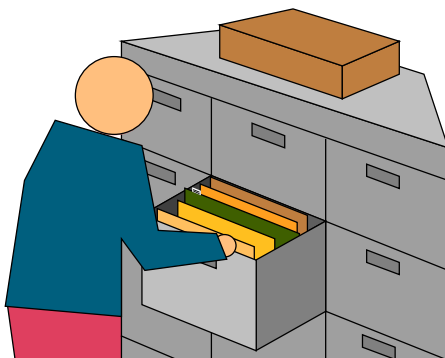
- ONE user SHARING SOFT-Cores in a long period of time during a project or in several projects. The BASIC RE-user action.
- SEVERAL users SHARING among them SOFT-Cores at the same time (producer/consumer interaction) or at different times (RE-user action).

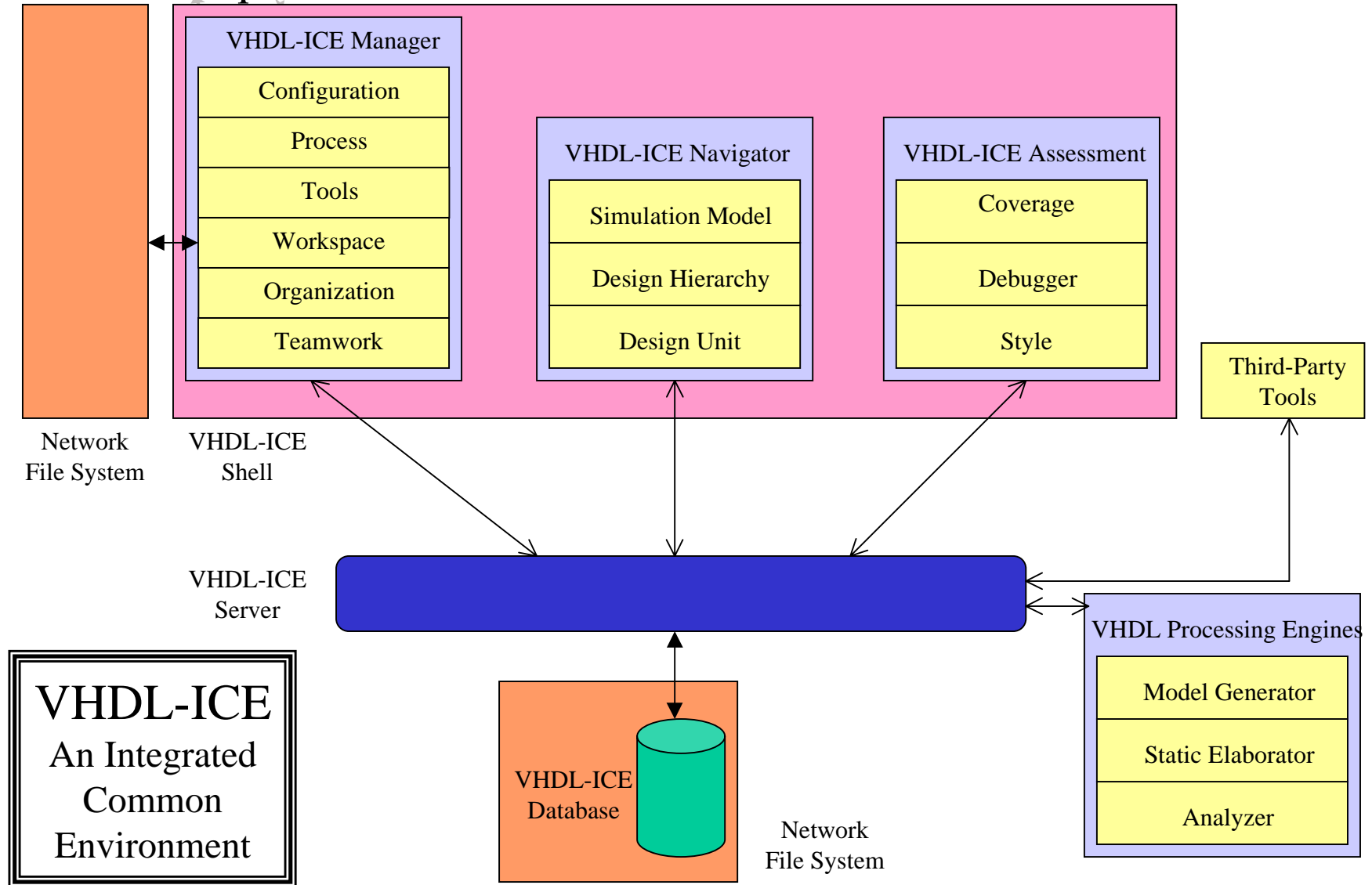


There is a NEED of an Environment for *Managing* and *Reusing* SOFT-Cores supporting MULTIPLE and CONTROLLED ACCESS through the NETWORK.

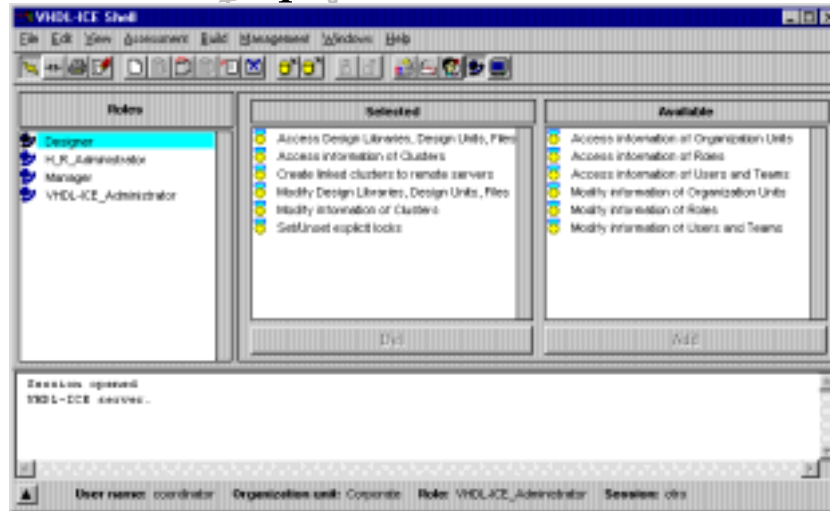


These TOOLS will relay on the MANAGEMENT and EXPLOITATION of the DATABASES where DESIGN LIBRARIES of SOFT-Cores will be stored.

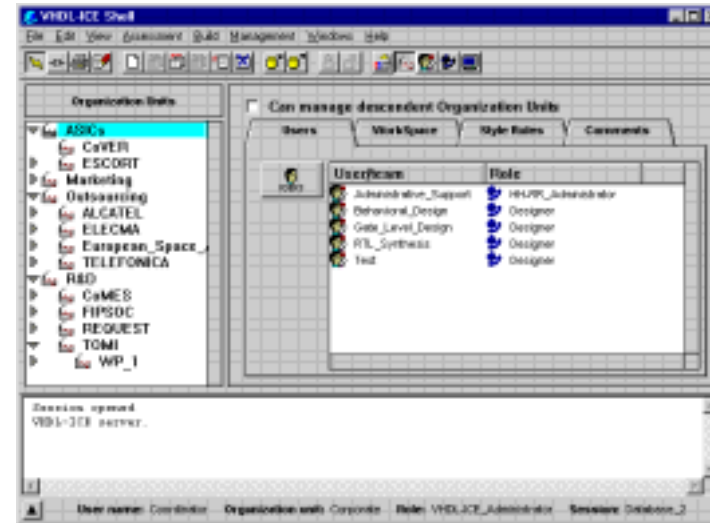




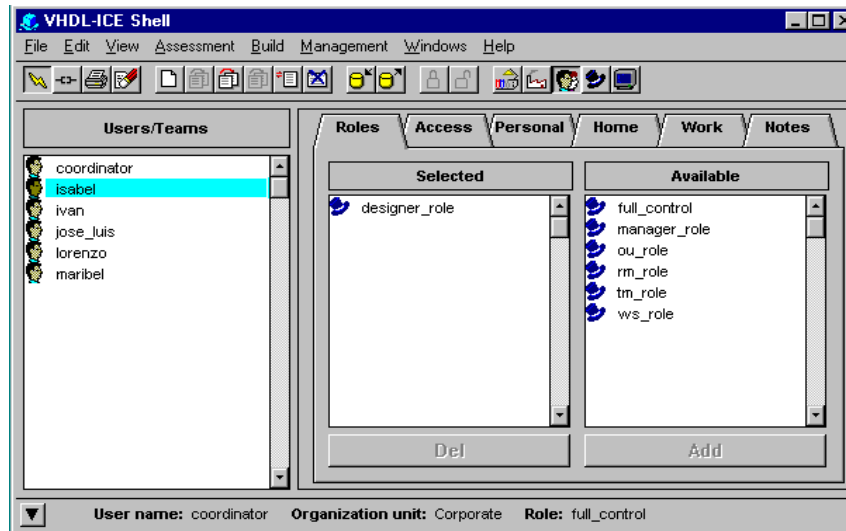
**VHDL-ICE**  
An Integrated  
Common  
Environment



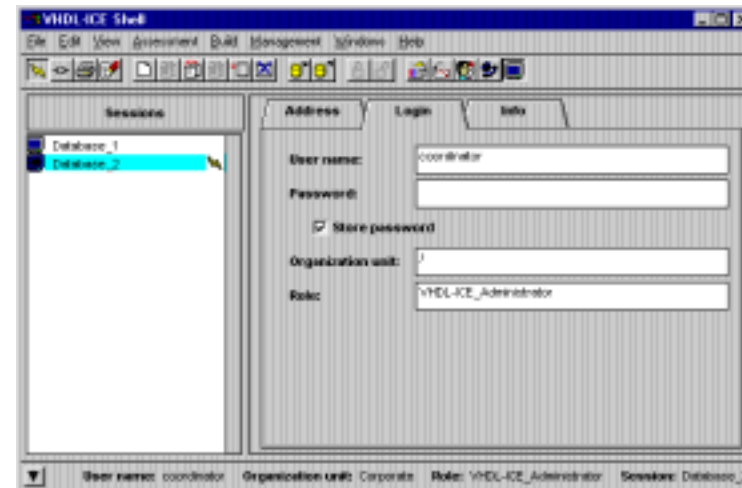
**Role-Based Access Control**



**Organization Units**

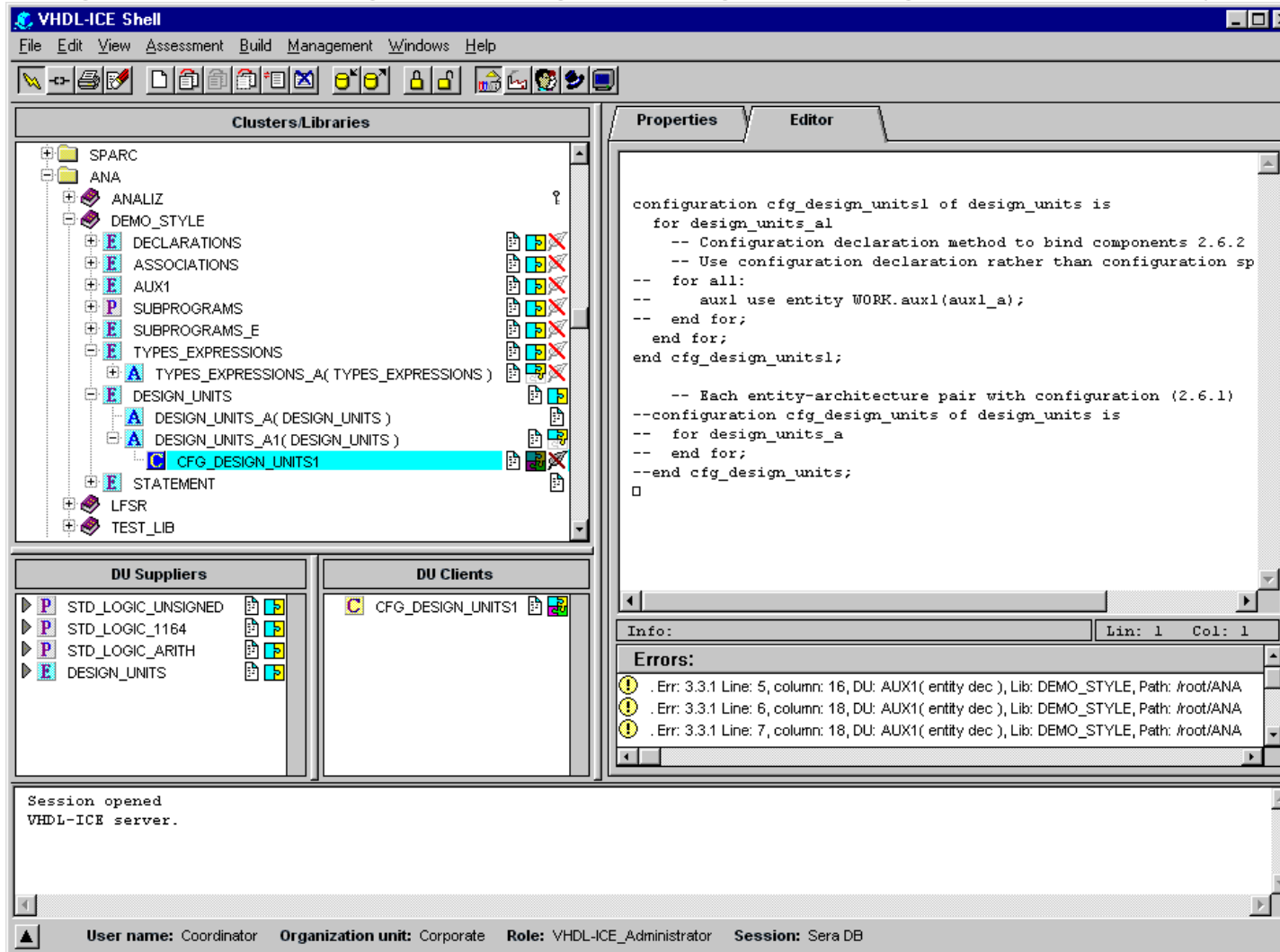


**Users and Teamwork**



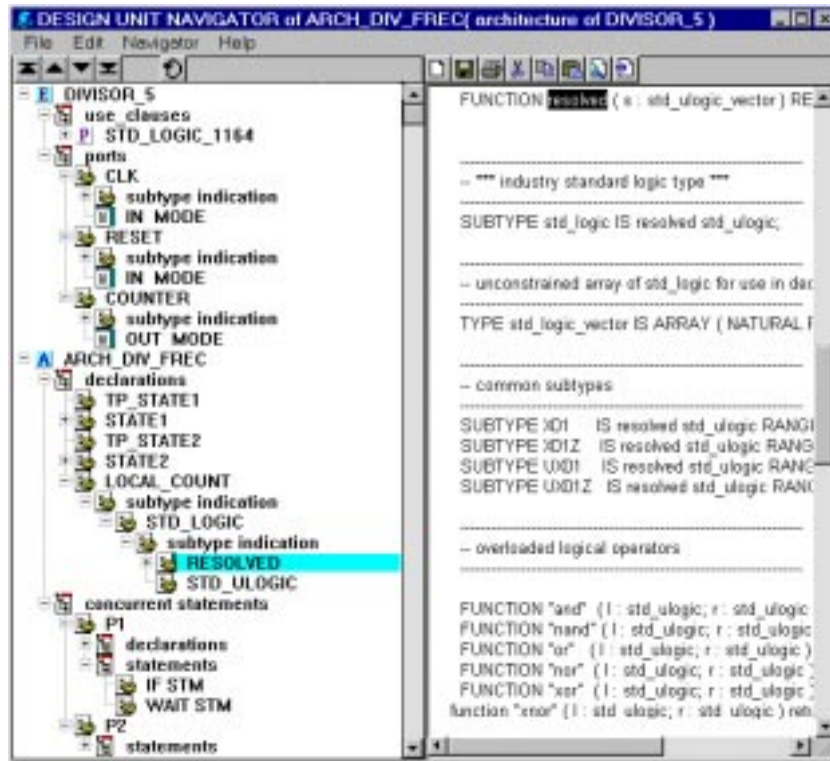
**Sessions**

# Engineering and RE-engineering through Navigation and Style Checking

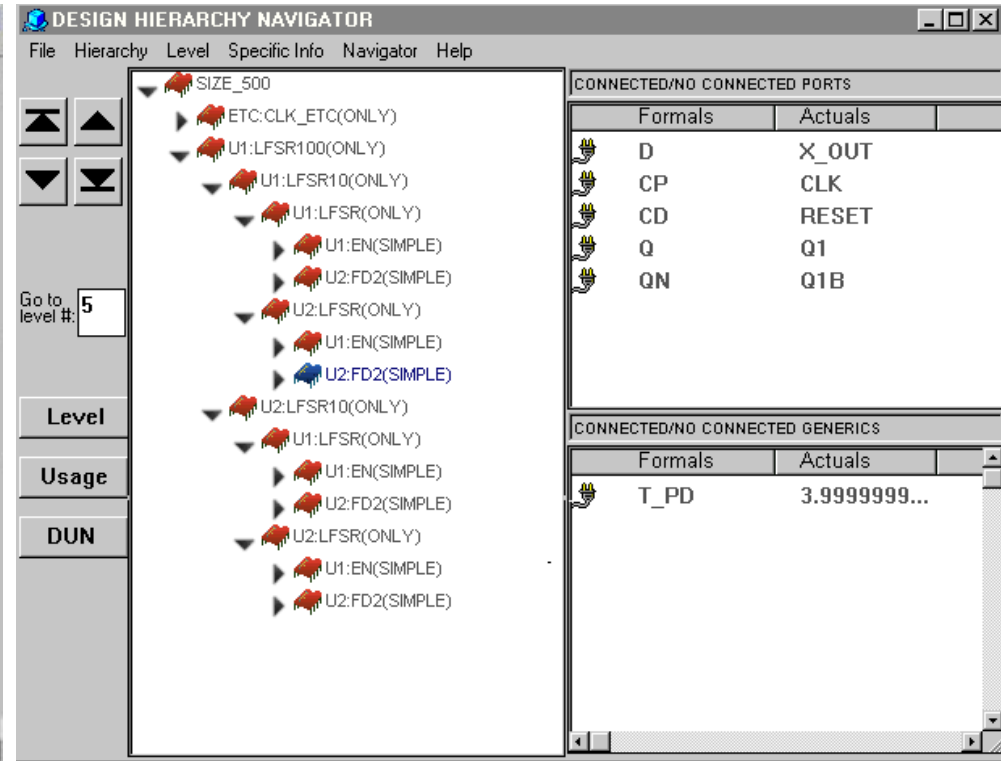


The screenshot displays the VHDL-ICE Shell interface. The main window is divided into several panes:

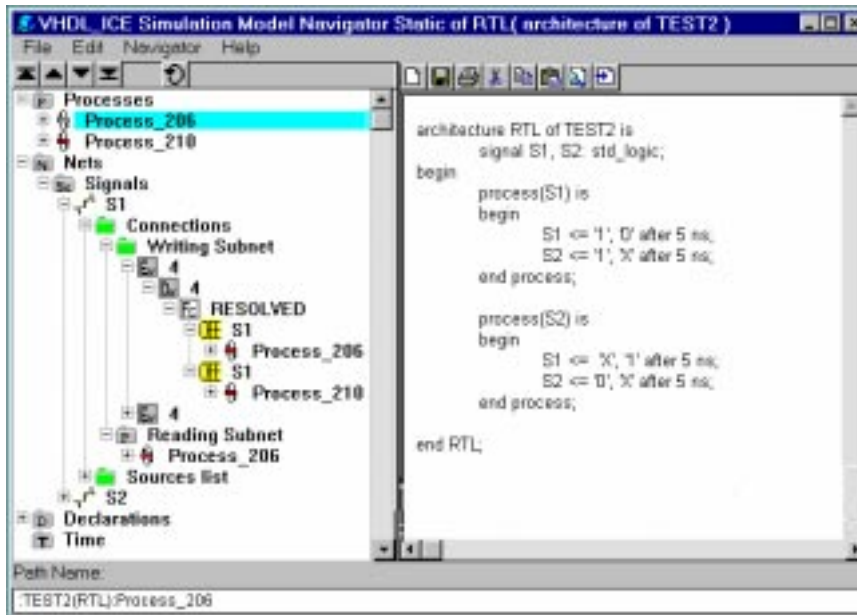
- Clusters/Libraries:** A tree view showing the project structure. The selected path is `SPARC > ANA > DEMO_STYLE > DESIGN_UNITS > DESIGN_UNITS_A1 > CFG_DESIGN_UNITS1`.
- DU Suppliers:** A list of design unit suppliers including `STD_LOGIC_UNSIGNED`, `STD_LOGIC_1164`, `STD_LOGIC_ARITH`, and `DESIGN_UNITS`.
- DU Clients:** A list of design unit clients, currently showing `CFG_DESIGN_UNITS1`.
- Editor:** A text editor displaying VHDL code for configuration `cfg_design_units1`. The code includes declarations for `design_units_al` and `design_units_a`, and uses the `AUX1` entity.
- Errors:** A list of error messages:
  - . Err: 3.3.1 Line: 5, column: 16, DU: AUX1( entity dec ), Lib: DEMO\_STYLE, Path: /root/ANA
  - . Err: 3.3.1 Line: 6, column: 18, DU: AUX1( entity dec ), Lib: DEMO\_STYLE, Path: /root/ANA
  - . Err: 3.3.1 Line: 7, column: 18, DU: AUX1( entity dec ), Lib: DEMO\_STYLE, Path: /root/ANA
- Session Info:** A status bar at the bottom showing: `User name: Coordinator Organization unit: Corporate Role: VHDL-ICE_Administrator Session: Sera DB`.



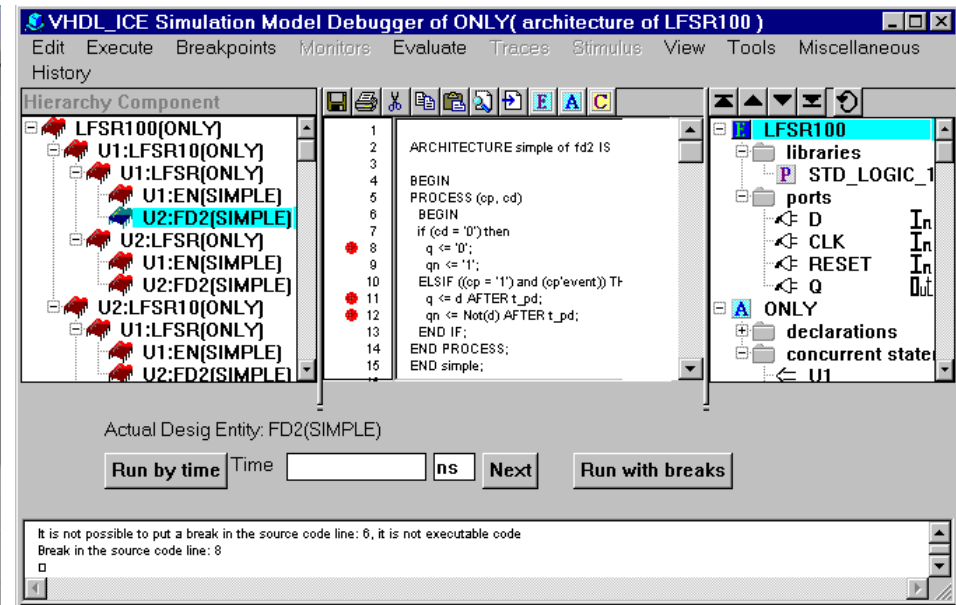
Design Units Navigation



Design Hierarchy Navigation



Simulation Model Navigation

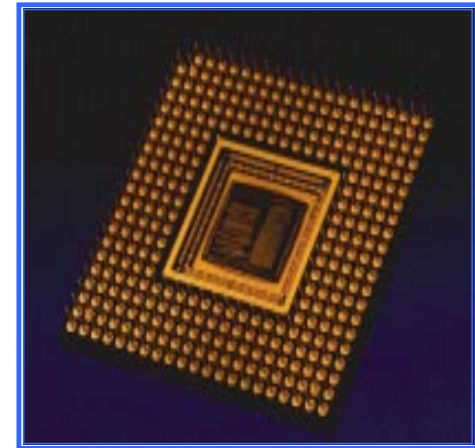


Simulation Debugger

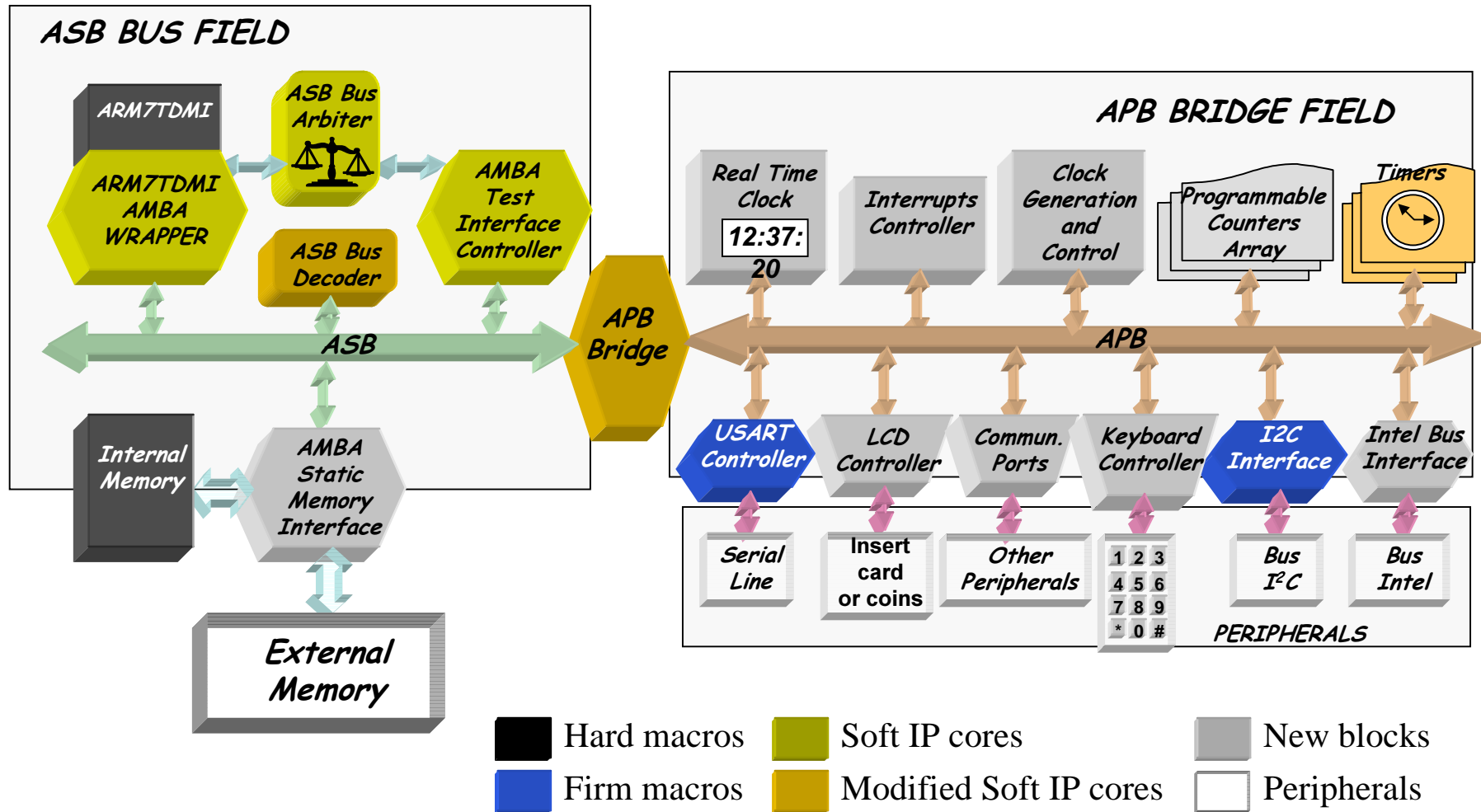
# User Application: Micro-controller for Pay Phones



- Include all system functionality
  - Specific hardware device drivers (LCD, keyboard, etc.)
  - Reduction on PCB size and cost.
- Power Management System
  - Very Low “Static” Power consumption (under 150  $\mu$ A).
  - Processor speed and devices enabling controlled by Sw.
- Based on ARM/AMBA system
  - Usage of IP modules
  - Decoupling Hw/Sw
- Ready for future enhancements:
  - RTOS, Web Services, etc.



# Circuit Architecture



# Re-Usage of Soft IP cores in the design flow



Improves productivity



Need for some minor changes in functionality

- Understand the way they work
- Measure of the quality
- Version management



## VHDL-ICE Benefits



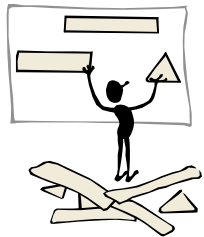
Management of design teams and role based access control



Analysis and debugging of design units



Uniform design style and quality



Design management and export/import of design structure

## Conclusions and Future Work

- The RBAC system of the VHDL-ICE environment to share VHDL Soft-Cores libraries located in a distributed network of databases provides a powerful design reuse framework.
- The VHDL-ICE Workspace and the Navigation Tools have been presented as appropriate tools for design reuse.
- The users' experience has also shown the need for applying some kind of reverse engineering tasks when reusing Soft-Cores.
- Complete VHDL-ICE functionality by the end of 1998.