On the Way to the 2.5 Gbit/s ATM Network. ATM Multiplexer Demultiplexer ASIC

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PRESENTATION OUTLINE

- INTRODUCTION
- GENERAL DESCRIPTION
- ARCHITECTURE
- DESIGN METHODOLOGY
- PHYSICAL IMPLEMENTATION
- CONCLUSIONS
- QUESTIONS & ANSWERS

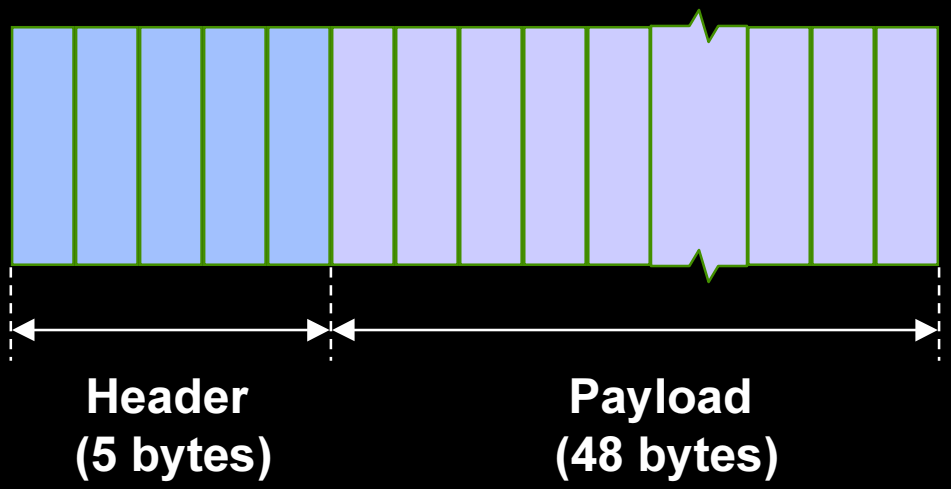
INTRODUCTION. Presentation Purpose

To describe the AMDA integrated circuit (*ATM Multiplexer / Demultiplexer ASIC*)

- **Motivations and challenges**
- **Functionality**
- **Architecture**
- **Design**

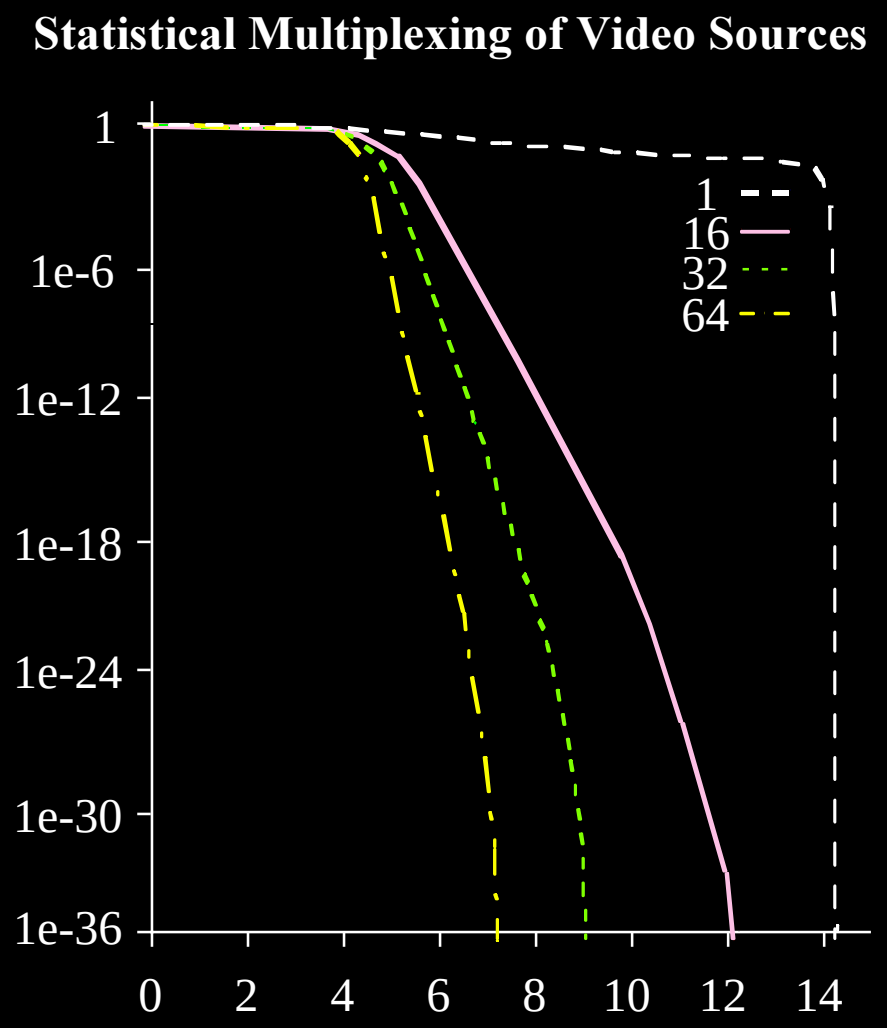
INTRODUCTION. ATM Basics

- **ATM (*Asynchronous Transfer Mode)***
  - ITU selected method for broadband communications (B-ISDN)
- **ATM cell**



INTRODUCTION. ATM Concepts

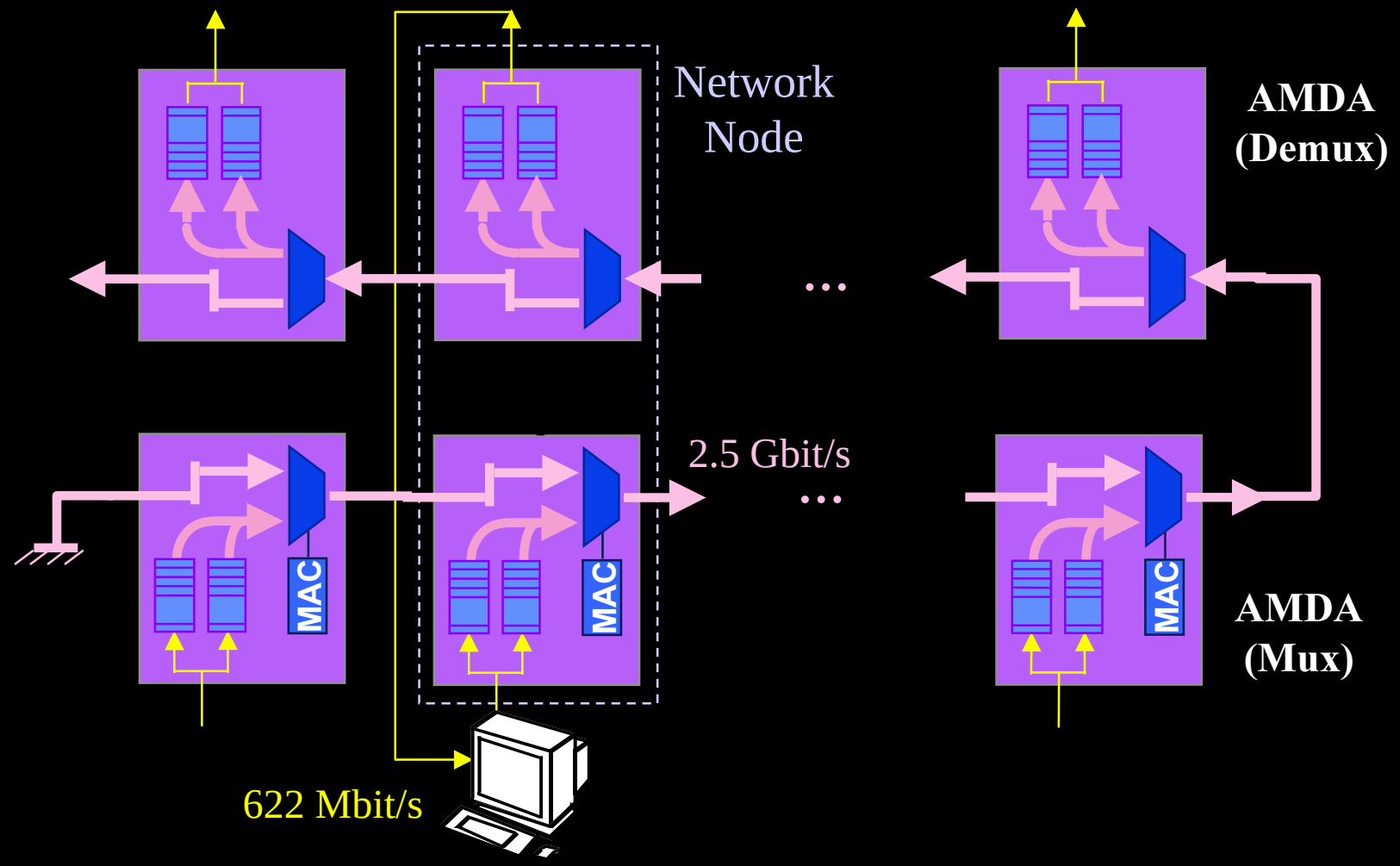
- **Statistical Gain:** ***Several sources can share a link with a lower bandwidth than the sum of the their peak rates***
- **Contention: Several cells from different sources try to access the channel at the same time**
  - **Traffic Queues**
  - **Loss probability**
  - **Delay variations**



INTRODUCTION. The AMDA ASIC

- **MOTIVATION**
  - To exploit the statistical gain characteristics of ATM networks
  - The Need of a block able to add and extract traffic to/from a high speed ATM network
- **PROBLEMS**
  - Distributed algorithm for the Medium Access Control (MAC)
  - Traffic queues dimensions for multiplexing and demultiplexing
  - Speed, Power, Cost
- **OBJECTIVE**
  - ASIC to handle the multiplexing and demultiplexing needs on a 2.5 Gbit/s ATM network
    - First time right
    - Easy test
    - Performing ATM extraction algorithm
    - Optimize system design

AMDA. ATM Network



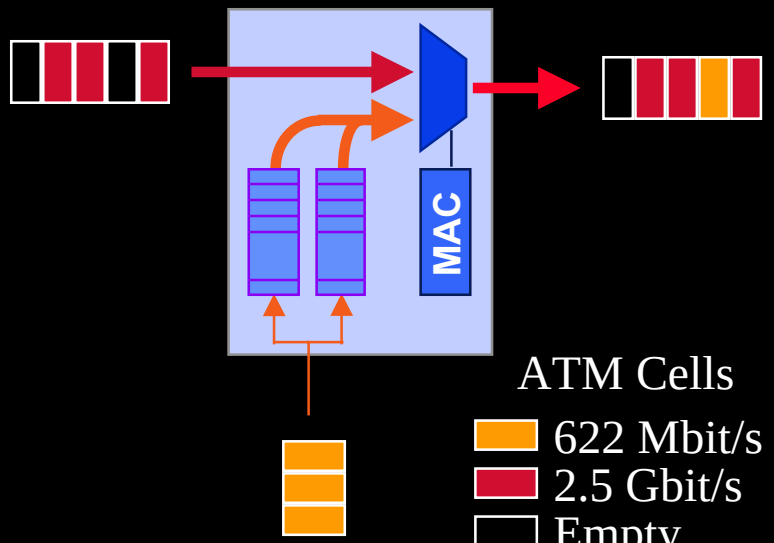
GENERAL DESCRIPTION (1)

- **Two Functional Modes (not simultaneous)**
  - MULTIPLEXER
  - DEMULTIPLEXER

- **MULTIPLEXER Mode**

  Adds ATM traffic (up to 622 Mbit/s) to a high speed ATM flow (2.5 Gbit/s)

  Functions
  - Multiplexing
    - Two queues (high/low priority)
  - Distributed Medium Access Control
    - Scalability
    - Fiability



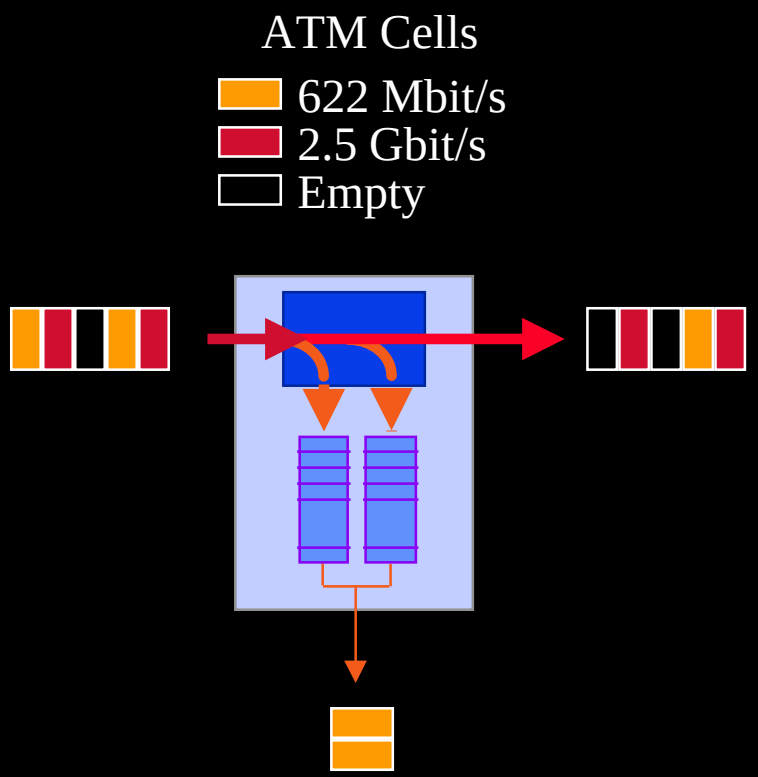
GENERAL DESCRIPTION (2)

DEMULTIPLEXER Mode

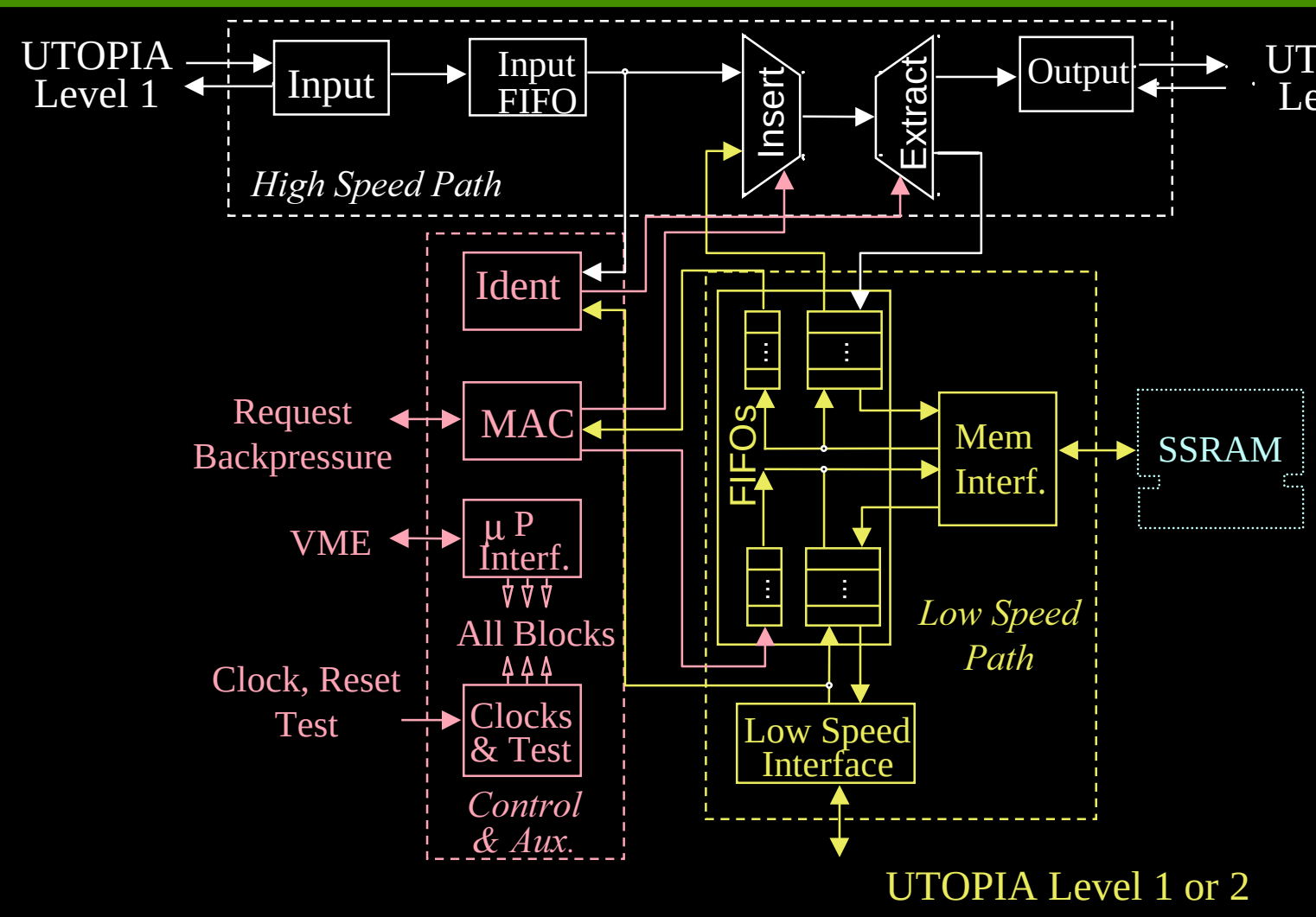
Extracts ATM cells from a high speed link (2.5 Gbit/s) to an ATM receiver (up to 622 Mbit/s)

Functions

- **Filtering**
  - **Verifies cell headers**
  - **Can replace cells in the high speed flow with empty cells**
- **Data rate adaption**
  - **Cell queues (high/low priority)**



ARCHITECTURE. Block Diagram



High Speed Path (1)

- **High Speed Input Interface**
  - UTOPIA Level 1 (16 Bits @ 155 MHz). Rx-ATM Layer
  - Conversion to the internal format (64 bits)
  - Programmable extraction of Medium Access Control signals (*request, backpressure*)
  - Empty cells identification
  - Parity check and wrong cells counter
  - Cell integrity control and manteinance
- **Input FIFO**
  - DPRAM 56x64 (8 ATM Cells)
  - Plesiochronism and physical layer support
- **Insertion Block (Multiplexer)**
  - Replaces the high speed link empty cells with cells from the low speed path, under MAC control
  - Congestion indication (ABR support)

High Speed Path (2)

- **Extraction Block (Demultiplexer)**
  - Writes cells from the high speed link in the low speed path FIFOs
  - Controlled by the cells identification block
  - Allows point-multipoint communications
  - Statistical counters on the high speed path cells
- **High Speed Output Interface**
  - UTOPIA Level 1(16 bits @ 155 MHz) Tx-ATM Layer
  - Conversion from the internal 64 bits format to 16 bits
  - Programmable insertion of Medium Access Control signals
  - Empty cells generation
  - Parity generation and insertion (BIP8)

Low Speed Path

- **Low Speed Path FIFOs**
  - Four DPRAMs (42x64, 28x64, 8x16 and 8x17)
  - Internal buffers for the external memory
  - Two logical queues: Low and high priority cells
- **External Memory (SSRAM) Interface**
  - Addressing capability 256Kx32 (16K ATM cells)
  - Two logical queues with programmable sizes and thresholds
  - Generates the *Backpressure* signal
  - Burst Access (bandwidth 3Gbit/s with a 110MHz clock)
  - Multiplexed address/data bus (pin count reduction)
- **Low Speed Interface**
  - UTOPIA Level 1 or 2 (8 bits @ 33 MHz or 16 bits @ 50 MHz) Tx/Rx-ATM
  - High programmability

Control Blocks

- **Medium Access Control (MAC)**
  - Medium Access Distributed Algorithm (ADAM©)
    - Minimizes queues sizes, *CDV* and network position dependence
  - Controls the insertion block
  - Generates and propagates medium access request signals
- **Cells Identification Block**
  - Identifies ATM connections with 13 programmable header (VPI/VCI) bits (up to 8K channels)
  - Programable parameters for each connection in a 2Kx24 memory (6 bits/canal)
    - Extract and Propagate control bits
    - Cell Priority and Loss Priority bits
    - Selective Discard enable and status bits
  - Statistical Counters

Qualities of Service

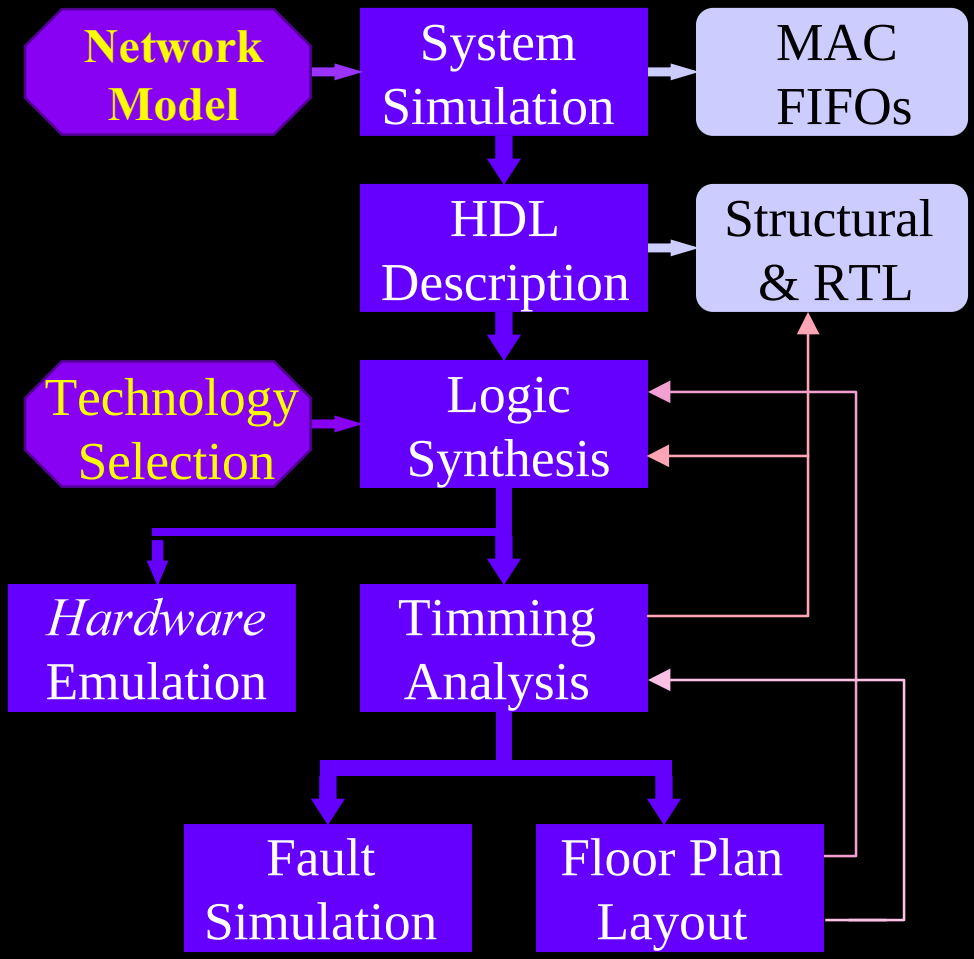
- **Cell Priority and Loss Priority bits allow four different types of services**

		Cell Delay Sensitivity	
		High	Low
Cell Loss Sensitivity	High	Encoded Video	Data
	Low	Voice	Web

Auxiliary Blocks

- **Microprocesor Interface**
  - VME Bus compatible
  - Sstatistical counters register control
  - Eight interrupts
- **Clock Generation Block**
  - Generates internal clocks from the System Clock (155 MHz)
    - 64 bit word clock (40.5 MHz)
    - MAC Clock (77.5 MHz)
  - Synchronizes reset signals (system reset and software reset)
- **Test Control Block**
  - Generates test control signals for structural tests and BIST
  - *Ad hoc* test & fault simulation (95% coverage)

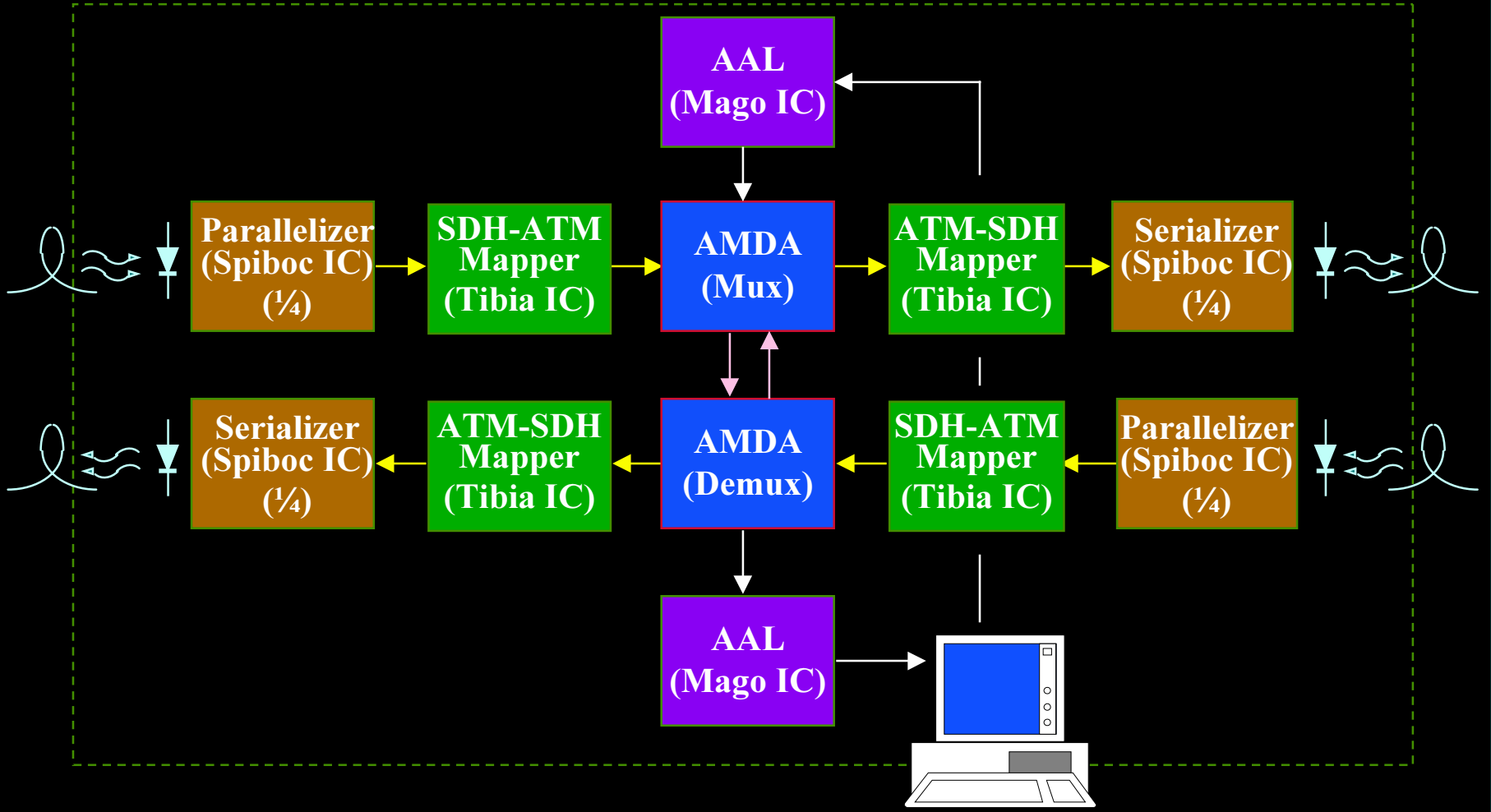
DESIGN FLOW


Network Model
System Simulation
MAC FIFOs
HDL Description
Structural & RTL
Technology Selection
Logic Synthesis
Hardware Emulation
Timming Analysis
Fault Simulation
Floor Plan Layout

PHYSICAL IMPLEMENTATION

- Technology LSI-Logic LCB500K (0.5 μm)
- 34800 Equivalent gates (NAND2)
- 48 Kbit Single port RAM
- 8.5 Kbit Dual port RAM
- Die size 6.7 x 6.7 mm
- Package PQFP 208 pins (3 n.c.)
  - 31 Supply (3.3 V) and 37 Ground (68 supply)
  - 42 Inputs, 35 outputs, 60 bidirectional (137 functional)
    - 21 PECL inputs @ 155MHz clock
    - 19 PECL outputs @ 155 MHz clock
    - 36 LVTTL Bidir @ 110 MHz clock
    - Remainign I/Os with lower speed clocks (Max 50 MHz)

A 2.5 Gbit/s Network Node



CONCLUSIONS

- The AMDA I.C. simplifies the implementation of wide-band networks
- Statistical gain exploitation
- Bandwidth shared evenly
- Scalability
- Easily integrated in a high speed ATM network node