SIMULATION OF AN ATM NETWORK USING VERILOG

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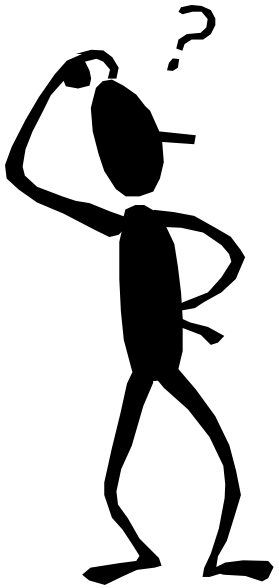
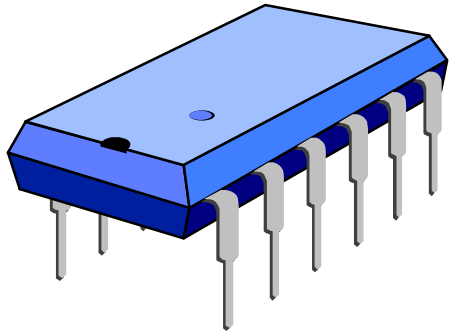
OBJECTIVE

Show how the Verilog HDL can be effectively used in system simulations to aid in the functional definition of an ASIC design





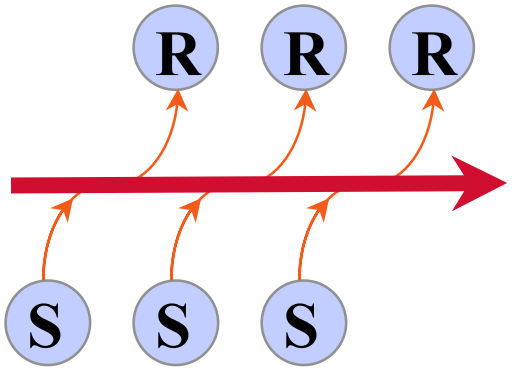
CONTENTS

- INTRODUCTION
- PROBLEM DESCRIPTION
- SIMULATION ENVIRONMENT
- MODELS DESCRIPTIONS
- SIMULATIONS AND RESULTS
- CONCLUSIONS
- QUESTIONS AND ANSWERS

INTRODUCTION (i)

❑MOTIVATION

- ❍ASIC to add/extract traffic on a high speed ATM channel
- ❍USES
  - Hihg speed active *backplanes*
  - Local/Metropolitan area networks (*LAN/MAN*)

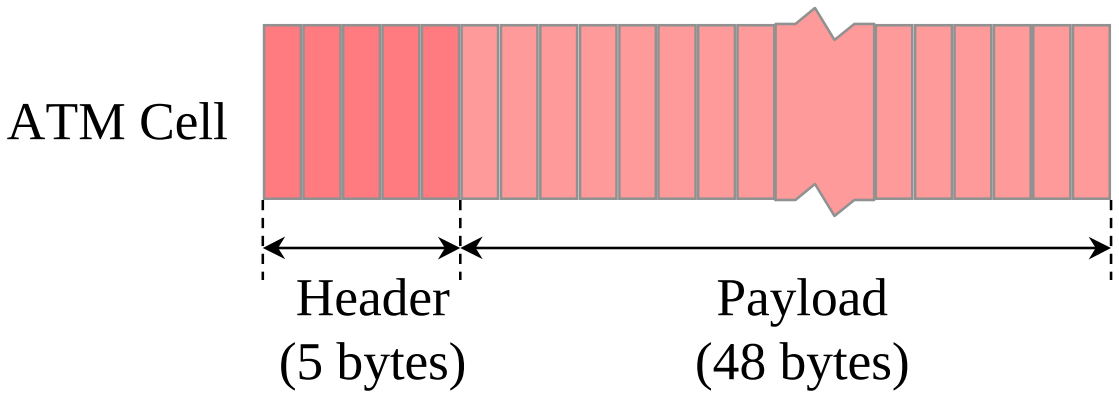


❑PROBLEMS AND AIMS

- ❍Determine de circuit functionality (Medium Access Control algorithm - MAC)
- ❍Traffic queues dimensioning in order to minimize:
  - Cell loss probability
  - Cell delay variation
  - Node position dependency of those parameters

INTRODUCTION (ii)

- ATM (Asynchronous Transfer Mode) Backgrounds
  - UIT Recommended method for broadband systems (B-ISDN)



INTRODUCTION (iii)

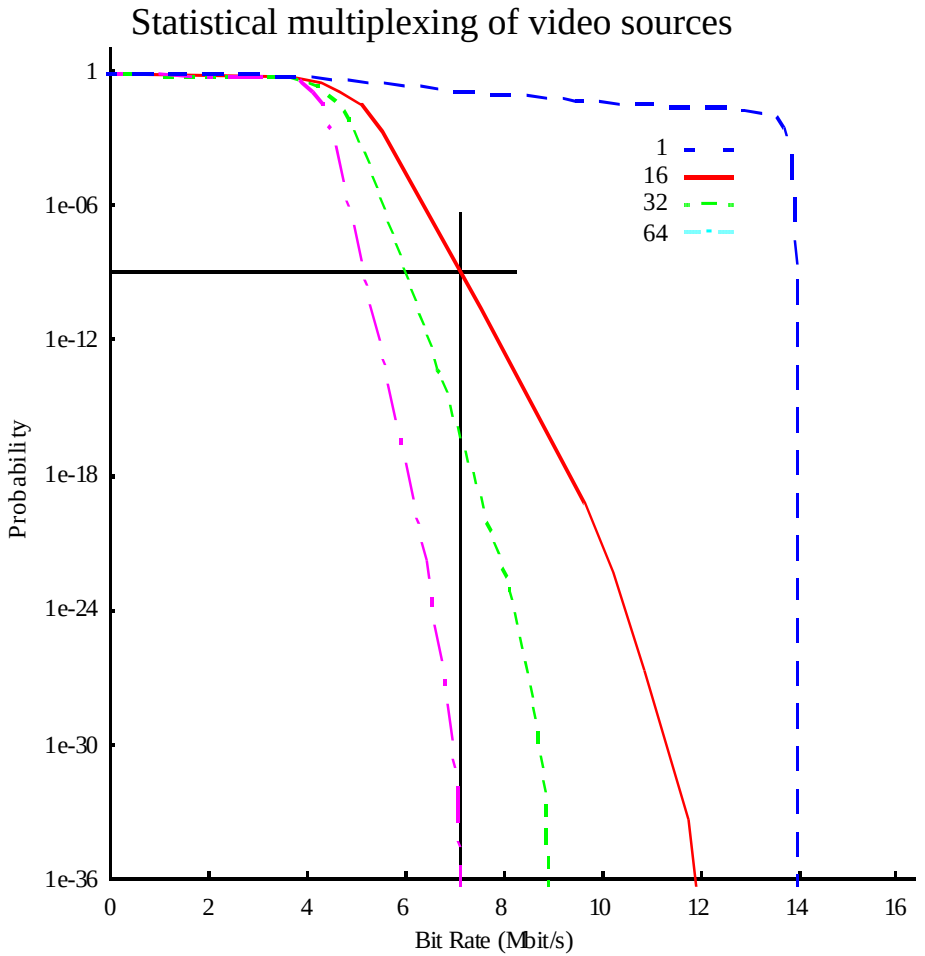
- *Statistical gain*

  Several individual VBR sources can share a link with a total bandwith less than the sum of the sources peak rates.

- *Congestion*:

  Two or more cells comming from different sources try to access simultaneously to the common channel

  - Traffic queues: Loss probability and delay variations.



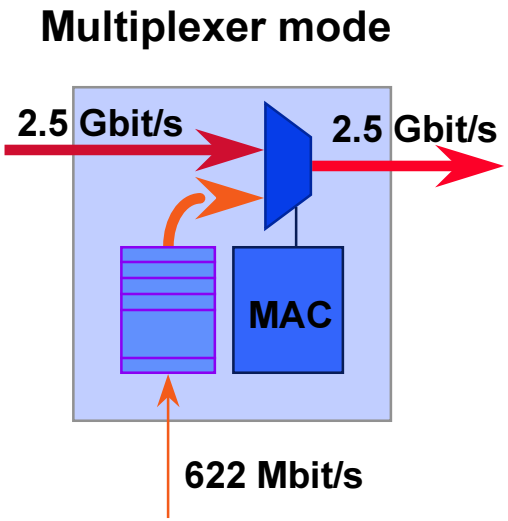
PROBLEM DESCRIPTION (i)

- ASIC with Two operation modes (AMDA)
  - MULTIPLEXER
  - DEMULTIPLEXER

- MULTIPLEXER Mode

  Adds low speed ATM traffic (up to 622 Mbit/s) to a high speed (2.5 Gbit/s) ATM flow.

  Functions:
  - Multiplexing
  - Distributed Medium Access Control (MAC):
    - Scalability
    - Fiability



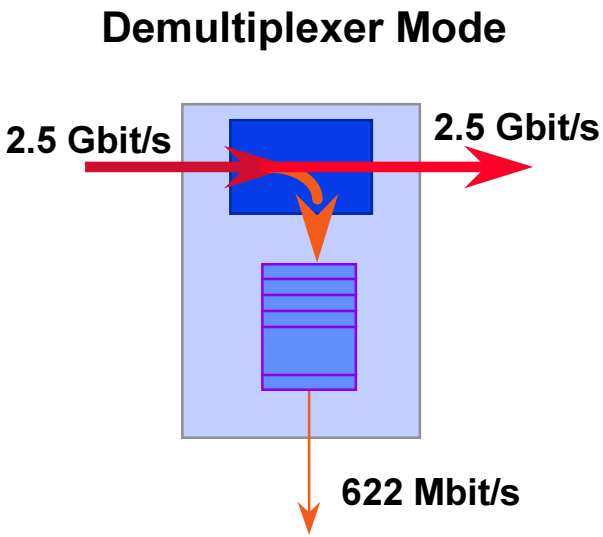
PROBLEM DESCRIPTION (ii)

- DEMULTIPLEXER Mode

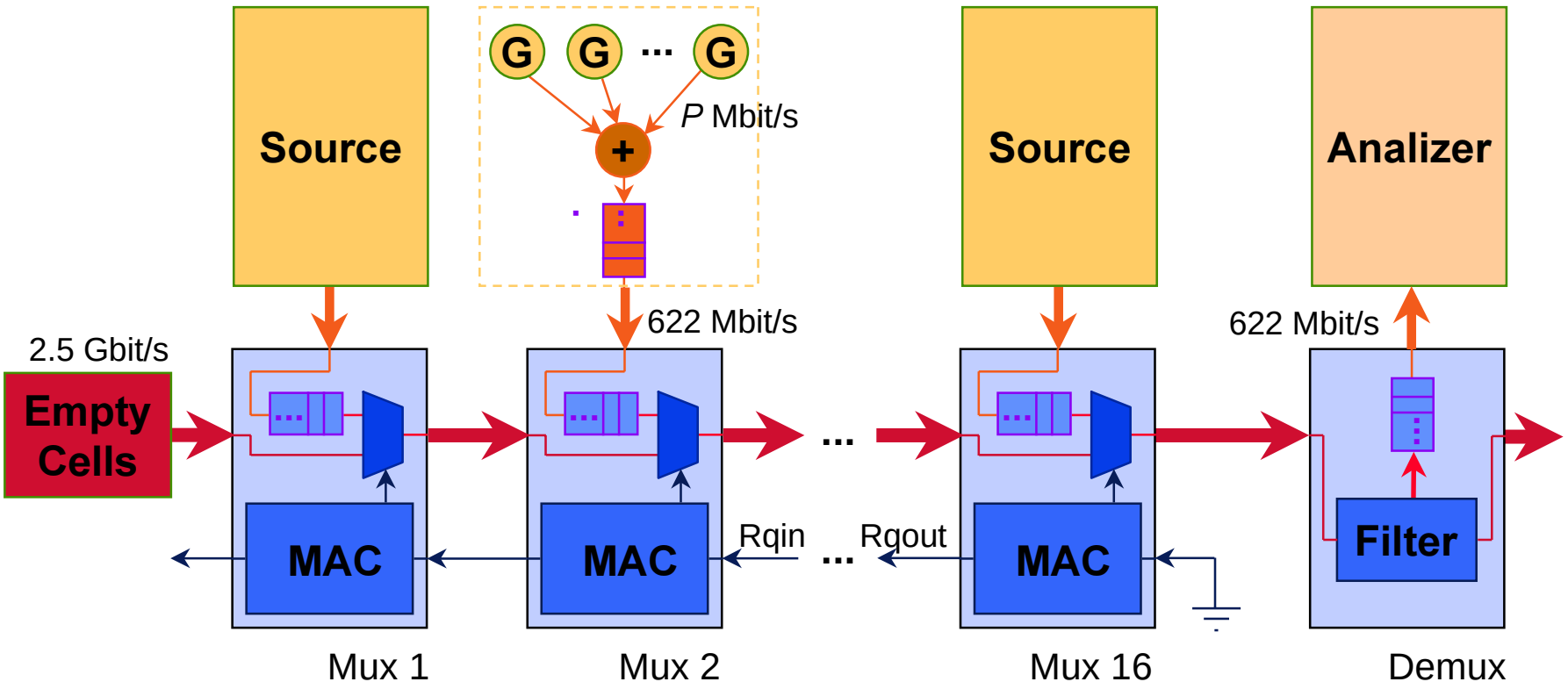
  Extracts cells from the high speed channel (2.5 Gbit/s) to a low speed receiver (622 Mbit/s).

  Functions

  - Filtering:
    - Verifies cells headers
    - Extracted cells can be eliminated from the channel
  - Data rate adaptation
    - Incomming cells are queued in a FIFO.

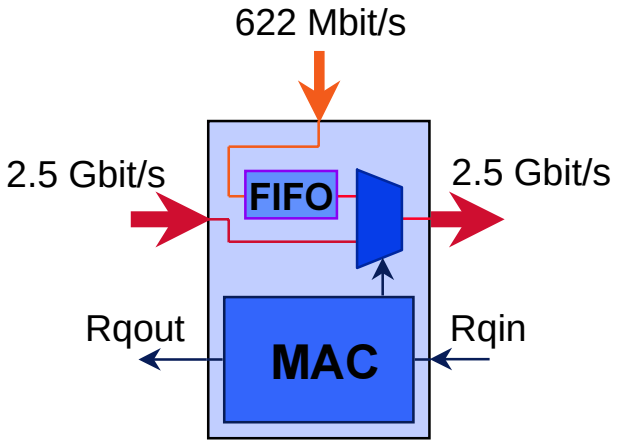


SIMULATION ENVIRONMENT



MODELS DESCRIPTION (i)

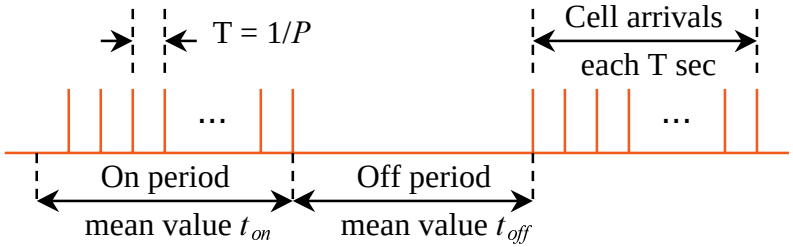
- MULTIPLEXER
  - Unbounded FIFO
    - FIFOs length measures with histograms
  - Several algorithms for medium access control (MAC)
    - Reference algorithm (IEEE 802.6)
    - Try to mantain a distributed global queue.
    - Inter node communications

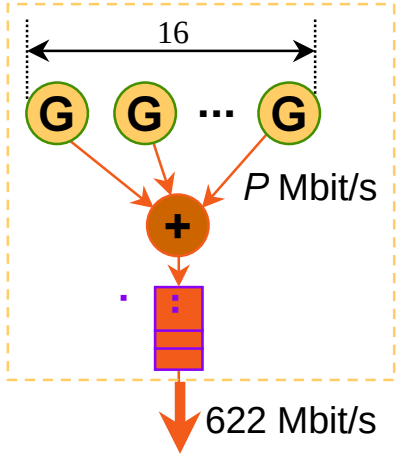


MODELS DESCRIPTION (ii)

❑ TRAFFIC SOURCES

❍ On/off model

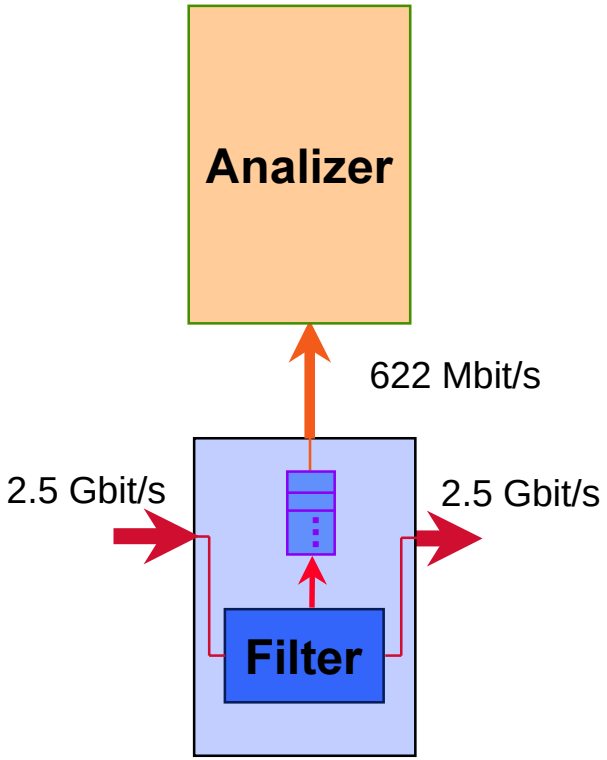




- ❍ Allows the representation of different services: Data, voice, video, etc.
- ❍ Each source: 16 Parametrizable On/Off generators + output FIFO
  - Parameters: *Ton*, *Toff*, *P*
  - Function $dist_exponential (independent seeds)
  - The FIFO limits the maximum peak rate to 622 Mbit/s.
- ❍ Cells abstraction, the only information is:
  - The arrival time to the multiplexer
  - A destination label

MODELS DESCRIPTIONS (iii)

- ANALIZER
  - Computes total delay and delay variation
  - Data is stored in histograms
- DEMULTIPLEXER
  - Unbounded length FIFO
  - Filter selects the cells to extract (programable)
  - FIFO length measurements with histograms



SIMULATIONS AND RESULTS (i)

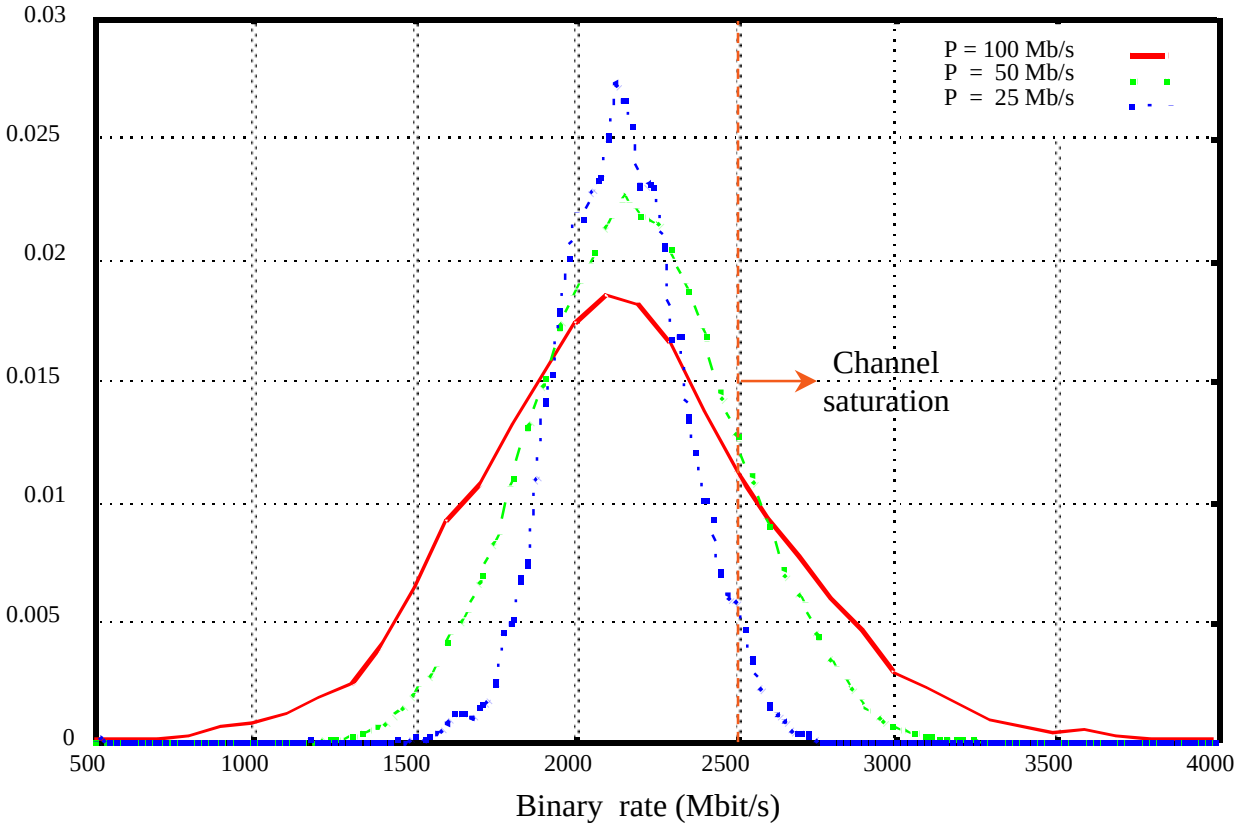
- TOTAL GENERATED TRAFFIC MEASUREMENTS
  - 16 Multiplexers with 16 on/off sources per multiplexer

Cond	P (Mbit/s)	t_{on} (ms)	t_{off} (ms)	b	B (Mbit/s)
1	100	0.5	5.5	12	8.33
2	50	1.0	5.0	6	8.33
3	25	2.0	4.0	3	8.33

  - Channel occupation 86% (14% empty cells)
  - Mean binary rate 2133 Mbit/s
  - Simulations length: 8 million cells in the high speed channel
  - Total generated traffic has a Gaussian pdf
  - Saturation (generated traffic > 2.5 Gbit/s) increases when burstiness (relation between peak and mean traffics, b = P/B) does.

SIMULATIONS AND RESULTS (ii)

- Taffic distributions

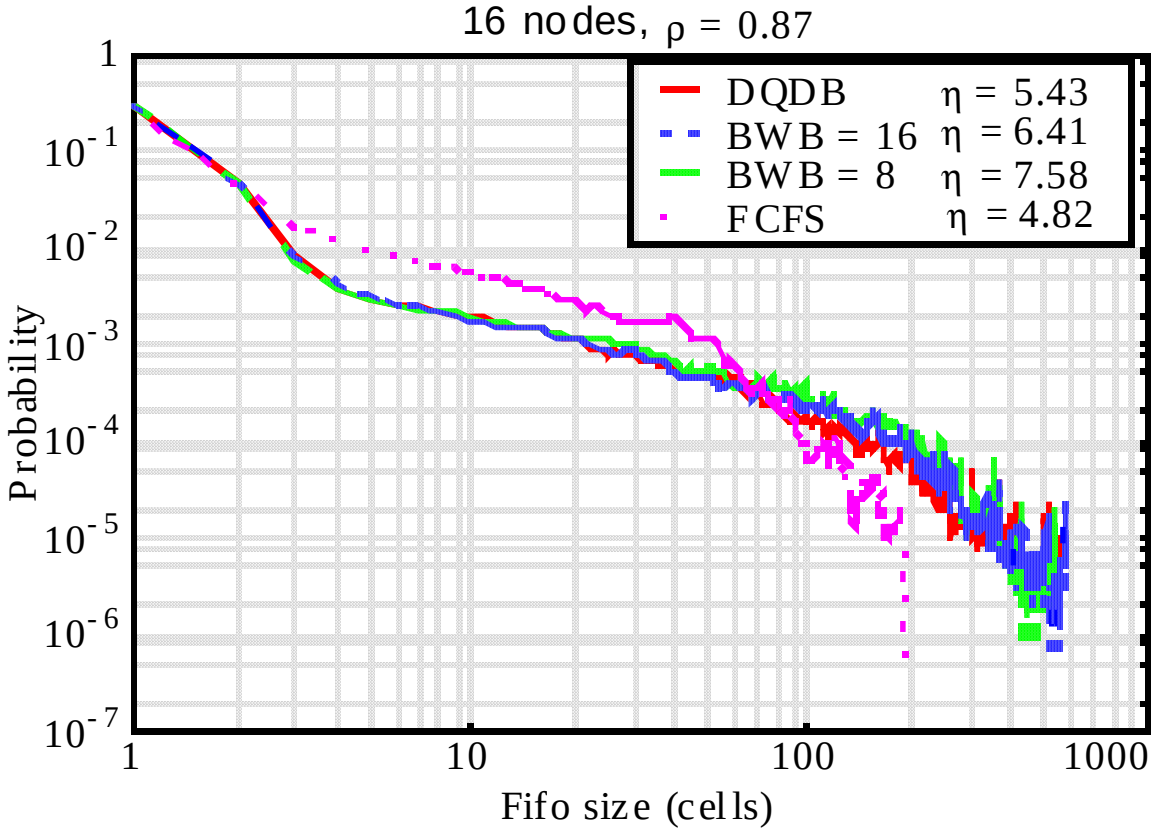


SIMULATIONS AND RESULTS (iii)

- MULTIPLEXERS SIMULATION
  - AIMS
    - Estimate FIFO size for a cell loss probability < 10^{-9}
    - Obtain the best MAC (FIFO size, delay, and position independence)
  - Simulated MACs: DQDB, BWB, FCFS
    - DQDB
      - High position dependence
    - BWB
      - Lower position dependence
      - Higher delay
      - Some bandwith is wasted
    - FCFS
      - Independent of node's position
      - Lowest delay

SIMULATIONS AND RESULTS (iv)

❑MULTIPLEXER FIFO SIZE

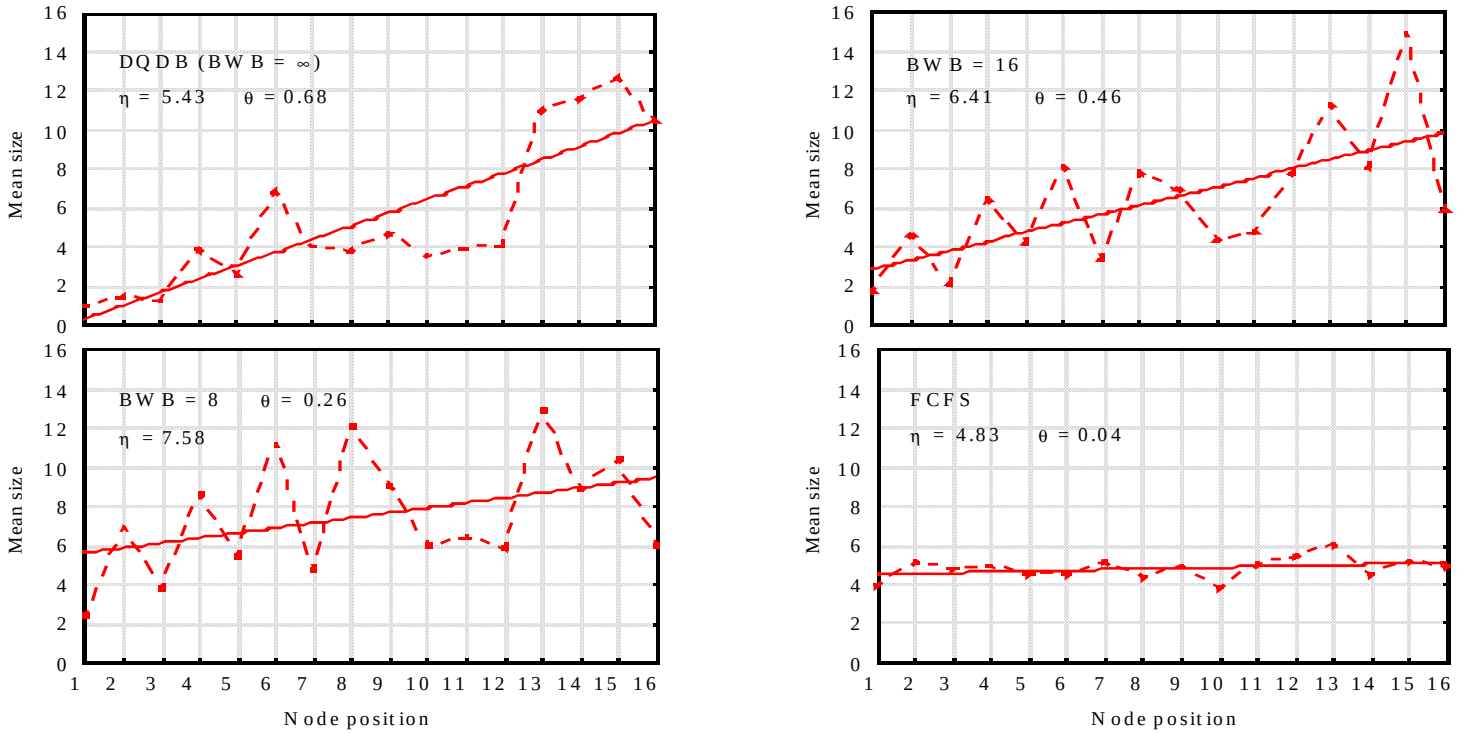


ρ: Mean channel occupation

η: Mean FIFO size

SIMULATIONS AND RESULTS (v)

❑NODE POSITION DEPENDENCE

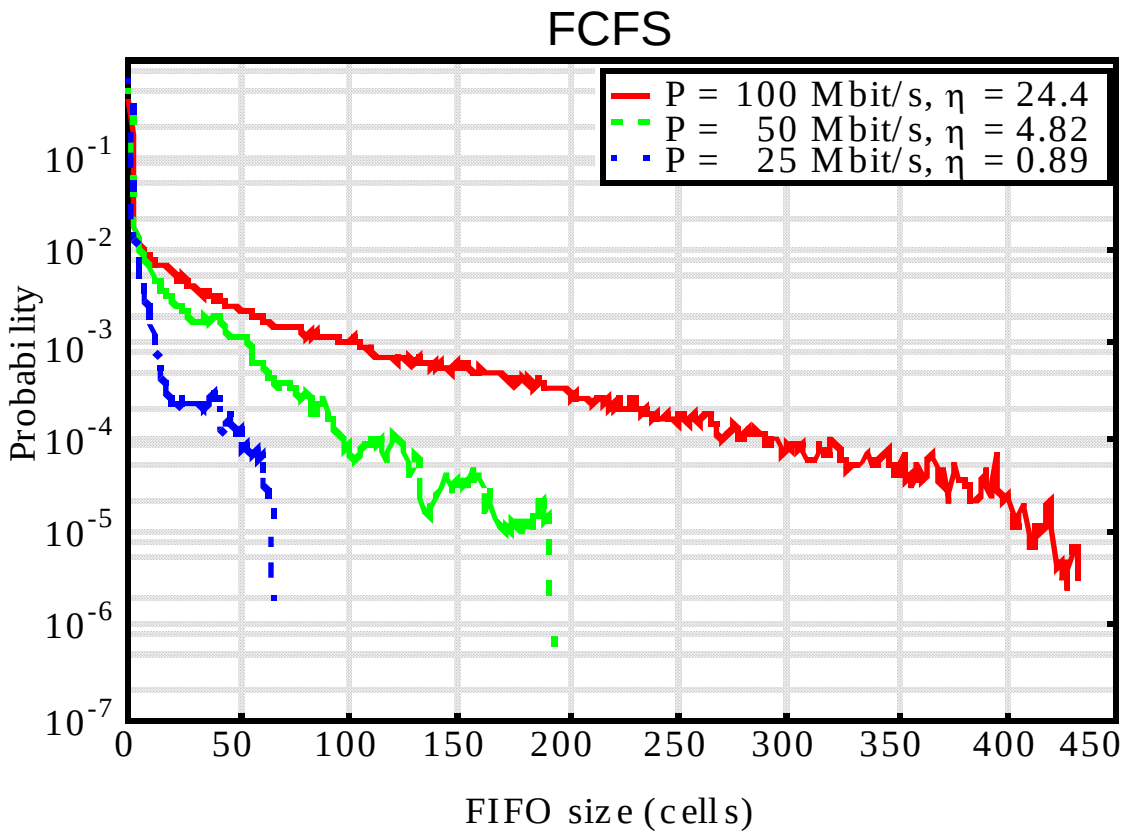


η: Mean FIFOs size over 16 nodes

θ: Interpolation slope

SIMULATIONS AND RESULTS (vi)

- DEPENDENCE ON TRAFFIC BURSTINESS

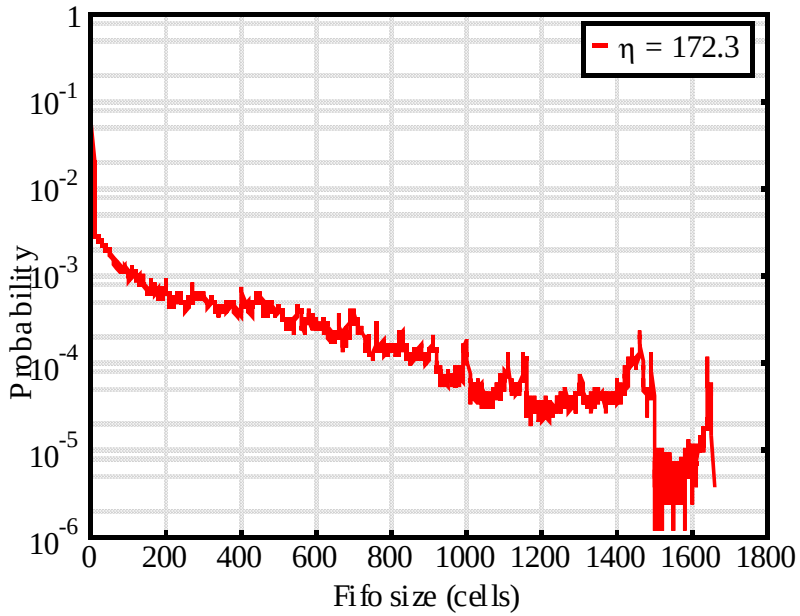


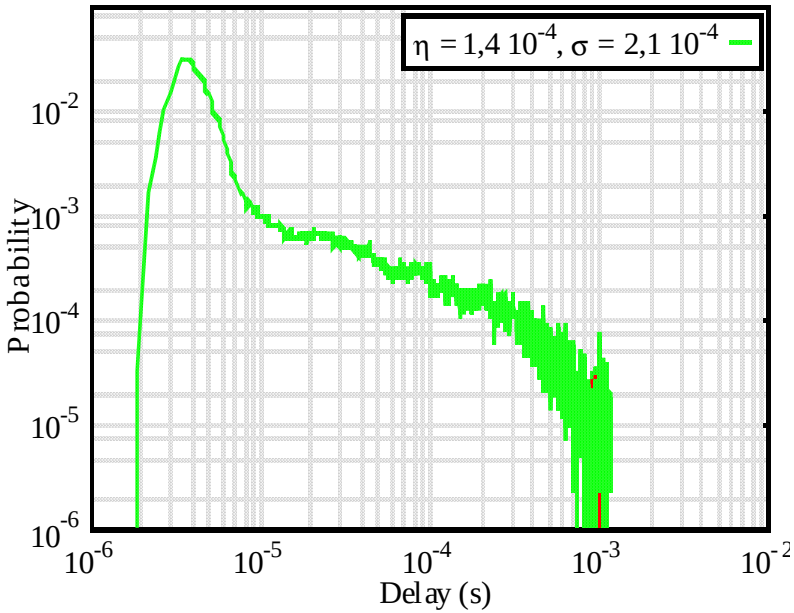
SIMULATIONS AND RESULTS (vii)

- DEMULTIPLEXERS SIMULATIONS
  - Estimate the FIFO size for a cell loss probability $< 10^{-9}$
  - Low speed channed mean occupation 86% (535 Mbit/s)
  - Dominant effect on delay

SIMULATIONS AND RESULTS (viii)

- DEMUX FIFO SIZE AND DELAY





CONCLUSIONS

- HDL Verilog has shown to fulfill the requirements for high level system definition and simulation
- Allows simple and fast implementations

Block	Number of lines
Source	112
Multiplexer	219
Demultiplexer	117
Analizer	52

- Supports diferent abstraction levels, and therefore fits easily in all design phases.
- Simulation times affordable ($3x10^5$ cells/hour using Verilog-XL on a Sparc 5 with 64 Mbytes RAM)

QUESTIONS & ANSWERS