Simulation of an ATM Network Using Verilog

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Abstract

High level modelling and simulation is a key element in the initial definition phase of an integrated circuit (ASIC) that is going to form part of a system. In this paper, the modelling and simulation with Verilog of the multiplexer/demultiplexer elements of a very high speed ATM (asynchronous transfer mode) network is presented. The system is built up by several ATM nodes that insert and extract traffic in a 2.5 Gbit/s channel, and where each node receives the traffic from an aggregate of on-off sources. Several simulations were performed with different algorithms for the common medium access control. Once the access algorithm was determined, several traffic patterns were also simulated to verify the system performance. The analysis of results was accomplished by means of a statistical study of the nodes traffic queue lengths histograms and of the cell delay variations in communications.

1. Introduction

The broadband integrated services digital network (B-ISDN) provides a common integrated access that supports a wide variety of services with different characteristics: interactive and distributive services, narrowband and broadband services (e.g. real time voice and video), bursty and continuous traffic (e.g. data and voice), etc. All of these different services have different quality requirements (e.g. voice is sensitive to delay and delay variation, while a certain percentage of errors is tolerable; on the other hand, non-real time data have no strict limits on delay, but require a high degree of integrity).

The asynchronous transfer mode (ATM) is the ITU recommended method for broadband systems [1, 2]. The ATM can be defined as a packet switching and multiplexing technique, which offers a high bandwidth utilization with a satisfactory quality for the final users. Through statistical multiplexing, several individual sources may share a high speed transmission link of capacity less than the sum of their peak rates. Through the statistical bandwidth assignment, a significant multiplexing gain can be achieved, especially for bursty traffic sources. This way of operation is especially attractive compared to the synchronous transfer mode (STM), since in STM a physical allocation of network resources (peak rate) to any connection is assumed for its duration. However, ATM requires effective congestion control strategies in order to guarantee a minimum quality of service in all connections. The congestion situation will arise in cases where two or more cells (a cell is the basic information transfer unit) coming from different sources, are directed simultaneously to the same destination. One of these cells is processed immediately while the remaining cells must be queued in a FIFO.

The work presented in this paper is motivated by the implementation need of an integrated circuit (AMDA ASIC) for multiplexing and access control to a very high speed (2.5 Gbit/s) ATM channel and the extraction (demultiplexing) of ATM connections from that channel. This ASIC will be used for high speed communications in backplanes and local/metropolitan area networks (LAN/MAN).

The ASIC design for ATM applications requires previous theoretical studies and extensive top-level simulations to determine the functionality of the circuit, the algorithms for traffic processing and the dimensioning of the FIFO queues that guarantee a very low cell loss probability.

In this paper it is presented the modelling and simulation of the multiplexing/demultiplexing elements of an ATM network, and the results obtained with the different models using Verilog as the tool for both description and top-level simulation. First, the functionality of the network nodes (AMDA ATM Multiplexer Demultiplexer ASIC) is briefly described, follows the description of the environment and simulation models, and finally the results obtained in the simulations are presented.

2. The AMDA functionality.

The basic functions of the high speed ATM multiplexer/demultiplexer ASIC (AMDA), are the addition/segregation of low speed ATM channels (up to 622 Mbit/s) to/from a 2.5 Gbit/s ATM flow.

In multiplexer mode, the traffic from the low speed sources is added to the high speed channel. In this

case, the low speed source will send cells to the AMDA that will be queued in its internal FIFO, waiting the arrival of empty cells on the high speed channel and replacing these cells. A key point in the multiplexing function, is the mechanism for the common medium access control (MAC). It must ensure to all nodes a similar probability of inserting its traffic, independently of its position in the network. This control must be distributed, so that the number of nodes will be easily scalable, and the network reliability is increased. There are several algorithms for the implementation of a distributed MAC, and one of the objectives of this work was to verify the different algorithms performances through statistical simulations. Ideally the algorithm must minimize the cell loss probability and the cell delay variation, enabling an even distribution of available bandwidth.

In demultiplexer mode, the high speed ATM channel cells header is verified, and those cells destined to the node are extracted. The extracted cells may be eliminated from the channel (replacing them with empty cells) or leaved on it (allowing point to multipoint communications and broadcasting). To decouple the data rates of the high speed channel and the low speed receiver, a FIFO stores the incoming cells, and the receiver reads the data from that queue at the required rate.

Each node of a network would contain two AMDAs one configured as multiplexer and the other as demultiplexer. All the nodes are linked in a bus as is represented in Figure 1.

3. The simulation environment.

The parameters to obtain from the simulation were the maximum length of the internal queues, the delay variation (CDV), and the dependency of both parameters with the node position.

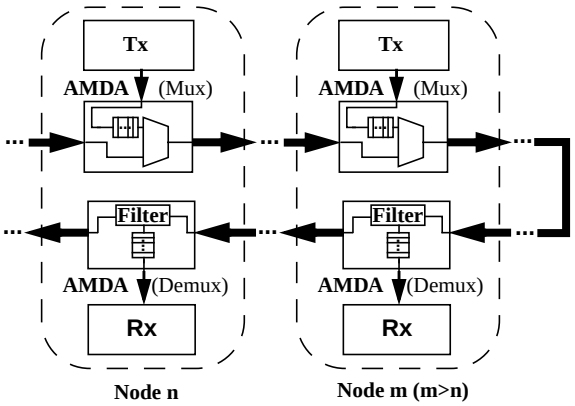

Figure 1: ATM Network

The simulation model used to obtain those parameters is shown in Figure 2. The multiplexer in the node at the leading end of the bus receives a continuous flow of empty cells at 2.5 Gbit/s trough the high speed channel. Each multiplexer adds the traffic from its low speed (622 Mbit/s) channel, replacing the high speed channel empty cells with source cells. The demultiplexers extract cells from the high speed channel to the analyser at 622 Mbit/s. The analyser performs the transmission delay measurements. All the models were described using the Verilog hardware description language (HDL). A reference network has been assumed consisting of 16 identical multiplexers, each one connected to an ATM traffic source, and only one demultiplexer. Each traffic source is composed in turn by 16 independent processes, to simulate the statistical behaviour of the traffic.

Considering that cell loss probabilities to obtain in an ATM system should be below 10^{-9}, it is necessary that the system simulations handle several millions of cells so that the obtained statistical values are meaningful. This forces to simplify as much as possible the ASIC, sources and traffic analyser models.

To assist in the validation of the results obtained with Verilog, the same model was simulated with the GPSS package, verifying that the results are practically identical in all the scenarios. Due to the high number of events that it is necessary to simulate, each block collects statistical data during the simulation and presents the results in a summarized report.

3.1. The multiplexer model.

As previously stated, there are mainly two parameters to measure in the system, the queues length and the cell delays. Concerning the queues occupation, since there was no initial estimation, they were modelled as infinite capacity FIFOs. On the other hand, to obtain the delay measurements, each cell arriving to a multiplexer, is tagged with the arrival time and a label identifying the destination, being this its only content. The FIFO length histograms measure the probability of the fact that in the arrival instant of a cell, there are N cells in the FIFO. These histograms are computed using a counters array, increasing the corresponding to the FIFO length in the arrival instant of each cell.

In addition to this FIFO, the multiplexer model includes the MAC description, whose algorithm is to be determined. As departure algorithm was used the MAC protocol used in the DQDB (Distributed Queue Dual Bus) network, that it is the basic architecture adopted by the IEEE as the metropolitan area network standard [6]. This algorithm attempts to maintain a global queue, distributed between the different nodes

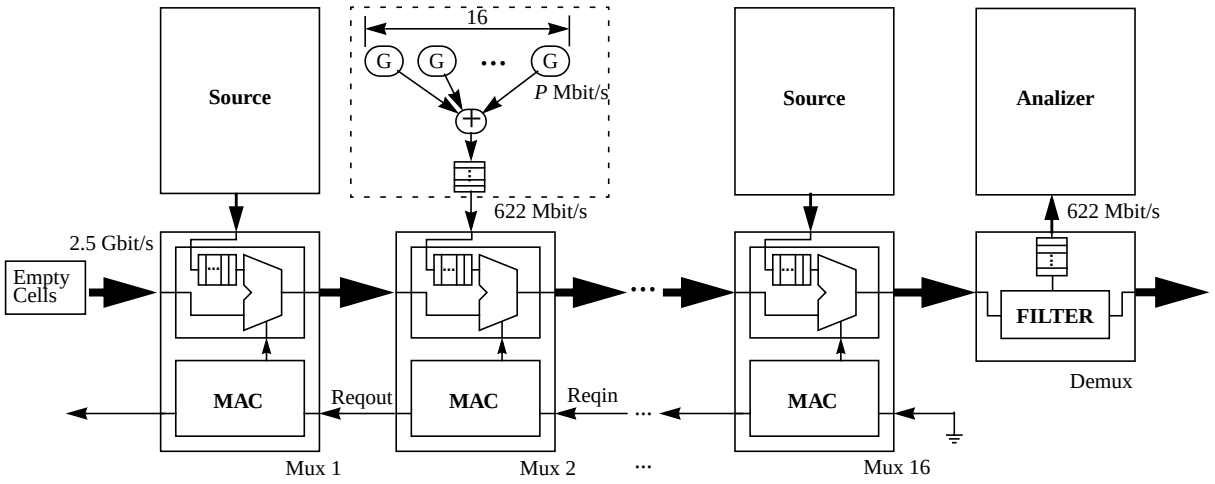

Figure 2: Simulation environment

of the net, with a round-robin service discipline. To maintain the global queue, each AMDA sends a request to inform the upstream nodes (the nodes preceding it in the data flow, see Figure 2) when it has a new cell ready for transmission. In response to these requests the upstream AMDAs should leave empty cells to pass trough, so that the downstream nodes may have the possibility to insert their cells.

In practice, due to the network transmission delays, the DQDB performance characteristics deviate from the ideal round-robin, resulting to a very position dependent behaviour of the network [7-10].

3.2. The ATM traffic sources.

Different models for the characterization of the ATM traffic sources have so far been identified [3, 4]. These traffic models have to be flexible enough to account for a large variety of services; video traffic is especially problematic due to its non Poissonian characteristics. One of these models, widely known and frequently used for ATM traffic modelling, is the on-off source model, which is an elementary one. Even though there are more accurate models [3] they are hardly used due to their complexity. Initially developed as a model for data transmission, it has been successfully used for the description of voice traffic [5], moreover, from Maglaris, et al. [4] it is derived that a video source can be modelled as a number of independent identical on-off source. This was the motivation to use 16 on-off independent traffic generators to model the nodes' sources.

The cell stream from a single on-off generator, is modelled as follows (see Figure 3): one period where the generation of the cells occurs (on), and a silence period with no cell generation (off). The on period is exponentially distributed with mean t_{on} ms. During this period we have cells arrivals every T ms, i.e., cells are generated with a binary rate P = 1/T. After the generation, and exponentially distributed silence period with mean t_{off} ms follows. The mean binary rate of each source is $B = P\ t_{on}/(t_{on}+t_{off})$. The burstiness is defined as the relationship between peak and mean rates, i.e. $b = P/B = (t_{on} + t_{off})/t_{on}$. The larger the value of this parameter, the greater the channel saturation probability for the same mean traffic, even though the statistical gain attainable also increases (increasing the FIFO size and cell delay variation).

The on-off generators are parametrizable to allow testing under different traffic conditions. Programmable parameters are the mean on and off times (t_{on}, t_{off}), and the peak binary rate during the on period (P).

Depending on these parameters and through the use of the "$dist_exponential" Verilog statistical function, the instants of cell generations are computed. As a previous step, the function was characterized to check the ranges where it matched closely the theoretical distribution, being detected a good approximation except around the origin.

The complete ATM source model is composed by 16 on-off generators and a FIFO. The FIFO has 16 input ports and one output port read at 622 Mbit/s. This way it is ensured that the maximum speed of the AMDA input interface is never exceeded. To assure

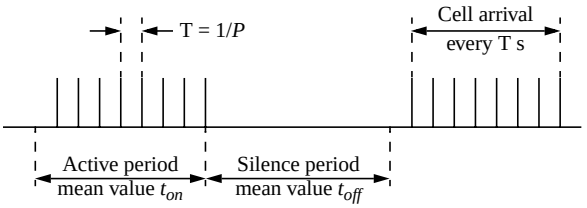

Figure 3: *On-off model*

that each on-off generator is independent from the other generators (non correlated generators), the last value returned for the current generator is passed as a seed to compute the following event in that generator.

3.3. The demultiplexer model.

The AMDA model operating as a demultiplexer, consists of a filter and a FIFO. The filter determines, depending on the cell value, if it must extract it to the FIFO or if it must leave it on the high speed channel. It is parametrizable to allow the simulation of different configurations. The FIFO is analogous to the one in the multiplexer, using the same mechanisms to compute statistics. This FIFO must be capable of absorbing the traffic peaks to adapt the speeds of both interfaces (2.5 Gbit/s and 622 Mbit/s).

3.4. The analyser model.

This model's function is to compute the cell delay variation (CDV) histogram. To accomplish this aim, it calculates the difference between the time instant when a cell enters some multiplexer, and the instant when it leaves out the demultiplexer. Histograms are computed as described previously.

4. The simulation results.

The first simulation was aimed to the measure of the total traffic added to the high speed channel. It was made to verify the validity of the source/multiplexer models. Generator parameters were programmed with conditions in table 1. In all cases, the mean traffic of each source equals to 8.33 Mbit/s, so that the mean load (ρ) of the high speed channel is 86%, but the burstiness is different in each case.

Table 1: Traffic conditions

Cond	*P* (Mbit/s)	t_{on} (ms)	t_{off} (ms)	b	*B* (Mbit/s)
1	100	0.5	5.5	12	8.33
2	50	1.0	5.0	6	8.33
3	25	2.0	4.0	3	8.33

The results presented have been derived collecting data from simulation runs representing a simulated time of 8 million cells. Traffic distributions are depicted in Figure 4. It can be appreciated that the generated traffic is of gaussian type, as corresponds to the addition of a high number of binomial distributions. Binary mean rate is in the three cases very close

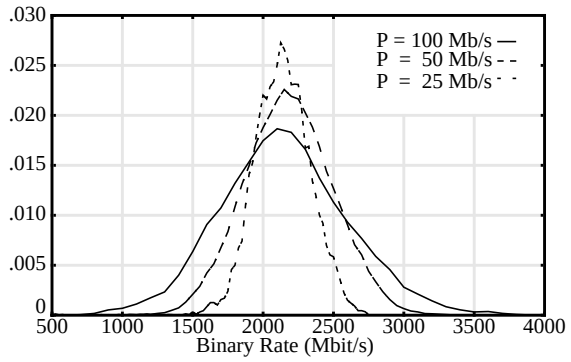

Figure 4: Traffic distributions

to the theoretical mean value of the gaussian distribution (2133 Mbit/s). Channel saturation, i.e. the area under the distribution curve for frequencies above 2,5 Gbit/s, increases as the peak rate of the sources and the burstiness do. The greater is the channel saturation, the larger will be the FIFO queues length of the multiplexers and therefore the cell delay variation.

4.1. The multiplexers simulation

It is necessary to estimate the multiplexers FIFO size, for a cell loss probability in the order of 10^{-9}. First, it was tried to determine the best algorithm for medium access control (MAC), in the sense that it produces a lower FIFO occupation and a greater independence with the node position. The studied algorithms where the DQDB, BWB and FCFS.

The band width balancing mechanism (BWB) is a modification of the DQDB to provide bandwidth allocation, among the nodes of an overloaded network, in a position independent way [7]. It has the drawback that part of the total bandwidth of the network is wasted (depending on a parameter designated module: MOD), and cell delay increases. To try to solve these drawbacks, new variations on the DQDB were proven, but with a first-come-first-served (FCFS) service discipline. Figures 5 and 6 show the simulation results.

Figure 5 depicts the mean FIFO length histograms over all the multiplexers for the algorithms considered: DQDB, BWB (MOD: 16 and 8) and FCFS. The values in the legends represent the network-wide values of the measures presented. η denotes the mean FIFO length of all nodes, and ρ the mean load offered by all the nodes. It can be observed that the smaller the value of MOD the greater are the FIFOs mean length and the longer are the histograms tails. (MOD infinite is equivalent to DQDB). It can be observed also that maximum sizes, and FIFOs mean length, are quite smaller with FCFS than with DQDB. So, in

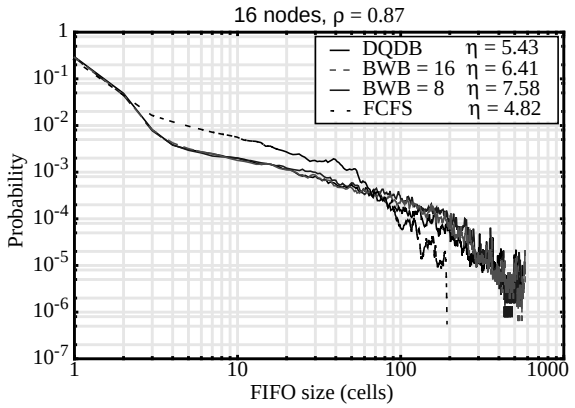

Figure 5: FIFO size histograms

terms of FIFOs size, FCFS algorithm greatly improves the DQDB, and the latter is slightly better than the BWB. Obtained results can be extrapolated with some techniques [11], to determine the quality of the required service (cell loss probability of 10^{-9}).

Figure 6 presents (with points joined with dashed lines) the FIFOs length against the node position (node index increases downstream) and the interpolation line (with a continuous trace). In the legend, besides the mean length (η) is presented the slope of the interpolation line (θ). The graphics reflect that the DQDB algorithm has a strong dependency with the node position, dependency attenuated with the BWB mechanism as the module is reduced, and it is almost null with the FCFS algorithm. Based on the results from Figs. 5 and 6 it can be concluded that the FCFS algorithm is the best one for the medium access control in the ATM network.

Once determined the algorithm, simulations under the different traffic conditions described in table 1, were performed to verify their effect on the FIFOs lengths. In Figure 7, are shown the FIFOs mean length histograms. It is observed that the histograms tails increase with the peak rate and the burstiness. (the percentage of time the channel is saturated grows with those factors and the FIFOs lengths increase very quickly when the channel saturates)

4.2. The demultiplexers simulation

In a similar way as for multiplexers, it is necessary to estimate the size of the demultiplexer FIFOS, so that the cell loss probability of extracted cells from the high speed channel will be of 10^{-9} or lower. As in that case, estimation is accomplished through extensive simulations where the mean traffic extracted by one demultiplexer node is one fourth of the network mean traffic, i.e 2488,32x0,86/4 = 622,08x0,86 = 535 Mbit/s. The traffic is generated by the multiplexers network of the previous point, with parameters values of condition number 2 in table 1. The peak traffic is obviously equal to the network capacity (2,5 Gbit/s). The obtained results correspond as in the case of the multiplexers to a simulation time of 2 million cells in the high speed channel.

In Figure 8 are shown the histogram and mean value (η) of the demultiplexer FIFO length and the cell delay variation (CDV). It can be observed that the demultiplexer FIFO sizes are very large, much than

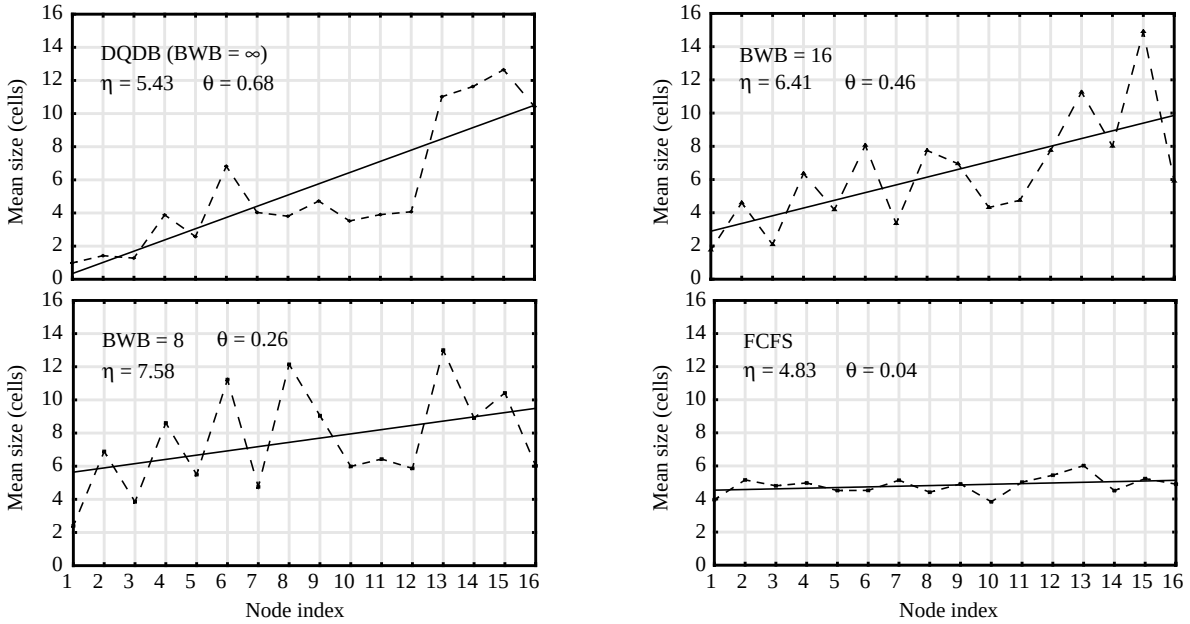

Figure 6: Node position effect

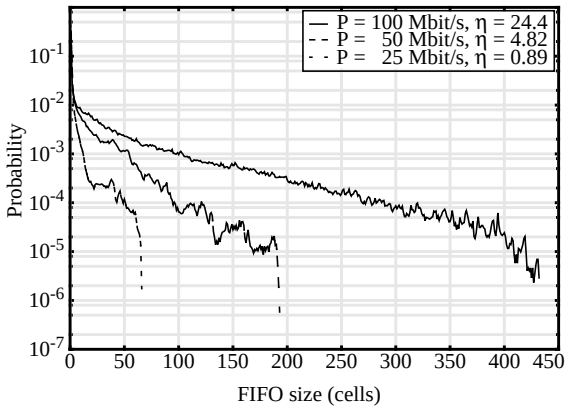

Figure 7: FIFO size under different traffic conditions

the multiplexers FIFOs (as studied in the previous paragraph), and so, they have a dominant effect on the delay.

5. Conclusions

In the present work the use of Verilog for a very high level simulation of an ATM network has been presented. Verilog is a language commonly used for hardware systems description and simulation, nevertheless it is a design language that supports top-down methodology, allowing different abstraction levels: functional descriptions, structural descriptions and a mixture of both, and therefore it integrates easily in all the ASIC design cycles. Verilog can be used efficiently for top-level system simulations, since it allows very fast and simple model implementations. Furthermore, though the simulator employed (Verilog-XL) is an interpreter, the simulation times seem reasonable (approximately 300 000 cells per CPU hour in a SUN Sparc-5 with 64 Mbytes of RAM). It could be expected that these times will improve significantly with a compiled simulator.

Acknowledgement

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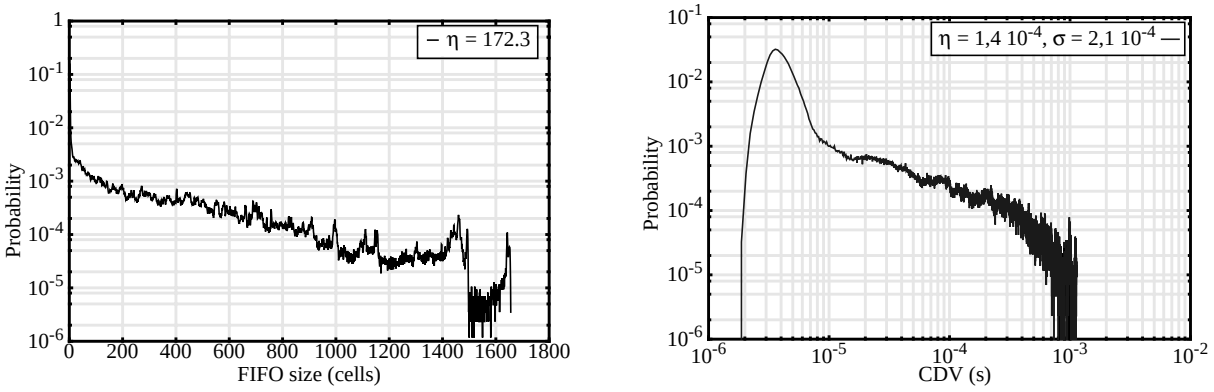

Figure 8: Demultiplexer FIFO size and cell delay variation