The μPP ASIC: Design, Methodologies and Tools for a Pay Phone System-On-a-Chip Based on an ARM Core and Design Reuse

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Objective

To describe the μPP integrated circuit (*Microcontroller for Pay Phones*)

- Motivations and Concerns
- Architecture and Functionality
- Design Methodology and Reuse

Outline

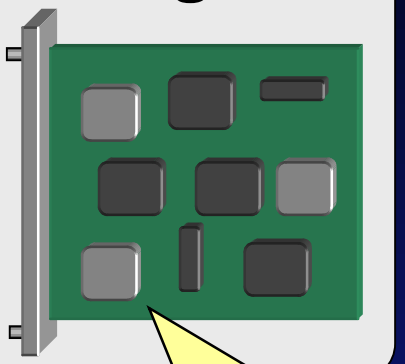
- INTRODUCTION
- GENERAL DESCRIPTION
- ARCHITECTURE
- BLOCKS AND REUSE
- METHODOLOGY
- PHYSICAL FIGURES
- CONCLUSIONS
- QUESTIONS & ANSWERS

Introduction

- TI+D Designed the Spanish Pay Phone System (TM) in 1990
- Deployed Mainly in Spain & South America
- In 1997 TID revised the design: The TMPLUS
- TI+D is now preparing the next version based on a SOC device: the μPP microcontroller

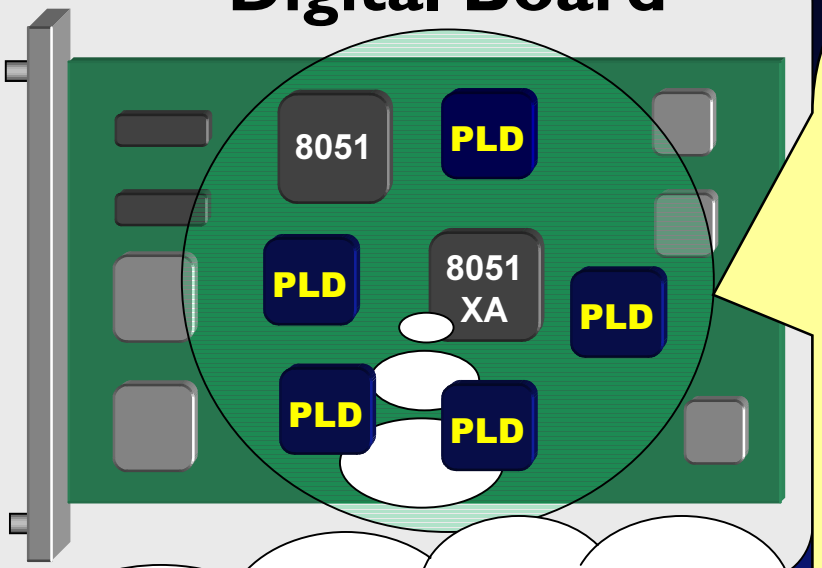
General Description

Analog Board



- Phone line interface
  - Speech
  - Ring
  - Tone filters
- Power supply

Digital Board



- Two micros:
  - 8051 (supervisor)
  - 8051XA (main processor)
- Peripherals:
  - Keyboard
  - LCD
  - Real time Clock
  - Pay Systems
  - Comms.

System-on- a-Chip Solution

µPP

Esprit Project 20724 (TOMI)

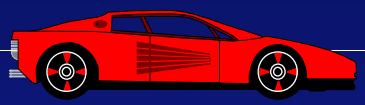
Design Objectives

- **TOMI ESPRIT Project 20724**
  - **Development of the μPP ASIC**

✔ **Increase Integration Level**

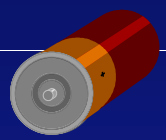
- **Reduce Cost**

- **Higher Performance**



- **Increase Reliability**

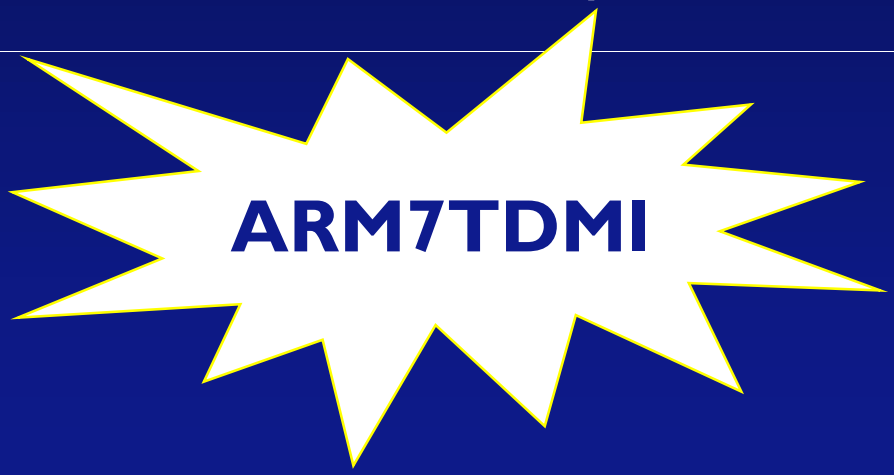
- **Lower Consumption**



✔ **Gain Experience in Designs Using Embedded Cores, IP Modules & Tools**

Design Concerns

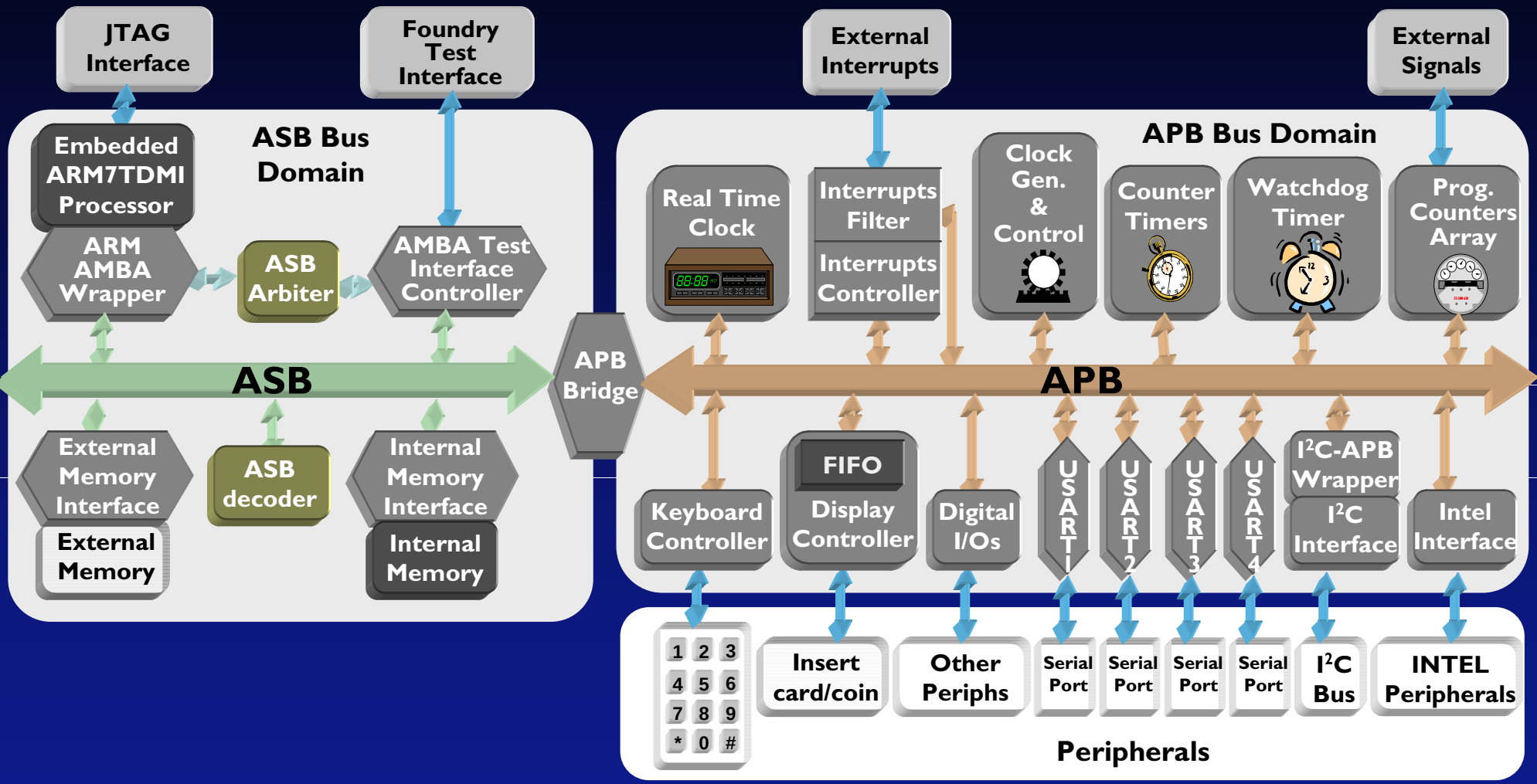
- Low Power (Supply from the Telephone Line)
- High Performance
- Small Size
- Availability from different ASIC foundries
- Reference Architecture and Hardware IP Modules
- Commercial Software (RTOS, soft modem, etc.)
- Code density
- Software debug interface



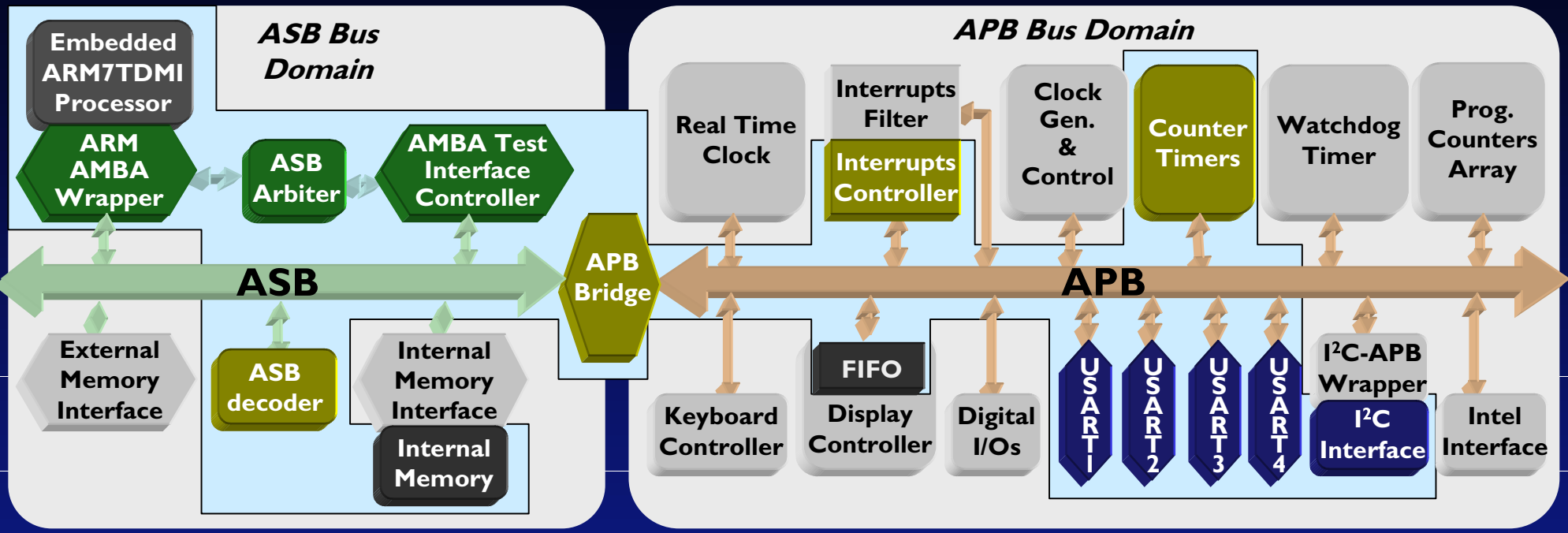
Circuit Architecture

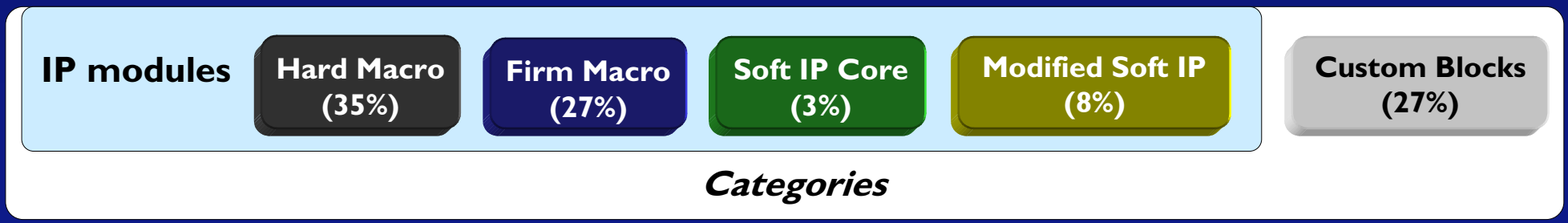
- Based on ARM's *Advanced Microcontroller Bus Architecture* (AMBA)
- Hierarchical
  - *Advanced System Bus* (ASB): High-Speed, High-Bandwidth, Multimaster
  - *Advanced Peripheral Bus* (APB): Low-Power, Low-Speed, Unclocked
- Advantages
  - Standard Hierarchical Architecture for Embedded Microcontrollers
  - Easy Division between High and Low Performance
  - ARM *Micropack* Provides:
    - Modules required to perform ASB and APB functionality
    - Examples of APB and ASB peripherals
    - Compliance testbenches for designing new APB and ASB modules
    - Easy Technology Re-targeting (HDL Synthesisable Code and Scripts Provided)

Circuit Blocks

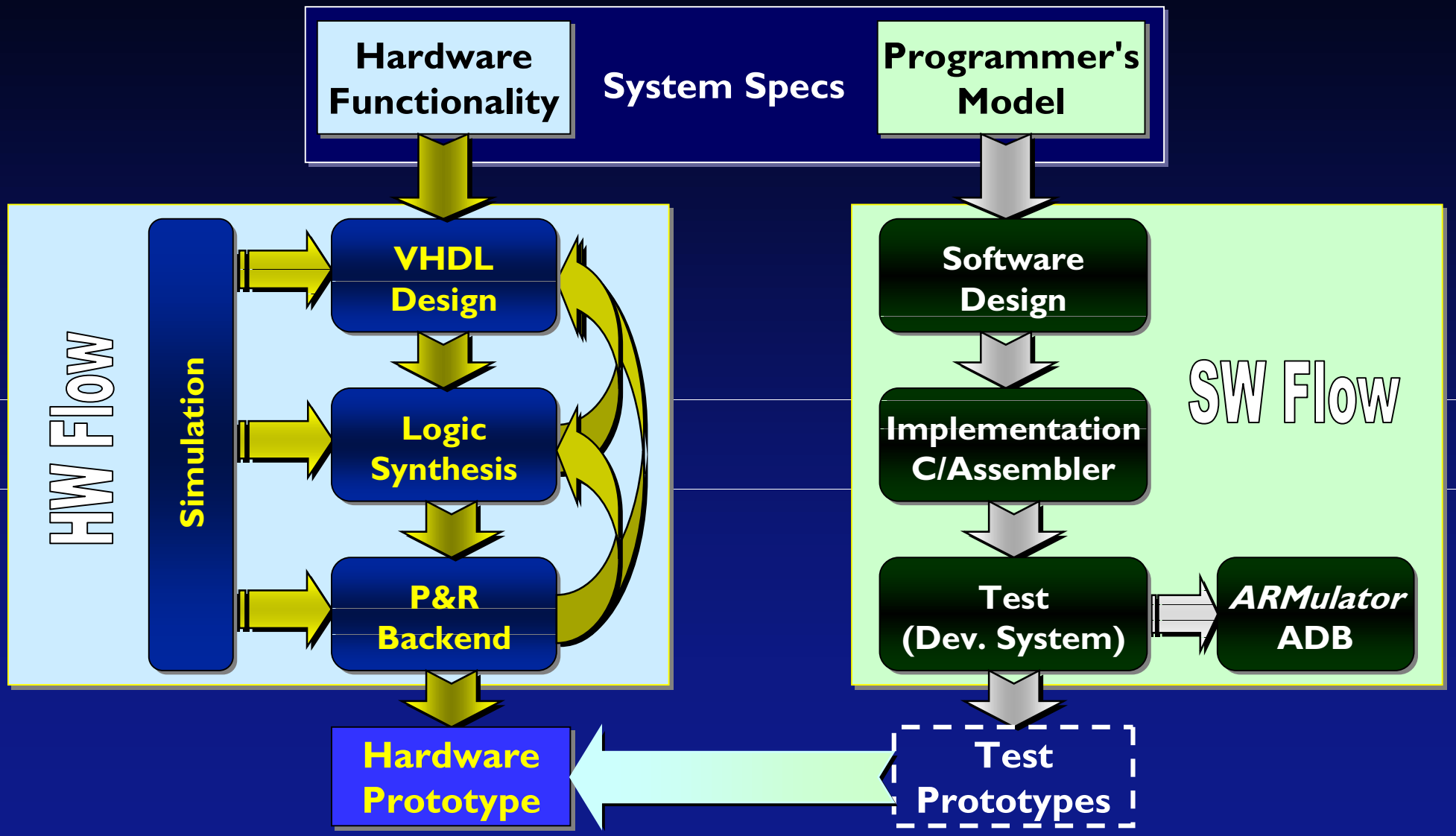


Design Reuse





Design Methodology



Hardware Design Flow

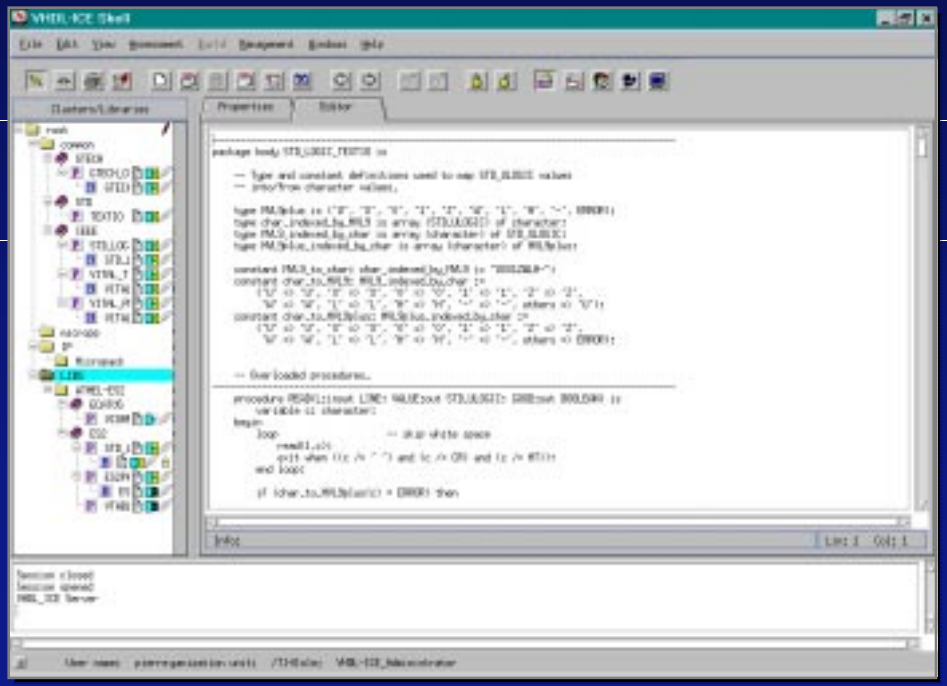
- Hard Cores (ARM7TDMI, Memories):
  - Only Simulation Model & Abstract
- Firm Blocks (USART'S and I^2C):
  - Gate *Netlist*
- Soft & Custom Blocks:
  - VHDL Customization (Soft *IPs*)
  - Latch Based RTL or Structural (GTECH) VHDL (Custom Blocks)
  - Simulation using Compliance Test-benches
  - Synthesis (*Micropack* Scripts)
  - Timing Analysis (Clock Block)
- Hardware/software Co-simulation Using Arm Model
- Test
  - Scan Chains for ARM and I^2C
  - BIST for Memories
  - AMBA Test Methodology using *Test Interface Controller* (TIC)

Software Design Flow

- Run In Parallel With The Hardware Design
- Software Development System
  - ARM Software Development Kit (including *ARMulator*)
  - ARM Development Board with Embedded-ICE
- Software Design
  - Starting from existing Software (ANSI C) for 8051 Microcontroller
  - Using an "Open" Programmer's Model (Relative Addresses)
  - Coding device drivers in Assembler and C
- Software Debugging System
  - ARM Software Development Kit
  - Final Application Board with Embedded-ICE Interface
- Hardware Software Co-simulation
  - Interrupts Service Routine simulated with HDL hardware model

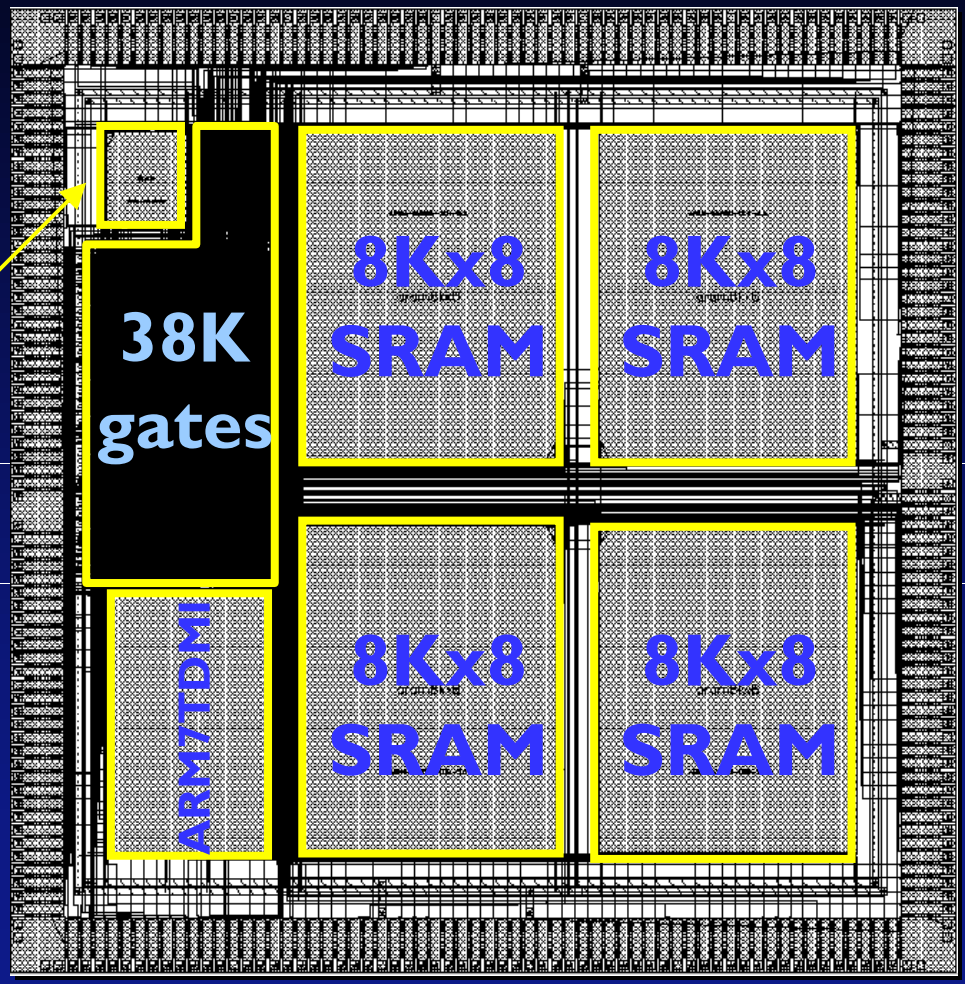
Design Management

- µPP is a Demonstrator for ESPRIT 20724 (TOMI: *Tools for OMI*)
  - ***Provide missing methods and tools to make practical the OMI concept of Supercells based system design***
- VHDL design management tools:
  - **Management and Reuse for Supercell-based design**
- VHDL-ICE:
  - **Client/Server**
  - **Multiplatform, distributed database**
  - **Several Concurrent Clients**
    - **Design Manager**
    - **Design Navigators**
    - **Assessment Tools**
    - **API for Third Party Tools**



µPP Circuit Main Figures

- 68K equivalent gates (excluding memory)
- 256Kbits (4*8Kx8) of single port static RAM
- 2Kbits (256x10) of Dual Port RAM
- Embedded ARM7TDMI
- 72.25 mm^2, ATMEL ECAT05 (0.5 µm CMOS)
- CQFP 304 pins package (samples)
  - 234 functional pins
  - Production will be in 256 PQFP
- 1-16 MHz/32 KHz selectable Clock
- 0.6 mW (sleep mode) to 300 mW



Conclusions

- Example of SOC solution for an existing System
  - Reducing final cost.
  - Increasing Reliability
  - Improving significantly system performance.
- Design Based on IP reuse
  - Reduction in design time
  - Confidence in the “First Time” success (IP modules proven in Silicon)
- Parallel development of Hardware and Software
  - Design interaction: Software needs are supported by Hardware
  - System “Ready to go” with the reception of circuit prototypes
- HDL Design Management tools:
  - Useful in IP based Designs