

CS623: CAD FOR VLSI DESIGN

Project

Weightage: 30

Last date: 5.00 PM, May 15, 2002

Instructions

1. All the files related to the project along with a report in Latex format should be kept in the home directory of your group in Lathangi in the directory named `proj_g< Group Number >`. For eg., Group 1 should put all files and report in the directory `proj_g1`.
2. Groups finishing early can come for a demo and individual viva-voce earlier.
3. All members of groups who have not given their demos before May 15 should be available for Demos scheduled on May 16, 17 and 18. The schedule will be available on the course web page.

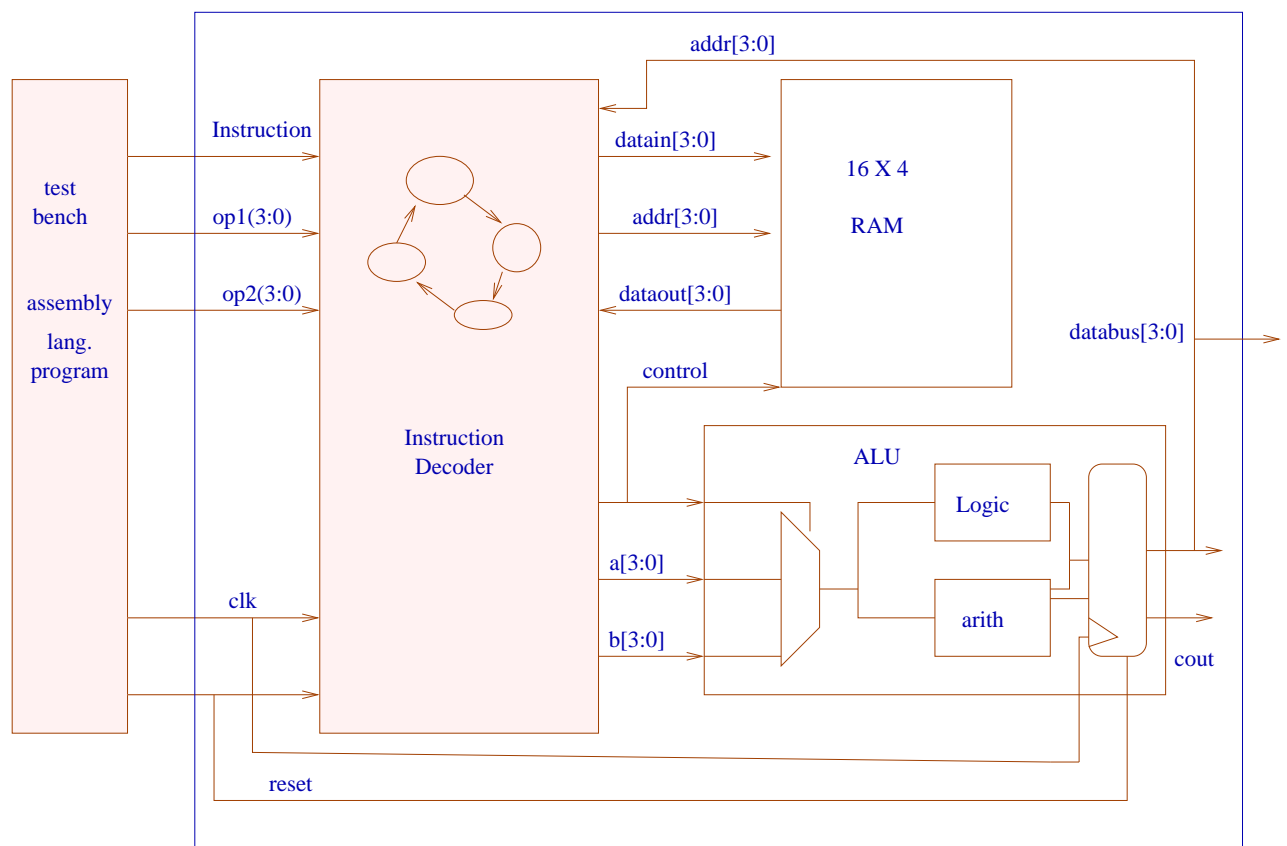
1 Design the 4-bit processor

Given the 4-bit processor of Assignment 1, complete all the steps of the Alliance CAD flow and produce a CIF (Caltech Intermediate Form) file for the same. The steps to be followed were listed in the Alliance CAD demo lectures of the course. A set of tutorials along with the lecture notes for using the Alliance flow is available on the course website. You may copy `/faculty/kama/.bash_profile` file into your home directory for setting up the PATH and other environment variables.

The following are some of the extensions which is needed to complete the project.

- Use the concept of **expanding opcodes** and include one more instruction called **dump** and this would have no arguments. The dump instruction will dump all memory values starting from address 0 to maximum address of your memory, one-by-one on the data bus at some regular intervals.
- Every test written for the processor must include a **dump** instruction at the last.

Figure 1



- Given an assembly language program for the processor, develop a program that will generate a pattern file that can be used at different stages throughout the design. The pattern file should be self-checking, meaning it should verify the content of the memory dumped by the `dump` instruction.
- Develop a small random test generator that will generate random assembly programs for the processor along with the memory image after executing the program to be appended to the pattern file.
- A pipelined implementation with better instruction throughput will be highly favored.

All the Best