

CS623: CAD FOR VLSI DESIGN

Assignment 2

February 28, 2002

Weightage: 10%

Submission Date: 20 Mar, 2002

1 Introduction

The assignment is to develop a synthesis tool for a very small subset of Verilog constructs. The synthesis tool should include the `genlib.h` in the course web-page and translate the verilog constructs using the modules defined in `genlib.h`

1.1 The Verilog Constructs

The two verilog constructs to be supported include

1. Continuous Assignment Statement.
2. `if` and `case` statement inside non-clocked always blocks. with a restriction that every branch of the conditional statements have *at most one* verilog statement.

1.2 Different Steps

The assignment comprises of **two** major steps with weightages 4 and 6.

1. Take a verilog program which has **only** continuous assignments; and, non-clocked always blocks with only `if` and `case` statements.
Translate them into a net-list using the different modules given in `genlib.h` and fill in the different modules in `genlib.h` that are used by your translator with the necessary code in Verilog. Replace the original Verilog code with the synthesized code and re-run the test bench.
2. In an arbitrary Verilog program, identify the above constructs and replace them alone with the translated net-list and re-run the test bench.