

CS623: CAD FOR VLSI DESIGN

March 28, 2002

Weightage: 10 marks

Last date: April 7, 2002

1. Design a synchronous BCD counter by developing a Layout of the same in MAGIC. Extract the layout and interface with IRSIM to show the behaviour. **(4)**
2. Design a 3-bit pipelined adder (shown in the figure) in MAGIC and perform layout extraction and interface with IRSIM. **(6)**

