

Packaging Effects on Reliability of Cu/Low- k Interconnects

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Invited Paper

Abstract—Chip-packaging interaction is becoming a critical reliability issue for Cu/low- k chips during assembly into a plastic flip-chip package. With the traditional TEOS interlevel dielectric being replaced by much weaker low- k dielectrics, packaging induced interfacial delamination in low- k interconnects has been widely observed, raising serious reliability concerns for Cu/low- k chips. In a flip-chip package, the thermal deformation of the package can be directly coupled into the Cu/low- k interconnect structure inducing large local deformation to drive interfacial crack formation. In this paper, we summarize experimental and modeling results from studies performed in our laboratory to investigate the chip-package interaction and its impact on low- k interconnect reliability. We first review the experimental techniques for measuring thermal deformation in a flip-chip package and interfacial fracture energy for low- k interfaces. Then results from three-dimensional finite element analysis (FEA) based on a multilevel submodeling approach in combination with high-resolution moiré interferometry to investigate the chip-package interaction for low- k interconnects are discussed. Packaging induced crack driving forces for relevant interfaces in Cu/low- k structures are deduced and compared with corresponding interfaces in Cu/TEOS and Al/TEOS structures to assess the effect of ILD on packaging reliability. Our results indicate that packaging assembly can significantly impact wafer-level reliability causing interfacial delamination to become a serious reliability concern for Cu/low- k structures.

Index Terms—Chip-packaging interaction, Cu/low- k , moiré interferometry, packaging effect, submodeling.

I. INTRODUCTION

STRUCTURAL integrity is a major reliability concern for high-density flip-chip packages due to large deformation and stresses generated by thermal mismatch between the silicon die and the substrate. By employing underfills, thermal

stresses at the solder bumps can be effectively reduced to improve package reliability [1]. However, the underfill causes the package to deform, leading to large peeling stresses at the die-underfill and die-solder interfaces, which significantly impact packaging reliability. At this time, the Al/oxide interconnect is being replaced by Cu damascene structures with oxide and low- k interlevel dielectrics. Compared with oxide, the low- k dielectric is softer, expands more and adheres weakly to other materials. For a standalone wafer structure, under a thermal loading from wafer process temperature (400 °C) to room temperature, an energy release rate of less than 1 J/m² has been reported for interfaces in Cu/low- k structures [2]. This is about five times less than fracture energies measured for low- k interfaces by the four-point bend test. While this indicates that interfacial delamination is not a critical issue for a standalone die, the problem is commonly observed in Cu/low- k interconnects after assembling the die into a plastic flip-chip package. This raises an important question concerning the effect of packaging driving interfacial delamination and its impact on the reliability of Cu/low- k chips.

In this paper, we first review high-resolution moiré interferometry, a powerful experimental technique for measuring thermal deformation in a flip-chip package. This is followed by a discussion of interfacial fracture energy measurement for low- k interfaces. Then results from three-dimensional (3-D) finite element analysis (FEA) to investigate the chip-package interaction based on a multilevel submodeling approach for low- k interconnects are discussed. Here the modeling results are verified using thermal deformation measured by high-resolution moiré interferometry. With a phase-shift technique, the resolution of moiré interferometry can reach 26 nm per fringe order, which is sufficient to determine deformation and strain distributions accurately within a small area, e.g., a solder bump, in the package. After verifying FEA at the packaging level, multilevel submodeling was conducted one level of detail at a time, extending from the first submodel level of the package around the solder bumps with the highest deformation to the final submodel level of the Cu/low- k interconnect. Simulation details and problems related to submodeling will be presented and discussed. In the submodel at the interconnect level, a crack with fixed length was introduced at relevant interfaces. A modified virtual crack closure (MVCC) technique was used to calculate the energy release rate. In our study, with the local stress and strain distributions obtained by modeling, the components of energy release rate corresponding to the three basic

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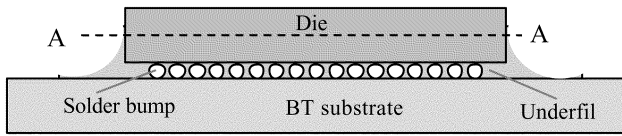


Fig. 1. Flip-chip package attached to substrate with solder bumps surrounded by underfill.

fracture modes 1, 2, and 3 can be separately determined. This enables us to evaluate the critical energy release rate at various interfaces with a properly defined mode mixity. Critical energy release rates calculated for relevant interfaces in Cu/low- k structures are compared with corresponding results obtained for interfaces in Cu/TEOS and Al/TEOS structures to assess the effect of ILD on packaging reliability. Our results indicate that packaging assembly can significantly impact wafer-level reliability causing interfacial delamination to become a serious reliability concern for Cu/low- k structures. Finally, the results from a study of the scaling effect on packaging reliability as a function of linewidth are reported.

II. EXPERIMENTAL MEASUREMENT OF THERMAL DEFORMATION FOR FLIP-CHIP PACKAGES

As shown in Fig. 1, a flip-chip package is formed by directly attaching a chip upside-down to a substrate with solder bumps. The large thermal expansion mismatch between the silicon die and the substrate introduces significant thermal stresses in the package, especially for the solder bumps along the outer rows. Underfill is commonly used to fill the gap between solder bumps in order to reduce the thermal stresses in the solder bumps, hence improving the solder reliability. However, new interfaces are introduced with the presence of underfill, such as solder-underfill, underfill-silicon and underfill-substrate interfaces. Delamination along these interfaces induced by thermal stresses generated during thermal cycling is frequently observed. Thermal deformation in the package is directly related to its geometry and the materials used in the package.

Thermal deformation of a flip-chip package can be determined using an optical technique of moiré interferometry. This is a whole-field optical interference technique with high resolution and high sensitivity for measuring the in-plane displacement and strain distributions [3]. Recently, this method has been successfully used to measure the thermal-mechanical deformation in electronic packages to investigate package reliability [4]–[6]. A widely used moiré interferometer for electronic package analysis is the portable engineering moiré interferometer (PEMI) originated from IBM. In its standard form, a grating frequency of 1200 lines/mm is used, which yields a spacing of the interference fringe corresponding to 417 nm of in-plane displacement. The sensitivity is adequate for measuring the overall thermal deformation of electronic packages but not sufficient for measuring thermal deformation in high-density electronic packages, particularly for small features, such as solder bumps. For such measurements, a high-resolution moiré interferometry method was developed in our laboratory based on a phase shifting technique [5]. With this method, a resolution of 26 nm per fringe was achieved.

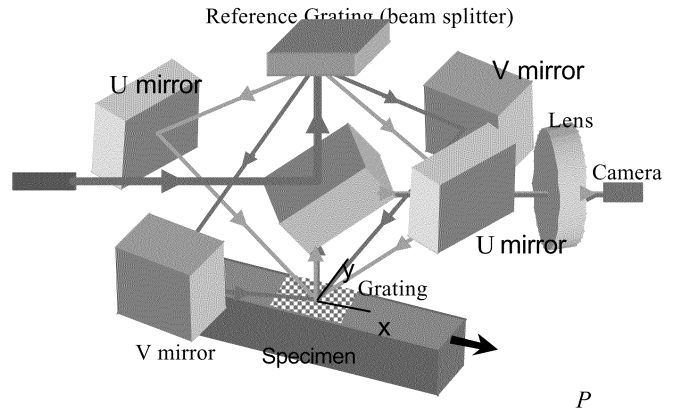


Fig. 2. Optical schematic of a moiré interferometer.

The conventional moiré interferometry image is an interferogram, which carries the in-plane displacement information. Discrete displacements can be obtained by counting the fringe order (417 nm per fringe). Fig. 2 shows the optical system of a moiré interferometer.

The phase-shifting technique provides a high-resolution capability for determining the displacement field by precisely shifting the phase angle of the two coherent incident beams to the sample grating. In the interferogram, one fringe spacing corresponds to a phase angle difference of 2π , corresponding to 417 nm of displacement. Between two interference fringes, the phase angle varies continuously, so for two points within an interference spacing, their relative displacement cannot be determined explicitly from the interference pattern. However, such a displacement can be obtained if their phase angle difference is determined. Phase-shifting moiré interferometry extracts the unknown phase angle as a function of position in the interferogram from four precisely phase-shifted moiré interference patterns. Its principle can be explained by expressing the intensity of the four images as [7]

$$\begin{aligned}
 I_1(x, y) &= I_0(x, y) + I'(x, y) \cos[\phi(x, y)] \\
 I_2(x, y) &= I_0(x, y) + I'(x, y) \cos\left[\phi(x, y) + \frac{\pi}{2}\right] \\
 &= I_0(x, y) - I' \sin[\phi(x, y)] \\
 I_3(x, y) &= I_0(x, y) + I'(x, y) \cos[\phi(x, y) + \pi] \\
 &= I_0(x, y) - I' \cos[\phi(x, y)] \\
 I_4(x, y) &= I_0(x, y) + I'(x, y) \cos\left[\phi(x, y) + \frac{3\pi}{2}\right] \\
 &= I_0(x, y) + I' \sin[\phi(x, y)]
 \end{aligned} \tag{1}$$

where $I_0(x, y)$ and $I'(x, y)$ are the background and periodically varying intensities in the interference pattern and $\phi(x, y)$ is the unknown phase angle of the interference pattern at each pixel location (x, y) . Each subsequent pattern is obtained by consecutively shifting a phase angle of exactly $\pi/2$, or 1/4 of the fringe period. The unknown phase angle is then determined as

$$\phi = \arctan \frac{I_4 - I_2}{I_1 - I_3} \tag{2}$$

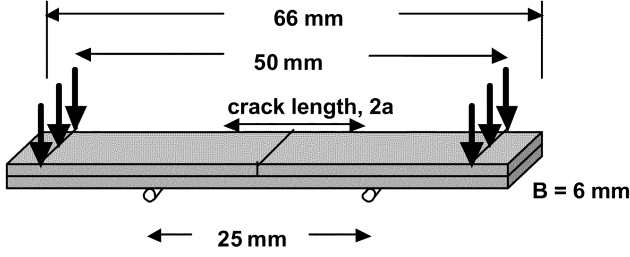


Fig. 3. Four-point bending geometry.

Once the phase angle is obtained, the continuous displacement can be determined; for example, the u field displacement can be expressed as

$$u = \frac{\phi}{4\pi f}. \quad (3)$$

The v field displacement has a similar relation as (3). The strains can then be evaluated accordingly:

$$\varepsilon_x = \frac{\partial u}{\partial x}, \varepsilon_y = \frac{\partial v}{\partial y}, \gamma_{xy} = \frac{\partial u}{\partial y} + \frac{\partial v}{\partial x}. \quad (4)$$

In operation, phase shifting is achieved by physically shifting the reference grating. Shifting the reference grating along the x -direction can phase shift the U field fringe pattern and shifting the reference grating along y -direction can phase shift the V field fringe pattern. To accomplish this, a high-precision piezoelectric transducer (PZT) is used to shift the reference grating.

III. EXPERIMENTAL MEASUREMENTS OF INTERFACIAL FRACTURE ENERGY FOR LOW-*k* INTERFACES

The interfacial fracture energy can be determined by measuring the critical energy release rate. One commonly used experimental technique for measuring the low- k interfaces is the four-point bending test [8], as schematically shown in Fig. 3. Compared with the silicon wafer, the dielectric layer is very thin, hence the sample structure responses can be assumed to be linearly elastic and the strain energy stored in the dielectric layer can be ignored [9]. Accordingly, the critical energy release rate G_C can be determined as

$$G_C = \frac{21(1-\nu^2)P_c^2 l^2}{16EB^2 h^3} \quad (5)$$

where E and ν are the Young's modulus and Poisson ratio of silicon, respectively, B is the sample width, h is the wafer thickness, P is the load, and l is the distance between the inner and outer loading points. P_c is the critical load when the crack propagates along the interface.

The four-point bending test can only measure the critical energy release rate at a fixed phase angle, or mode mixity. Since the critical energy release rate is a function of mode mixity, an instrument to measure interfacial adhesion energy under mixed mode loading was developed using the approach originally conceived by Fernlund and Spelt [10], [11]. This design utilizes a double cantilever beam (DCB) geometry, as illustrated in Fig. 4. The instrument allows interfacial fracture measurements for phase angles ranging from 0° (pure tension)

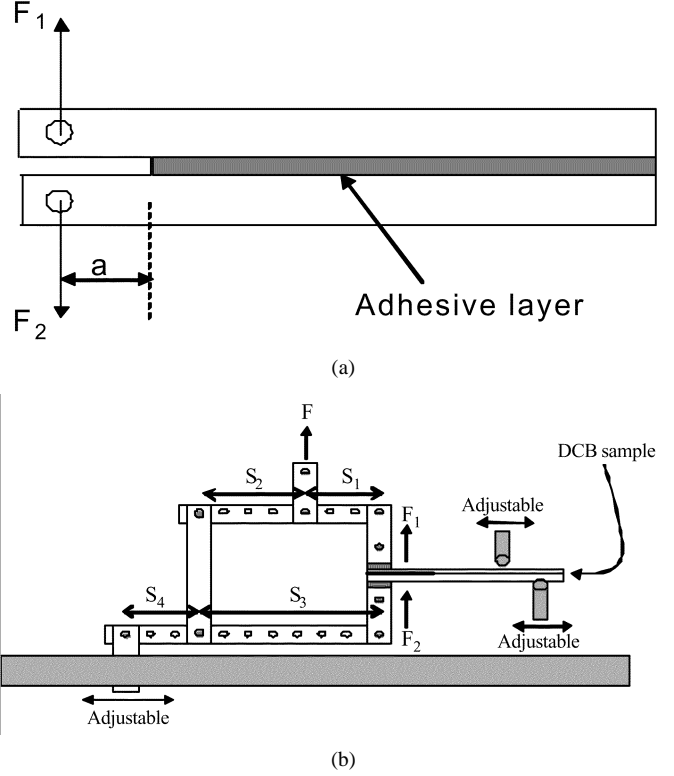


Fig. 4. Mixed-mode bending test. (a) Double cantilever beam geometry. (b) Mixed-mode loading fixture.

to 90° (pure shear). Additionally, multiple tests can be run on the same sample. The challenge of this technique resides in the crack length measurement, which is required for deducing the fracture energy for the DCB configuration. The energy release rate per unit crack length can then be defined as

$$G = \frac{(F_1 a)^2}{2D} \left[1 + \left(\frac{F_2}{F_1} \right)^2 - \frac{1}{8} \left(1 + \left(\frac{F_2}{F_1} \right)^2 \right) \right] \quad (6)$$

where the flexural rigidity per unit width D is given by

$$D = \frac{Eh^3}{12}. \quad (7)$$

The phase angle ψ varies as function of the ratio F_1/F_2

$$\psi = \arctan \left[\frac{\sqrt{3} \left(\frac{F_1}{F_2} + 1 \right)}{2 \left(\frac{F_1}{F_2} - 1 \right)} \right]. \quad (8)$$

IV. CHIP-PACKAGING INTERACTION (CPI)

Chip-packaging interaction has not been a serious problem for chips with SiO_2 interconnects. Unfortunately, this problem has become a major concern for packaging assembly of Cu/low- k chips. In a flip-chip package, the thermal deformation of the package can be directly coupled into the Cu/low- k interconnect structure inducing large local deformation to drive interfacial crack formation. For standalone wafer structures, FEA is commonly used to study thermal stresses in multilevel interconnect structures. To apply FEA to evaluate the packaging effect on thermal deformation of the interconnect structure,

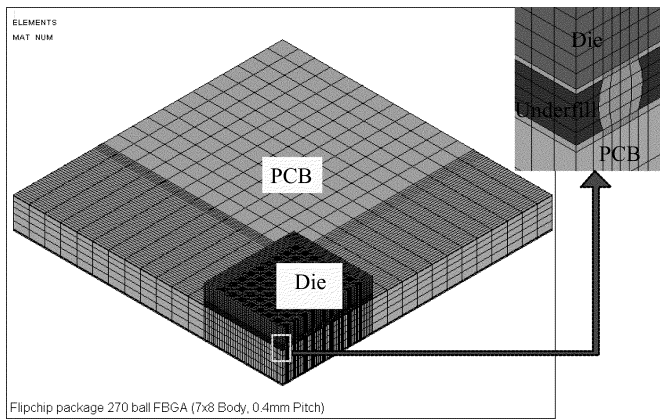


Fig. 5. Package level model.

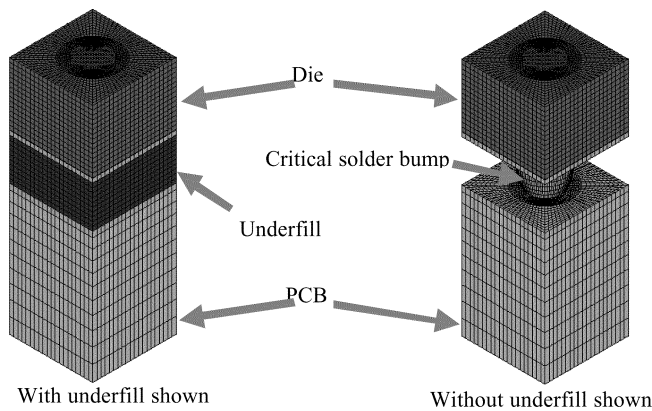


Fig. 6. Critical solder region model.

there is a basic difficulty due to the large difference in the dimension of the packaging and interconnect structures. For this reason, researchers from Motorola first introduced a multilevel submodeling technique to evaluate the energy release rate for interfaces in the interconnect structure after being assembled into a flip-chip package [12], [13]. This technique bridged the gap between the packaging and wafer levels. Energy release rates for various interconnect interfaces during packaging assembly were calculated using 2-D FEA models. However, a flip-chip package is a complicated 3-D structure that cannot be properly represented using a 2-D model. We developed, therefore, a 3-D FEA based on a four-level submodeling technique to investigate the packaging effect on interconnect reliability, particularly focusing on the Cu/low- k chips in comparison to Al and Cu/oxide chips.

A. Multilevel subModeling Technique

Level 1: Starting from the package level, thermal deformation for a whole flip-chip package was investigated first using 3-D FEA. At this package level, a quarter section of the package was modeled using the symmetry shown in Fig. 5. No interconnect structure detail was considered at this time because its thickness is too small compared with the whole package. Simulation results for this whole package level model were verified with experimental results obtained from moiré interferometry.

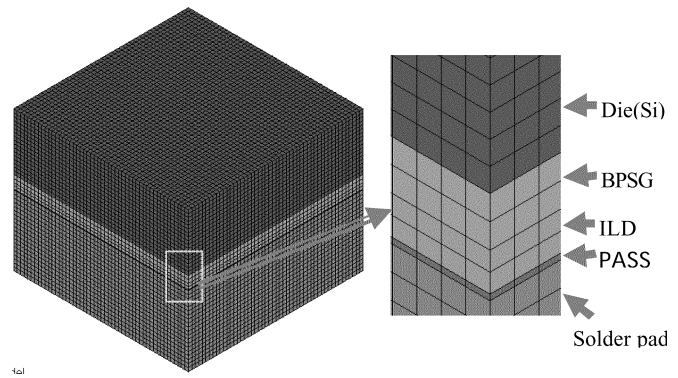


Fig. 7. Die-solder interface level model.

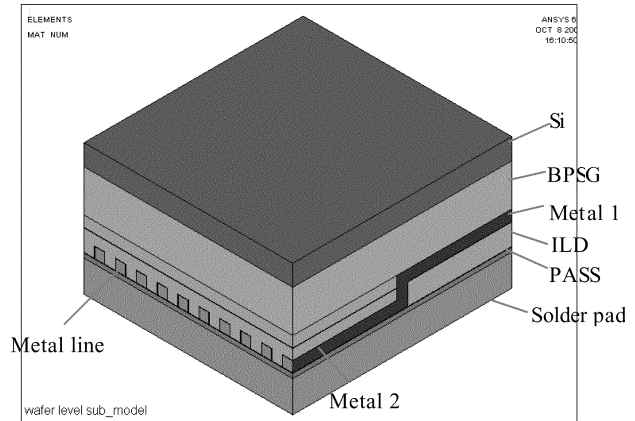


Fig. 8. Detailed wafer level interconnect structure model.

Level 2: From the simulation results for the package level modeling, the most critical solder bump was identified. A sub-model of the package level model (Level 1) focusing on the critical solder bump region with much finer meshes was developed as shown in Fig. 6. The built-in cut boundary technique in ANSYS [14] was used for submodeling. At this submodel level, a uniform ILD layer at the die surface was considered but still no detailed structure was considered in this submodel.

Level 3: Based on the Level 2 modeling results, a large peeling stress was found at the die-solder interface. At the critical die-solder interface region with the highest peeling stress, a submodel based on a Level 2 model was created using the cut boundary technique, as shown in Fig. 7. This submodel focused on the die-solder interface region (a small region of Level 2) containing a portion of the die, the ILD layer and a portion of the solder bump. Still only a uniform ILD layer at the die surface was considered at this level and no detailed interconnect structure was included.

Level 4: This submodel zoomed in further from the Level 3 model focusing on the die-solder interface region as shown in Fig. 8. Finally, a detailed interconnect structure was included. Ten lines were found to be sufficient to approximate the interconnect structure. The submodel was set up accordingly and at the center line a crack with a fixed length was introduced along several interfaces of interest. Energy release rate and mode mixity for each crack were determined using a modified virtual crack closure technique as discussed in the next section.

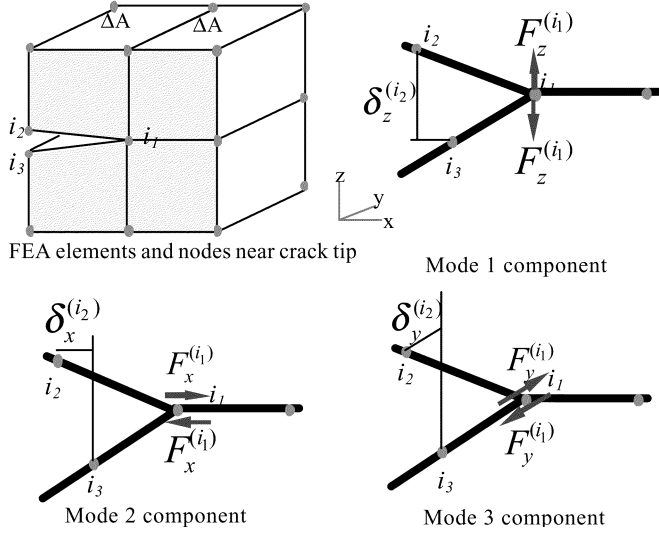


Fig. 9. Modified virtual crack closure technique.

B. Modified Virtual Crack Closure (MVCC) Technique

An MVCC technique was used to calculate the energy release rate [15]. Since the critical energy release rate is a function of mode mixity, the components of the energy release rate corresponding to the three basic fracture modes 1, 2, and 3 (Fig. 9) were separately determined. In our study, with the local stress and strain distributions obtained by modeling, the mode mixity for various interfaces can be properly defined and the critical energy release rate calculated accordingly.

For the eight-node solid elements shown in Fig. 9, the three energy release rate components G_I , G_{II} , and G_{III} can be obtained as

$$\begin{aligned} G_I &= \frac{\sum_i F_z^{(i_1)} \delta_z^{(i_2)}}{(2\Delta A)} \\ G_{II} &= \frac{\sum_i F_x^{(i_1)} \delta_x^{(i_2)}}{(2\Delta A)} \\ G_{III} &= \frac{\sum_i F_y^{(i_1)} \delta_y^{(i_2)}}{(2\Delta A)} \end{aligned} \quad (9)$$

where $F_x^{(i_1)}$, $F_y^{(i_1)}$, and $F_z^{(i_1)}$ are nodal forces at node i_1 along the x , y , and z directions, respectively. $\delta_x^{(i_2)}$, $\delta_y^{(i_2)}$, and $\delta_z^{(i_2)}$ are relative displacements between node i_2 and i_3 along the x , y , and z directions, respectively. Note that for simplicity only one element set is shown along crack front direction (y direction).

Once G_I , G_{II} , and G_{III} are determined, the phase angles may be expressed as

$$\begin{aligned} \psi &= \tan^{-1} \left[\left(\frac{G_{II}}{G_I} \right)^{1/2} \right] \\ \varphi &= \tan^{-1} \left[\left(\frac{G_{III}}{G_I} \right)^{1/2} \right]. \end{aligned} \quad (10)$$

In the FEA, the ratio of G_I , G_{II} , or G_{III} over the total $G(G_I + G_{II} + G_{III})$ may change due to changing the element size

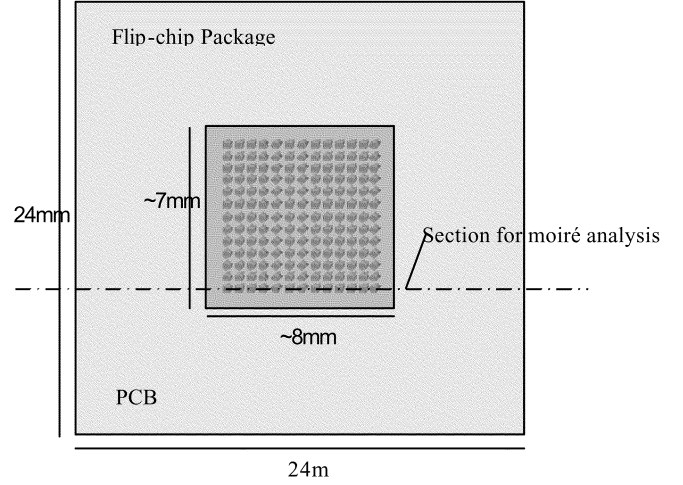


Fig. 10. Schematic of an experimental flip-chip package.

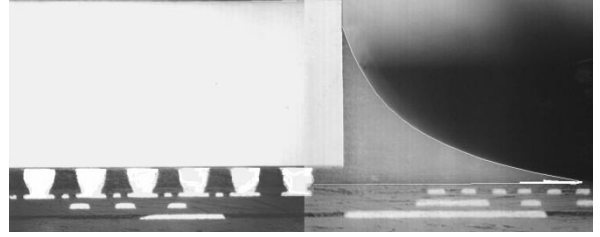


Fig. 11. Microscope picture for the cross-section of interest.

around the crack tip, especially when the element size is very small. In our simulation, the element size is relative large, hence the ratio of G_I , G_{II} , or G_{III} over the total G is insensitive to the element size.

The general interface fracture criterion can be expressed as

$$\left(\frac{G_I}{G_{IC}} \right)^l + \left(\frac{G_{II}}{G_{IIC}} \right)^m + \left(\frac{G_{III}}{G_{IIIC}} \right)^n = 1 \quad (11)$$

where G_{IC} , G_{IIC} , and G_{IIIC} are critical energy release rates for pure mode 1, 2, and 3, respectively, and l , m , and n are constants.

V. RESULTS AND DISCUSSIONS

A. Thermal Deformation of Flip-Chip Package

Moiré analysis was carried out for an experimental flip-chip package. The package was first sectioned and polished to the cross-section of interest. A schematic of the experimental flip-chip package with the cross-section that was analyzed is shown in Fig. 10.

Optical microscope pictures were taken for this cross-section. A very thin layer of epoxy adhesive (less than $5 \mu\text{m}$) was used to adhere a 1200 lines/mm grating on the cross-section of the specimen at 102°C . The deformation at this temperature was taken as a reference (zero) deformation state. The moiré experiment was performed at room temperature (22°C), hence providing a thermal loading of -80°C . A microscope picture for the right corner of the cross-section is shown in Fig. 11.

An IBM PEMI modified to incorporate the phase shift capability as shown in Fig. 12 was used for moiré analysis. The

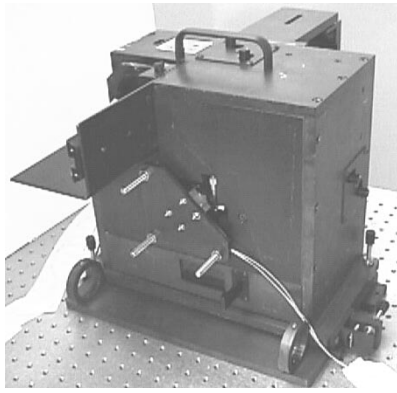
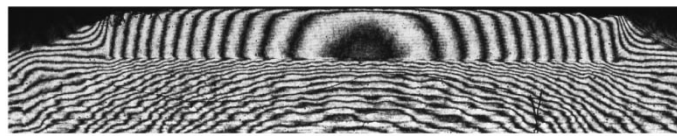


Fig. 12. Phase-shift PEMI with PZT modification mount on the back plate.



(a) U field



(b) V field

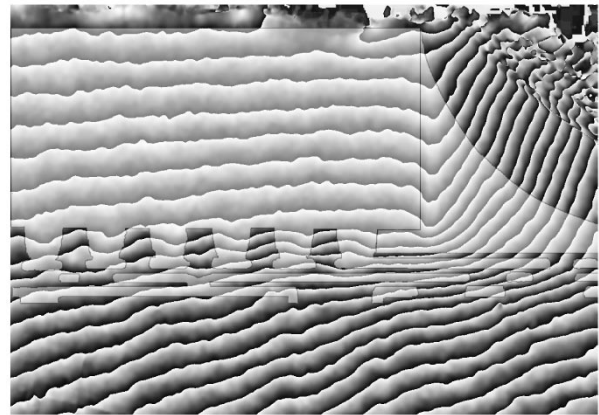
Fig. 13. Conventional moiré interferometry fringe patterns.

PEMI system was aligned using an undeformed 1200 lines/mm grating, which was used to apply the sample grating. Then the package with the deformed grating (due to the -80°C thermal load) on the cross-section surface was put into the system to capture the moiré images. Phase shift was performed by shifting the reference grating within the interferometer using a high-precision PZT. The reference grating was physically shifted 147, 295, and 441 nm relative to the I_1 image in order to generate the I_2 , I_3 , and I_4 images. Images were captured using a Photometrics 1.3 megapixel CCD camera with 12-bit grayscale sensitivity (4096 grayscales).

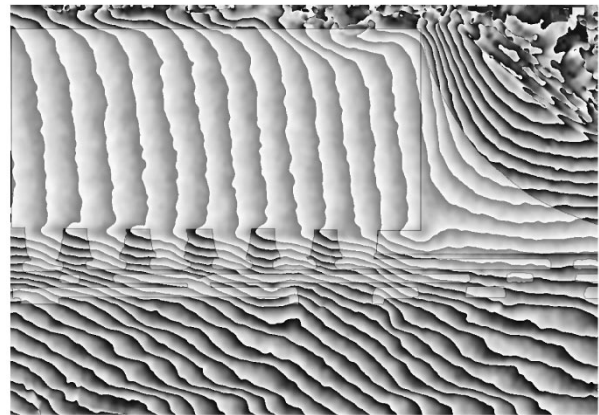
A moiré analysis software developed in our laboratory was used to calculate the phase map, displacement, and strain distributions. Two-dimensional displacement and strain distribution can be obtained throughout the area of interest.

The cross-sectional fringe patterns obtained by standard moiré analysis are shown in Fig. 13. A number of qualitative observations can be made from these fringe patterns.

- The U and V displacement fields show a global bending deformation of the package.
- The U field displays a relatively smooth horizontal (x) displacement distribution. This demonstrates that the underfill indeed reduces the thermal mismatch between the die and the substrate, hence protecting the solder bumps.
- The V field displays high density fringes in the solder bump-underfill layer, which is due to the high CTE of this layer.



(a) U field



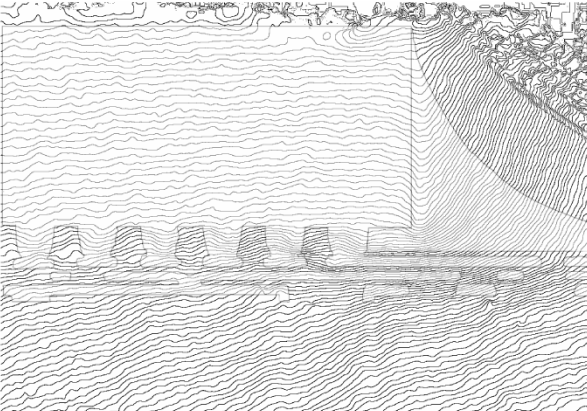
(b) V field

Fig. 14. Phase maps.

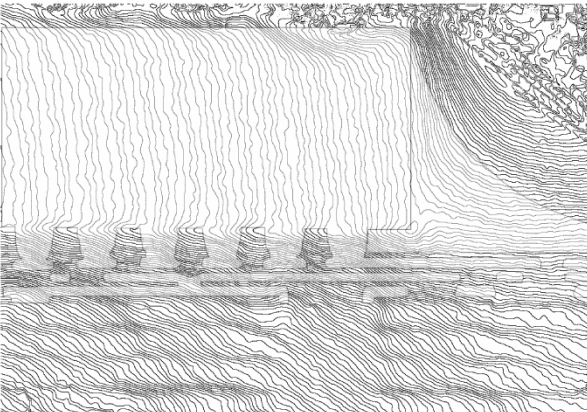
- The right-bottom and left-bottom die corner areas have the highest shear strains, which can be seen from the large displacement gradients along the vertical (y) direction in the U field.
- The most critical area appears to be at the fillet near the bottom die corner. In this region, the strains are close to zero, indicating large thermal stresses in this region because the total strain obtained from moiré fringes is the sum of thermal strain and stress-induced strain. This is expected since the thermal mismatch and mechanical property mismatch between these two materials usually produce singular stresses at a bimaterial apex [16], [17].

In the standard U and V moiré images shown in Fig. 13, only a few fringes can be observed in a solder bump. Since the fringes appear to be fuzzy and not well defined, it is difficult to extract accurate displacement data from these images. The U and V field phase contour maps generated from the phase-shifting moiré interferometer are shown in Fig. 14. An outline of the interfaces obtained from the optical micrograph picture is superimposed onto the phase contour for clarity. In comparison, the phase contours, as shown in Fig. 14 and separated by a fringe spacing of 208 nm, provide better defined displacement contours for the package.

The resolution can be further enhanced using phase contour maps corresponding to smaller phase separations. An example



(a) U field



(b) V field

Fig. 15. Displacement contour maps showing 52-nm displacement per contour.

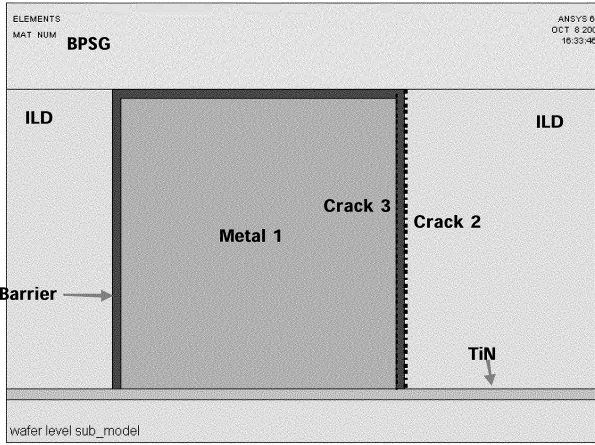
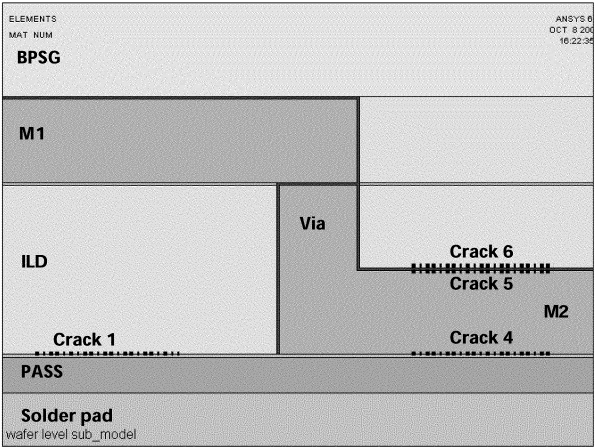


Fig. 17. Cracking along interfaces of interest.

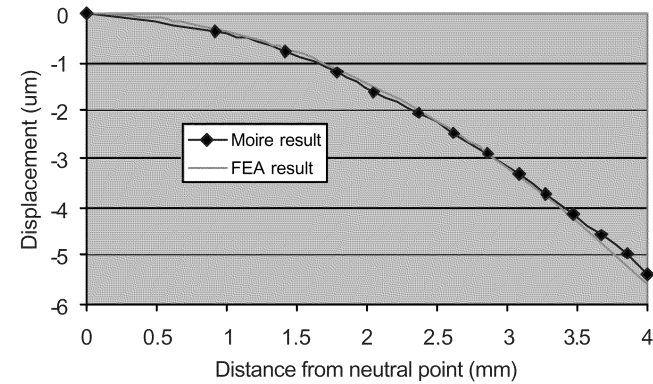


Fig. 16. Comparison of FEA and moiré results.

corresponding to a fringe spacing of 52 nm is shown in Fig. 15. The images with a fringe spacing of 26 nm are not shown here since the fringes are too dense to plot clearly. More results can be found in [18].

The FEA result for the package level modeling was first compared with moiré experimental results. Since the thermal load used in the moiré measurement was from 102 °C to 22 °C, we applied the same thermal load (102 °C to 22 °C) in the package level modeling in order to compare the moiré and FEA results. Detailed moiré results can be found in [10]. Fig. 16 shows the

TABLE I
MECHANICAL PROPERTIES

Material	E (GPa)	v	α (ppm/°C)
Al	72	0.36	24.0
Cu	122	0.35	17.0
TEOS	66	0.18	0.57
SiLK	2.45	0.35	66.0

z-displacement corresponding to the package warpage distribution along the die center line (see Fig. 10). The FEA and moiré results are in very good agreement.

After verification with moiré interferometry, FEA was applied to investigate standalone wafer structures as well as the packaging effect. Both Al and Cu interconnect structure with TEOS and SiLK as ILD were investigated. Cracks with a fixed length were introduced at six interfaces to evaluate the crack driving forces as shown in Fig. 17. Those four horizontal and two vertical interfaces were chosen since they are probably most susceptible to delamination during packaging assembly. Typical material properties used in our simulation are listed in Table I. For standalone wafer structures, thermal loading is set from wafer process temperature (400 °C) to room temperature (25 °C). When considering the packaging effect, thermal loading was set from −55 °C to 125 °C.

B. Crack Driving Force for Standalone Wafer Structures

Fig. 18 shows the energy release rates for cracking along the six interfaces illustrated in Fig. 17. For Al/TEOS and Cu/TEOS structures, the energy release rates are very small, less than 1 J/m^2 , for all of the interfaces. The Cu/SiLK structure has much higher energy release rates reaching 1.16 J/m^2 along SiLK/barrier and Cu/barrier interfaces. The mode mixities for interfaces in Cu/SiLK structure are also shown in Table II. In the Cu/SiLK structure, crack 2 along the SiLK/barrier side wall and crack 3 along the barrier/Cu interfaces have high energy release rates exceeding 1 J/m^2 . The fracture mode for these two cracks becomes almost pure mode 1. These two interfaces can be the most critical ones during wafer processing. However, compared with critical energy release rates for low- k interfaces obtained from experiments (larger than $4\text{--}5 \text{ J/m}^2$), these values are considerably lower, hence critical crack formation in Cu/low- k interconnect structures during wafer processing is not expected to be a serious problem although the result does not rule out the possibility of delamination due to subcritical crack growth.

C. Packaging Effect

The four-step multilevel submodeling was conducted to calculate the energy release rate for interconnect level cracking in order to evaluate the packaging effect. We assumed a stress-free state at -55°C for the whole package and the crack driving force was obtained at 125°C . Fig. 19 gives the energy release rates for the six interfaces as described in Fig. 17 in the Al/TEOS, Cu/TEOS and Cu/SiLK interconnect structures. The results show that the packaging effect on the energy release rate is generally very low for Al/TEOS and Cu/TEOS structures so that the impact of packaging on interconnect reliabilities can be ignored for the oxide interconnect structures.

The results showed in Fig. 19 indicate a significant packaging effect for the Cu/SiLK structure. The interfacial crack driving force can be as high as 16 J/m^2 therefore interfacial delamination can be a serious reliability problem for Cu/SiLK structures. From Fig. 11 we see that interfaces parallel to the die surface (Crack 1, 4, 5 and 6) are more prone to delamination due to the packaging effect while vertical interfaces 2 and 3 show little effect. The mode mixities driving interfacial crack formation for Cu/SiLK structure are summarized in Table III. For the Cu/SiLK structure, the cracks along the 1, 5, and 6 interfaces are very close to a pure mode 1. But for the Cu/PASS interface, both mode 1 and 3 components are present. To evaluate the possibility of crack propagation along those interfaces, the critical energy release rates have to be determined as a function of mode mixity. Such data can be obtained by variable mode-mixity bending beam test.

D. Scaling Effect

Finally, we investigated the packaging affect on interconnect reliability due to continuing scaling of the interconnect line width. Calculations were carried out for the ILD/PASS interface in the Cu/SiLK structure with line width decreasing from 0.5 to $0.1 \mu\text{m}$. The normalized energy release rates obtained are shown in Fig. 20. Overall, for the standalone wafer structure,

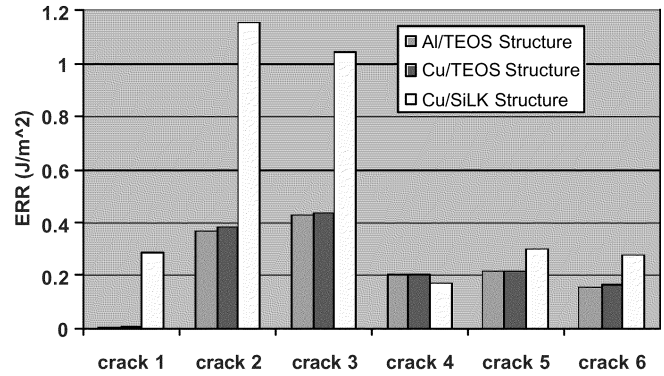


Fig. 18. Energy release rates for standalone wafer structures (from 400°C to 25°C).

TABLE II
MIXITY FOR STANDALONE CU/SiLK STRUCTURES

	Crack 1	Crack 2	Crack 3	Crack 4	Crack 5	Crack 6
G_I/G	0.80	0.99	0.98	0.07	0.92	0.99
G_{II}/G	0.20	0.00	0.01	0.84	0.06	0.01
G_{III}/G	0.00	0.01	0.01	0.09	0.02	0.00
$G(\text{J/m}^2)$	0.2908	1.1556	1.0476	0.1718	0.3022	0.2811

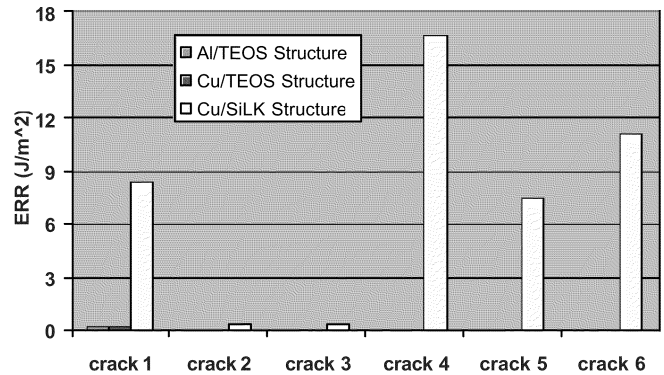


Fig. 19. Energy release rates when considering packaging effect.

TABLE III
MODE MIXITY FOR CU/SiLK STRUCTURE CONSIDERING PACKAGING EFFECT

	Crack 1	Crack 2	Crack 3	Crack 4	Crack 5	Crack 6
G_I/G	0.98	0.56	0.71	0.77	0.95	0.94
G_{II}/G	0.01	0.03	0.02	0.23	0.04	0.05
G_{III}/G	0.01	0.41	0.27	0.00	0.01	0.01
$G(\text{J/m}^2)$	8.34	0.40	0.36	16.71	7.52	11.11

the driving force for interface delamination increased with decreasing line width although its value is still too low to be of concern. It is interesting that the driving force for interfacial delamination does not change much with line width scaling. The implication of this result will be investigated.

VI. CONCLUSION

We have summarized experimental and modeling results from studies performed in our laboratory to investigate the

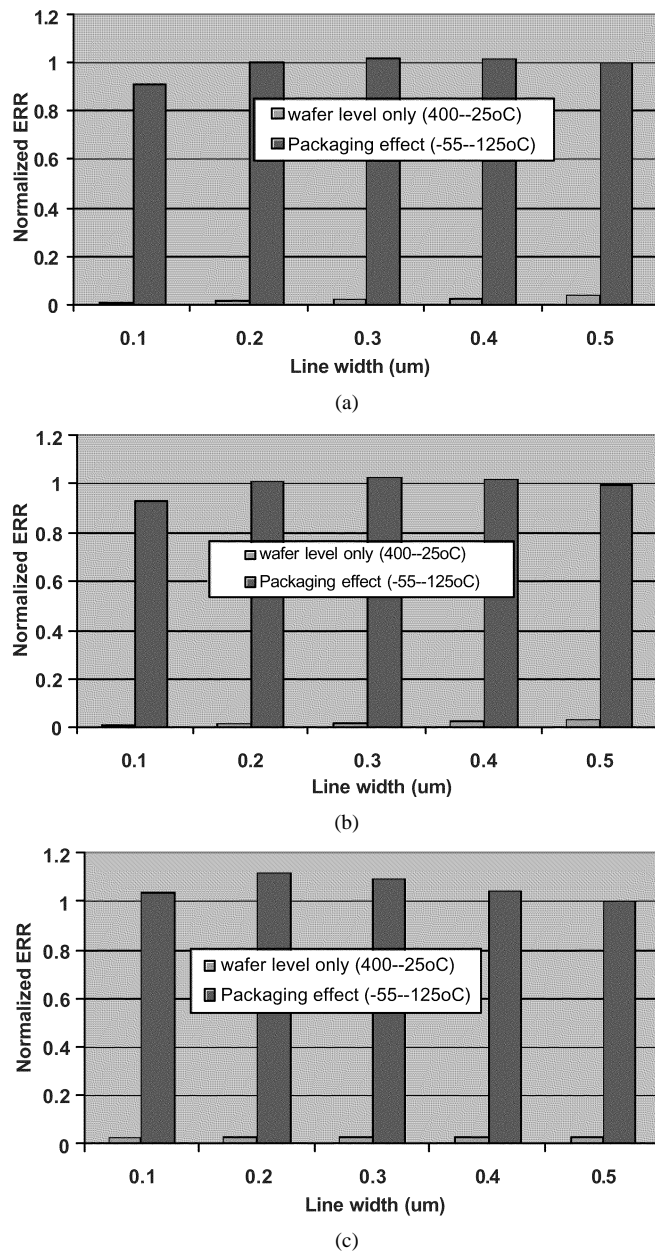


Fig. 20. Scaling effect. (a) Al/TEOS structure, TEOS/PASS interface. (b) Cu/TEOS structure, TEOS/PASS interface. (c) Cu/SiLK structure, SiLK/PASS interface.

chip-package interaction and its impact on low-*k* interconnect reliability. We first reviewed the application of high-resolution moiré interferometry to measure thermal deformation in a flip-chip package. Then results from 3-D FEA based on a multilevel submodeling approach in combination with high-resolution moiré interferometry to investigate the chip-package interaction for low-*k* interconnects were discussed. Packaging-induced crack driving forces for relevant interfaces in Cu/low-*k* structures were deduced and compared with corresponding interfaces in Cu/TEOS and Al/TEOS structures to assess the effect of ILD on packaging reliability. For a standalone chip, the energy release rate driving interfacial delamination during wafer processing was found to be low

compared with the critical energy release rate for interfacial delamination obtained from the four-point bend test. After the die is assembled into a flip-chip package, thermal deformation at the package level can be directly coupled into the interconnect structure, increasing significantly the driving force for interfacial delamination and can seriously impact the chip reliability, especially for Cu/low-*k* structures. Interfaces in the interconnect structures parallel to the die surface are more prone to the packaging effect. Finally, the packaging effect was investigated as a function of line width and the energy release rate does not seem to change with decreasing line width.

REFERENCES

- [1] Y. Tsukada, Y. Mashimoto, T. Nishio, and N. Mii, "Reliability and stress analysis of encapsulated flip chip joint on epoxy based printed circuit board," in *Proc. Advances in Electronic Packaging, Joint ASME/JSME Conf. Electronic Packaging*, vol. EEP-1-2, Milpitas, CA, Apr. 1992, pp. 827-835.
- [2] Y. Du, "Thermomechanical stress studies for advanced copper metallization and integration," Ph.D. dissertation, Univ. of Texas, Austin, 2001.
- [3] D. Post, B. Han, and P. Ifju, *High Sensitivity Moiré: Experimental Analysis for Mechanics and Materials*. New York: Springer-Verlag, 1994.
- [4] G. Wang, P. Ho, T. Hayden, E. Pyun, and D. Gundel. (2001, Apr.) Solder joint stress in a cavity-up flex-based BGA. *Chip Scale Rev., Tech. Forum* [Online]. Available: http://www.chipscalereview.com/issues/0401/tech-Forum02_01.html
- [5] X. Dai and P. S. Ho, "Thermo-mechanical deformation of underfilled flip-chip packaging," in *Proc. 21st IEEE/CPM Int. Electronics Manufacturing Technology Symp.*, 1997, pp. 326-333.
- [6] Y. Guo, C. K. Lim, W. T. Chen, and C. G. Woychik, "Solder ball connect (SBC) assemblies under thermal loading: I. deformation measurement via moiré interferometry, and its interpretation," *IBM J. Res. Develop.*, vol. 37, pp. 635-648, 1993.
- [7] M. R. Miller, I. Mohammed, X. Dai, N. Jiang, and P. S. Ho, "Analysis of flip-chip packages using high resolution moiré interferometry," in *Proc. 49th IEEE Electronic Components and Technology Conf.*, 1999, pp. 979-986.
- [8] P. G. Charalambides, J. Lund, A. G. Evans, and R. M. McMeeking, *J. Appl. Mech.*, vol. 56, pp. 77-82, 1989.
- [9] Z. Suo and J. W. Hutchinson, "Sandwich test specimens for measuring interface crack toughness," *Mater. Sci. Eng.*, vol. A107, pp. 135-143, 1989.
- [10] G. Fernlund and J. K. Spelt, "Mixed-mode fracture characterisation of adhesive joints," in *Composites Sci. Technol.*, 1994, vol. 50, pp. 441-449.
- [11] J. W. Wylde and J. K. Spelt, "Measurement of adhesive joint fracture properties as a function of environmental degradation," *Int. J. Adhesion Adhesives*, vol. 18, pp. 237-246, 1998.
- [12] L. Mercado, C. Goldberg, and S. Kuo, "A simulation method for predicting packaging mechanical reliability with low-*k* dielectrics," in *Proc. Int. Interconnect Technology Conf.*, 2002.
- [13] L. Mercado, C. Goldberg, S. Kuo, T. Lee, and S. Pozder, "Analysis of flip-chip packaging challenges on copper low-*k* interconnects," in *Proc. 53th IEEE Electronic Components and Technology Conf.*, 2003, pp. 1784-1790.
- [14] *ANSYS Manual*, ANSYS, Inc., Canonsburg, PA, 2003. [Online.] Available: <http://www.ansys.com>.
- [15] F. G. Bucholz, R. Sistla, and T. Krishnamurthy, "2D and 3D applications of the improved and generalized modified crack closure integral method," in *Computational Mechanics '88*, S. N. Atluri and G. Yagawa, Eds. New York: Springer Verlag, 1988.
- [16] J. C. W. van Vroonhoven, "Effects of adhesion and delamination on stress singularities in plastic-packaged integrated circuits," *Trans. ASME: J. Electron. Packag.*, vol. 115, pp. 28-33, 1993.
- [17] P. S. Theocaris, "The order of singularity at a multi-wedge corner of a composite plate," *Int. J. Eng. Sci.*, vol. 12, pp. 107-120, 1974.
- [18] G. Wang, J.-H. Zhao, M. Ding, and P. Ho, "Thermal deformation analysis on flip-chip packages using high resolution moiré interferometry," in *Proc. Itherm*, 2002, pp. 869-875.

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