EE314 Digital Electronics Laboratory
Term Projects
Spring 2004

Each project will be carried out by a group of two students. This term there are 5 different project options. The difficulties of these projects are different. However, the difficulty of the projects **will not** affect your grade.

Within the project you are required to submit following:

1. Design (paper-pencil work, to be included in the final report)
2. Design entry in XILINX software
3. Detailed simulations for design verification in XILINX, and implementation.
4. Project demonstration
5. Final report

While doing your design follow hierarchical design method. You may use only AND, OR, NAND, NOR, XOR, XNOR, INV, IBUF, and OBUF. You can use any-input-gates and the ones with complemented inputs. Examples are NAND5B3, XNOR7, INV, IBUF8, etc. Any other components (like full-adders, flip-flops, multiplexers, etc) should be built hierarchically.

The design entry and simulations should be completed using the XILIX installed in the Student Computer Laboratory. Each team should take the printouts of all the building block schematics, and their pad report (after the implementation). Also make sure that you have archived the project into floppy disks and bring them to the laboratory.

Both team members must attend the demonstration. In case there is a problem with your project you will be allowed to modify it during the lab session. However, since you will have limited time, make sure that your design is fully functional and the implementation does not contain any errors.

PROJECT DEFINITIONS

1. DISPLAY CONTROLLER FOR AN AIR CONDITIONING SYSTEM

Design a combinational circuit to control the display of an air conditioning system. The display controller has three inputs: Current temperature (CT), desired temperature(DT), display mode (DT). CT and DT inputs are 1 digit BCD numbers showing the current temperature level of the room and the desired temperature level that the user has entered respectively (Both are scaled to the range 0-9). The display mode toggles the display between Operation Mode and Fan Speed Modes. In the Operation Mode the seven-segment display shows whether the system is in Cool, Heat or Off states (See Table 1 for details). In the Fan Speed Mode the display shows the fan speed which is the absolute value of the difference between current and desired temperature levels. If either CT or DT is an invalid BCD number then the seven segment displays 'E' corresponding to an error state. Figure 1 shows the circuit diagram.

Table 1: Display specification in Operation Mode

Condition	Mode	Display
CT > DT	Cool	'C'
CT = DT	Off	'O'
CT < DT	Heat	'H'

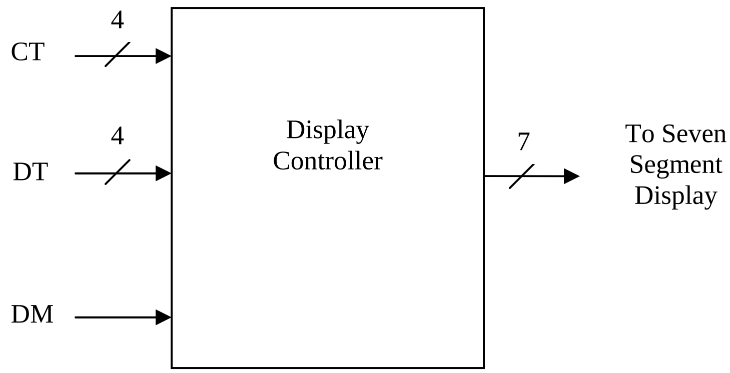

Figure 1: The Display Controller and its input/output pins.

2. DIGITAL CLOCK

In this project, you will design a digital clock that shows the hour and the minute in HH:MM format and which can set to the desired time. One configuration for this project may be as follows:

> Second, minute and hour parts will be implemented by counters. When 1 second passes, the *second counter* will increase by one. When the *second counter* is 60, it will reset with the next second and give an "increment" signal to *minute counter*. Same is also true for minute and hour counters. So, you need a "1 second" clock here. This might be done by directly taking a clock signal with 1 second period from outside, or taking a faster clock and dividing it by required value in order to generate a 1 second period clock.

Since the Xilinx boxes we are using has only one 7-segment display, you will multiplex this display by showing one digit at a time. In other words, when a DISPLAY signal is taken, it will display the 2^{nd} digit of hour, 1^{st} digit of hour, 2^{nd} digit of minute and 1^{st} digit of minute in order with a sufficient time between the digits (for example 1 second). Notice that, in order to test the circuitry better, an additional property might be added in order to show the *second* also, otherwise testing the circuit will be rather difficult.

Do not forget that, this is an exciting and challenging project and will probably take longer time compared to the other projects.

3. ELEVATOR CONTROLLER

You are expected to design an elevator controller for a building of 4-floors. The specifications in this project title will not be defined strictly, so you can do assumptions if it increases the functionality or simplifies the circuit. Here are the important points:

- There are 4 floors, and there will be 2 buttons on each floor, one is for going upstairs, and one is for going downstairs.
- The elevator will stop on the floors, where the floor calling the elevator is on the way of the elevator.
- The elevator will wait on a floor until the door of the elevator is opened and closed, or a certain amount of time passes
- If the elevator is called from a floor, and it is not on the way of the elevator, it should remember this floor, and go to that floor as soon as possible.

You may for example display the current floor on the 7-segment display and use the switches on the box as the buttons on each floor. You should also take into account the time required for the elevator to travel between the floors.

4. TEMPERATURE SENSOR

You will design a temperature sensor and display the result. Unlike the project given last semester for analog design, you are not allowed to use an all-in-one chip. You will use a single sensor in order to acquire the temperature information. Then with an A/D converter you will convert the measurement. The display is either in Celsius or in Fahrenheit or in Kelvin. You will work with the bare FPGA board. As there is a limited number of boards only a limited number of groups can choose this project.

5. FIR FILTER (PARALLEL OPERATION)

Finite impulse response (FIR) filters are used in a number of digital signal processing applications due to a number of their advantageous [3]. They are composed of a number of registers, where current and past values of the input are stored. The contents of these registers are multiplied by some coefficients and the result is stored in an output register. Depending on the coefficients used many different filtering characteristics can be obtained. The size of the hardware depends both on the input wordlength and the number of coefficients and hence memory units. The number of the memory units used in the circuit is known as the order of the filter. For example, if a FIR filter uses only current and previous input values, it is a 1^{st} order filter since it only requires a single memory location to hold the 1 past value at a time. Similarly, if a FIR filter calculates the average of 5 samples including the current value, its order will be 4, since it would require only 4 memory units to hold up to 4 past values.

The output wordlength may also be larger than the input wordlength. For example, if you add current value to the one previous value and store the result in a register, the output should be 1-bit larger as compared to the input, since the maximum gain can be two, which corresponds to 1-bit only.

In this project, you will design and implement a 3rd order FIR filter. The filter will perform the following operation:

$$y(n) = 1*x(n) - 0.5*x(n-1) + 0.25*x(n-2) - 0.75*x(n-3)$$

In the above equation y(n) is the output and x(n) is the input. The current and previous values of the x are denoted by the index terms in the parentheses.

In this design you will design and implement an 8-bit FIR filter. Assume that the input is in 2's complement form. For this circuit, since there will be 4 simultaneous additions (all the coefficients are less than or equal to 1), it will be sufficient if you just use a 10-bit register to store the output values.

You can either use parallel or serial architecture. Note that parallel architecture will be simple, but it will require large adders. On the other hand serial architecture will be small in size, but it requires a more challenging design [4]. Designing the circuit using a bit-serial architecture will be awarded with some bonus.

References

[1] Contemporary Logic Design, Randy H. Katz
[2] Digital Design, M. Mano
[3] Discrete Time Signal Processing, A. Openheim
[4] Selim Eminoğlu, "Analog-Digital Mixed-Signal VLSI Modules for Audio Band Signal Processing Applications," MS Thesis, METU, September 1998.