# Deformation and Failure of Multi-Layered Under-Bump-Metallurgy in Flip-Chips

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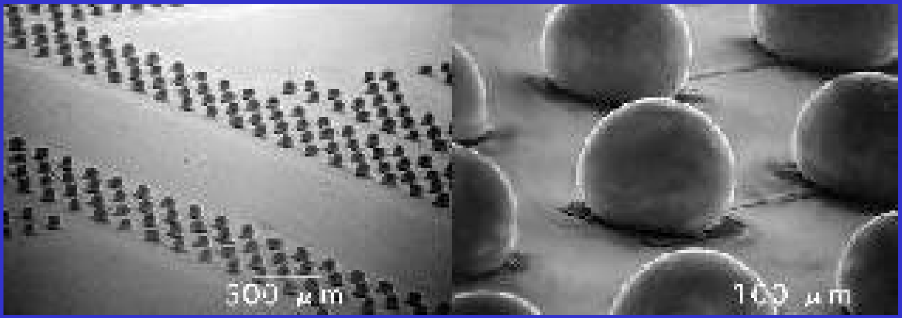
## OBJECTIVES:

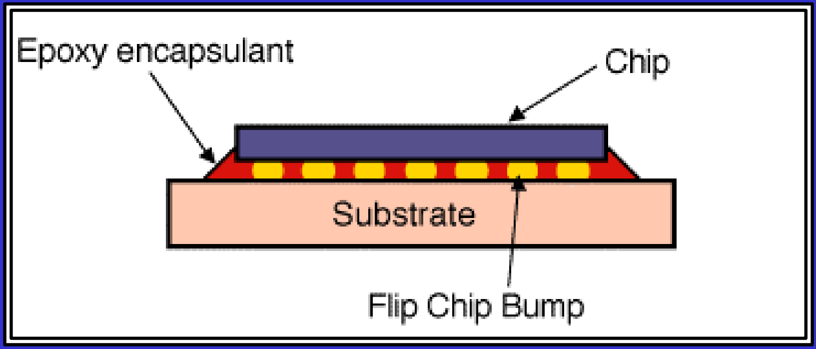
Identify potential fracture modes and likely delamination sites at or near under bump metallurgy (UBM) and solder bumps within flip chip packages using detailed models

## KEY-POINTS:

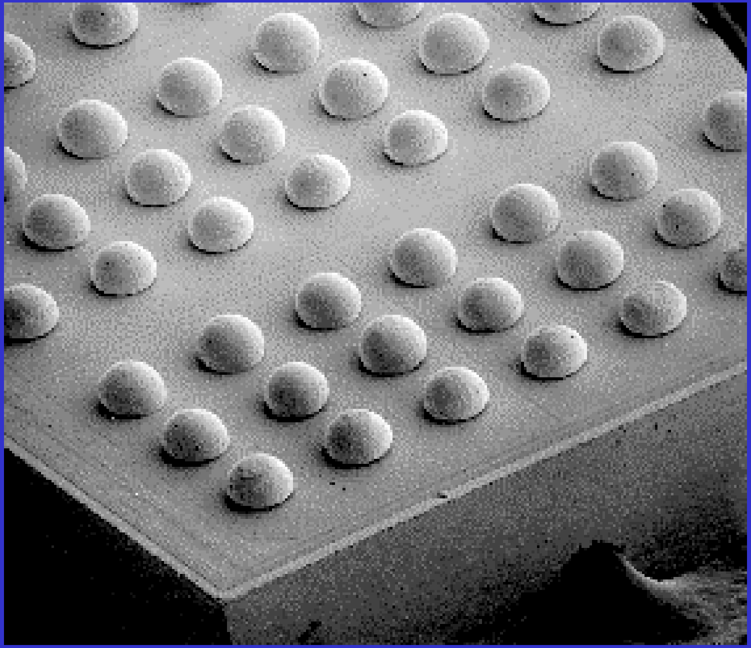
- Apply multi-scale finite element models (MS-FEM) to flip-chip package analysis
- Model sub-μm thick multi-layers of UBM.
- Study stress concentration and delamination under temperature change.
- Compute mixed mode fracture parameters along interface cracks



### Flip Chip



### Solder Bumps (~100μm dia)



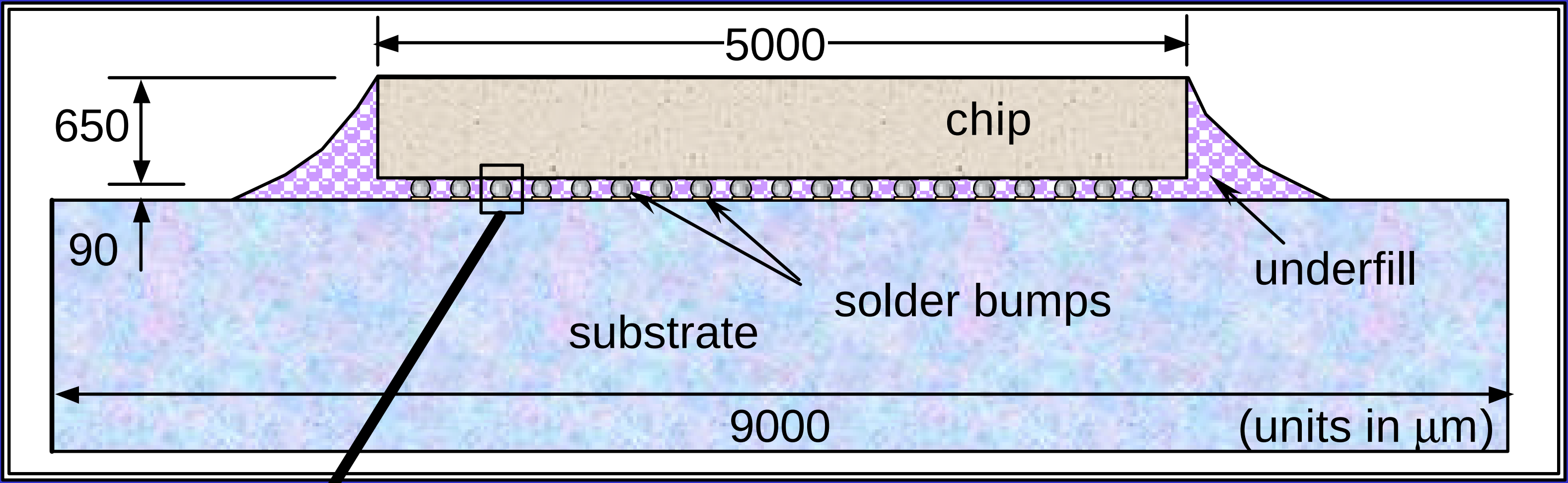
# OUTLINE

1. Modeling
    - Structures of UBM and Solder Bumps in Flip-Chip Package
    - Key Structural and Material Features Technique
    - Multi-Scale Finite Element Analysis
2. Stress Analysis from Finite Element Calculations
    - Global Model
    - Local Cell Model
3. Delamination Analysis
    - Short Cracks
    - Long Cracks
4. Summary

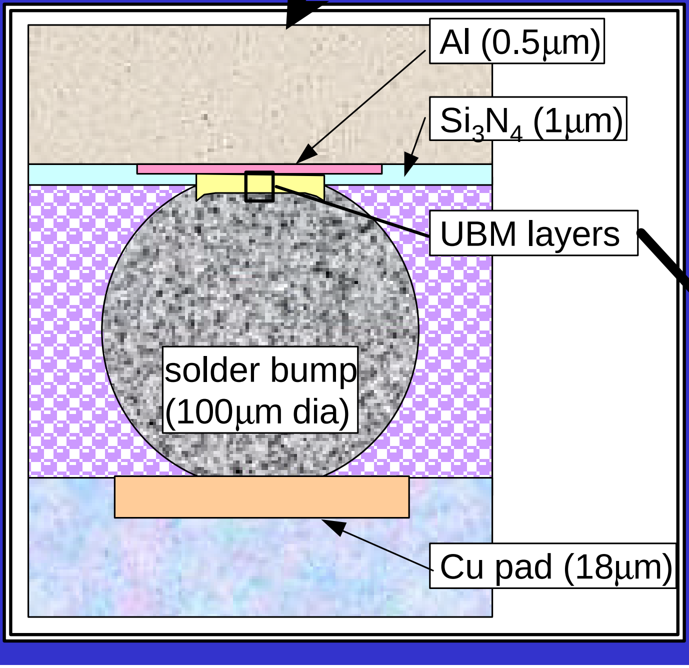
# Structures of UBM and Solder Bumps in Flip-Chip Package

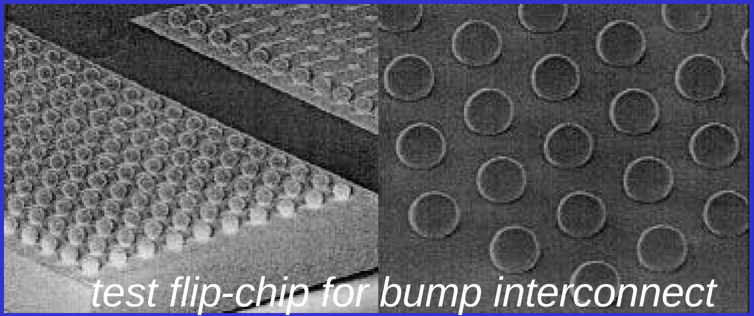
*complex model with scales ranging from millimeters to sub-microns.*

**Packaged Flip Chip** (fabricated at Microfab Technology in Singapore)

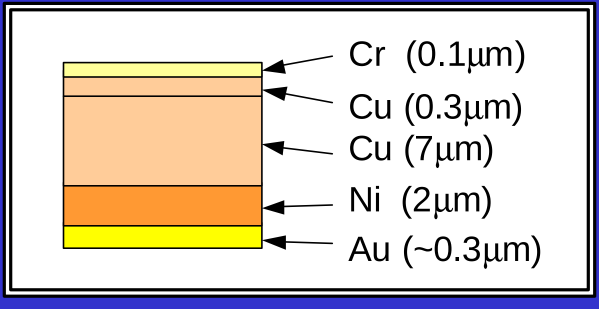


**Solder Bump**




*test flip-chip for bump interconnect*

**Under Bump Metallurgy**



# Key Structural and Material Features

**Structures** ⇒ *dimensions span four orders of magnitude* (mm to sub-μm)

- *In the finite element analysis, very small elements are needed near solder bumps for accurate fracture analysis.*
- *Use Multi-Scale Finite Element Analysis ® two separate calculations, one for the whole packaged geometry (global model) and another for the small region surrounding a single solder bump (cell model).*

**Materials** ⇒ *need to include many material types*

| Materials | CTE (ppm/°C) | E (GPa) | $\nu$ | $\sigma_o$ (MPa) |
|---|---|---|---|---|
| chip (Si) | 2.8 | 131 | 0.30 | |
| passivation ($Si_3N_4$) | 2.9 | 325 | 0.24 | |
| bond pad (Al) | 23.2 | 70 | 0.24 | |
| UBM layer 1 (Cu) | 16 | 117 | 0.30 | |
| UBM layer 2 (Ni) | 12.7 | 200 | 0.31 | |
| solder bump (63Sn/37Pb ) | 21 | 30 | 0.35 | 20 |
| underfill (FP2546) | 33 | 8.5 | 0.28 | |
| substrate (FR4) | 18 | 22 | 0.28 | |

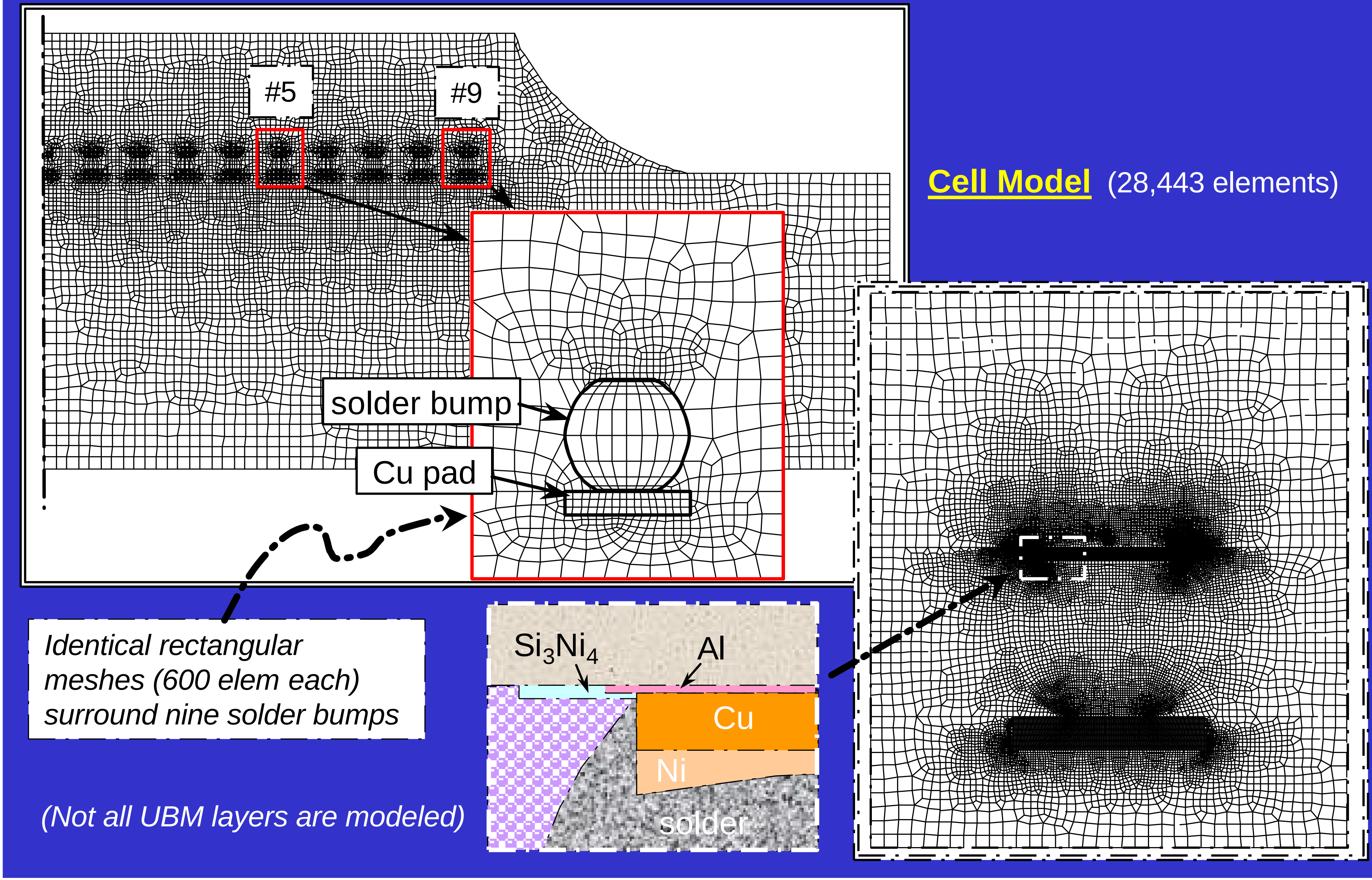
(*only solder is modeled as elastic-plastic materials*)

*Modeling is the biggest task !*

# Multi-Scale Finite Element Analysis

**Global Model** (12,551 elements)

**Cell Model** (28,443 elements)

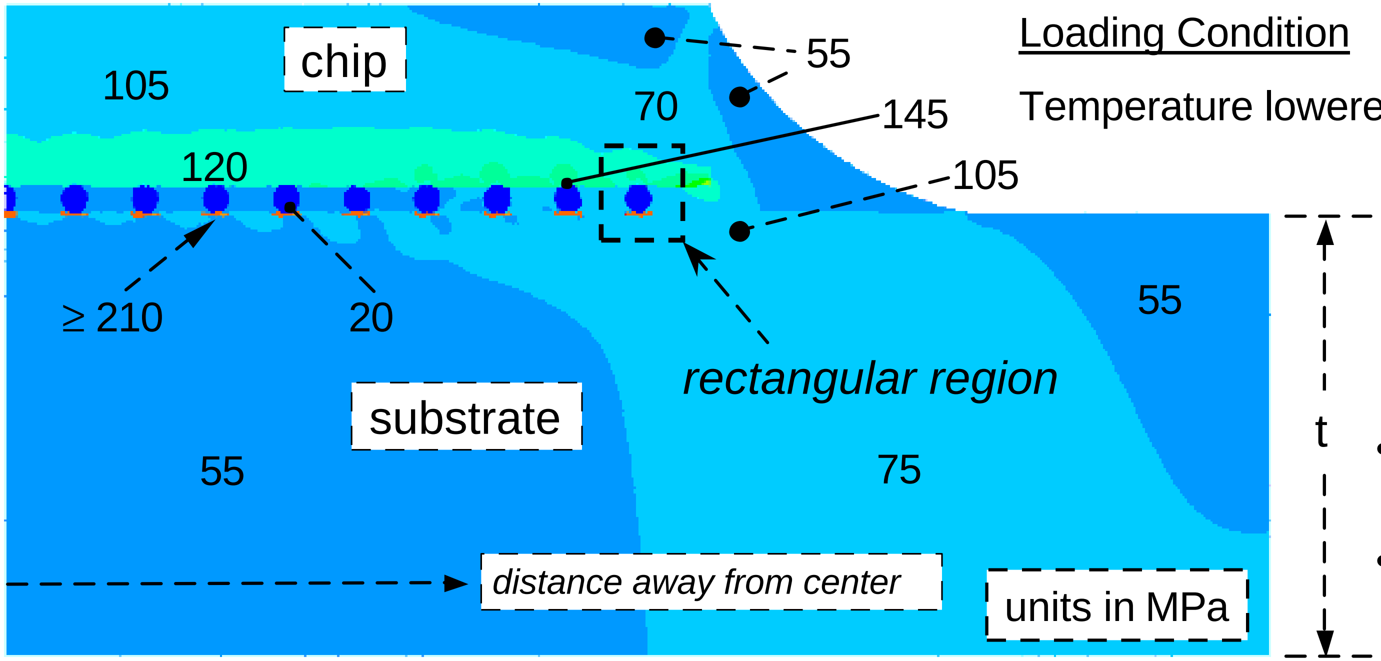


*Identical rectangular meshes (600 elem each) surround nine solder bumps*

*(Not all UBM layers are modeled)*

# Finite Element Analysis (Global Model)

⇒ *evaluate deformation surrounding each solder bump*



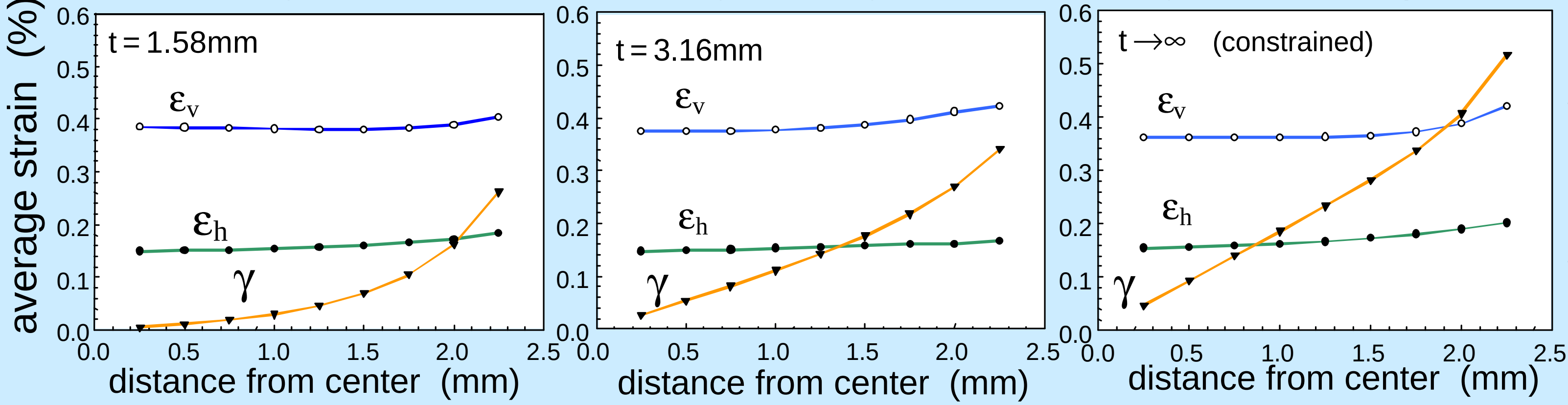
Loading Condition

Temperature lowered from 180°C to 20°C

mises stress
@ ΔT= –160°C

- *Solder bumps are completely yielded*
- *Higher stress further away from center*

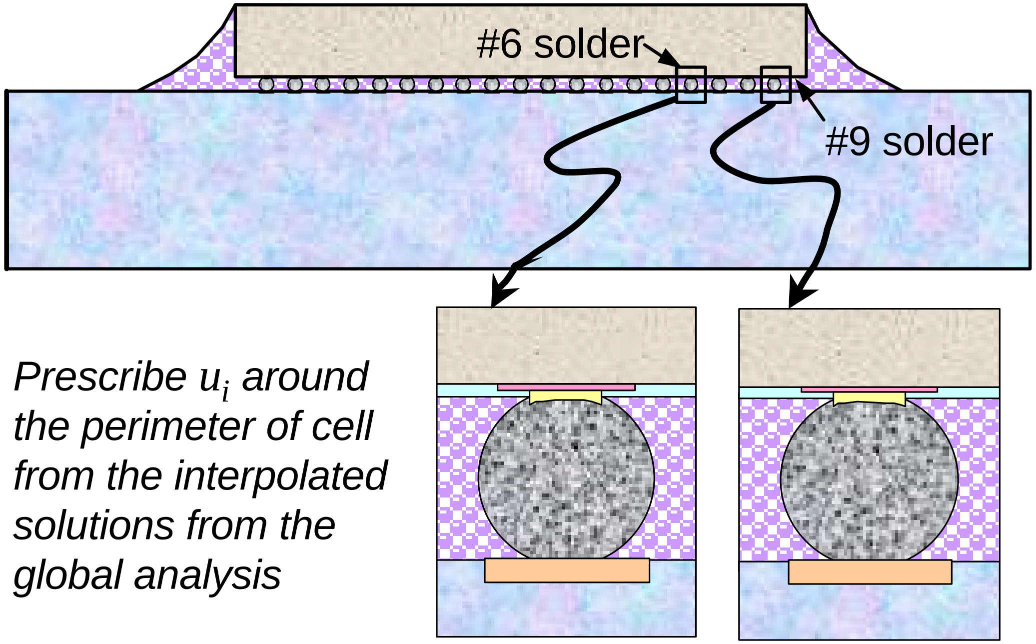
Average Strains within Rectangular Regions surrounding Solder Bumps



- *Normal strains nearly constant*
- *Shear strain increases toward edge*
- *Magnitudes higher with thicker substrate*

# Finite Element Analysis (Cell Model)

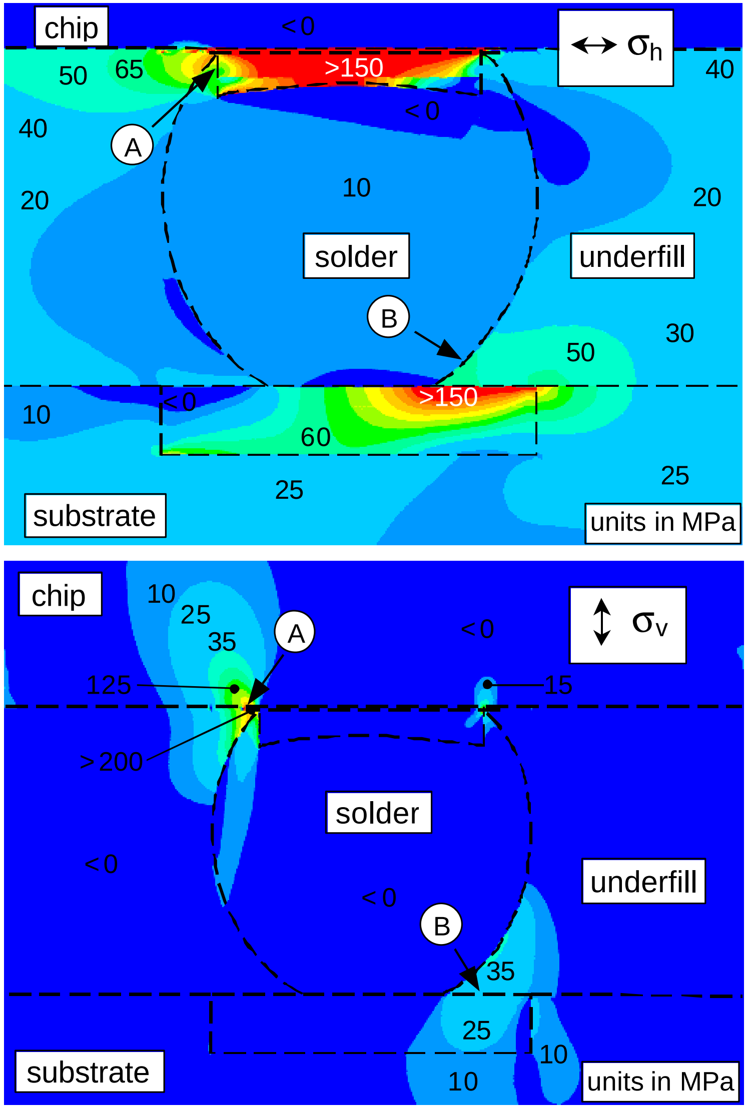
⇒ *evaluate detailed deformation surrounding each solder bump*



*Prescribe $u_i$ around the perimeter of cell from the interpolated solutions from the global analysis*

*Normal Stresses*

*#9 solder bump with t = ∞*



## Consistency Check

*Measure the accuracy of two-model analysis by comparing;*

1. *Total reaction forces on four sides*

$\Sigma \underline{F}_{global}$ *vs.* $\Sigma \underline{F}_{cell}$ ⇒ *mean difference is 6.8%*

2. *Total strain energy within the region*

$W_{global}$ vs. $W_{cell}$ ⇒ difference *is 3.1%*

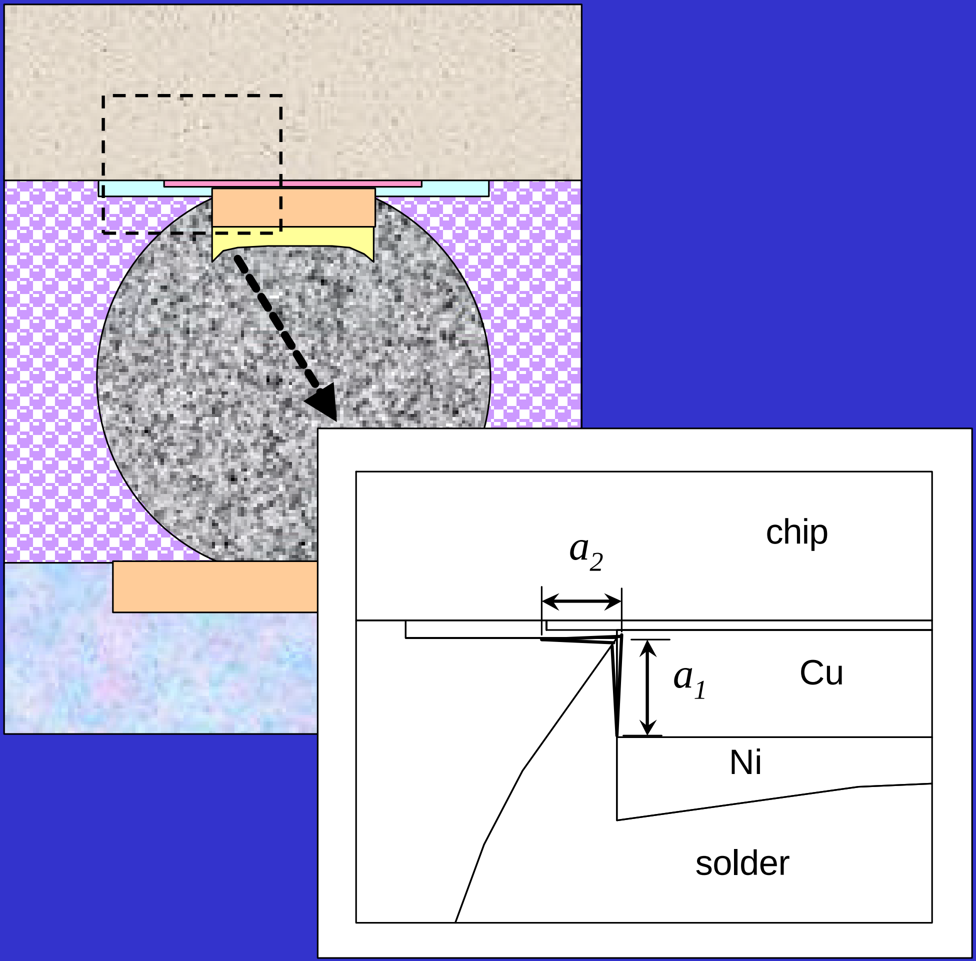
*rectangular region in global model ® 600 elements*
*cell mode for local analysis ® 28,443 elements*

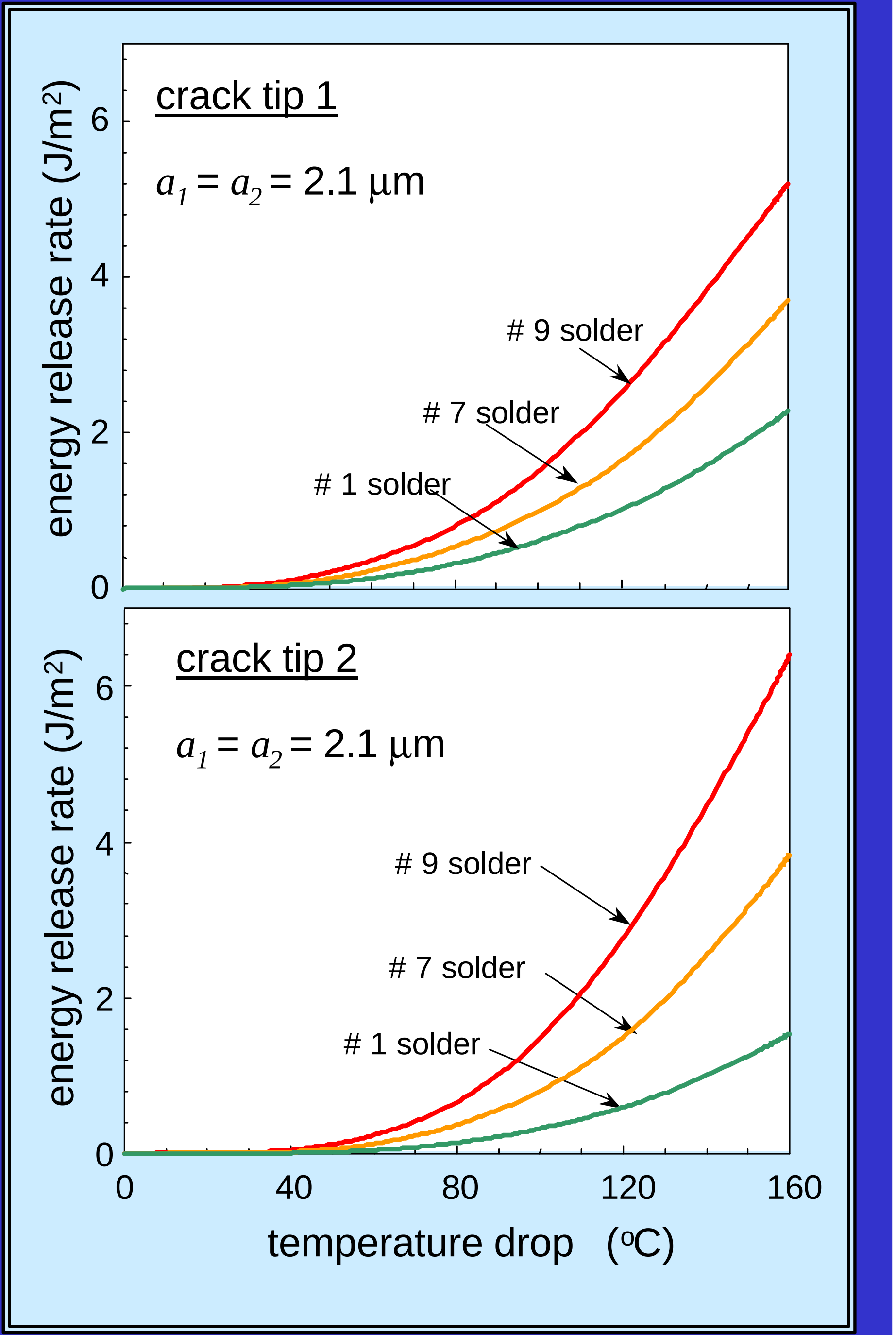
# Delamination Analysis

## Short Cracks

A corner delamination with two interface crack tips between

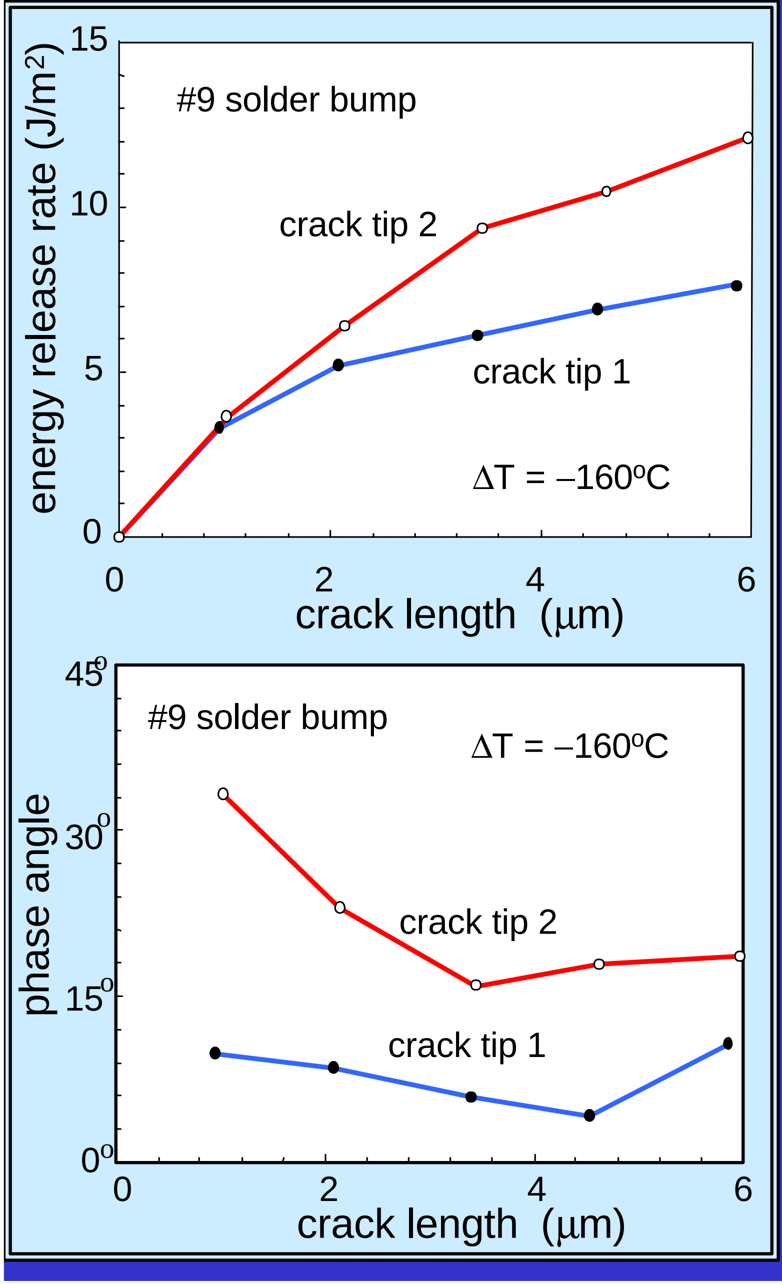
1. Cu and solder
2. $Si_3N_4$ and underfill





## Growing Cracks

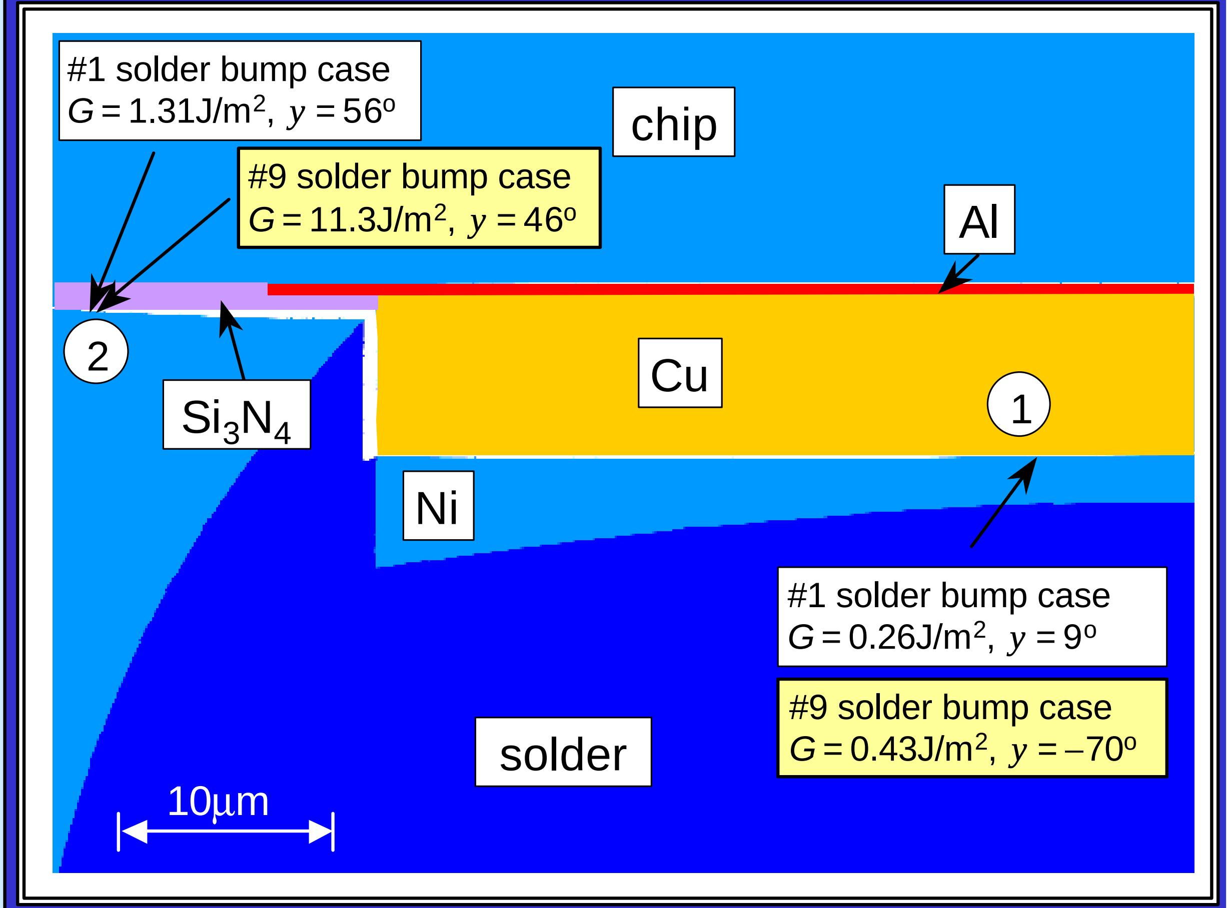
Longer corner interface crack



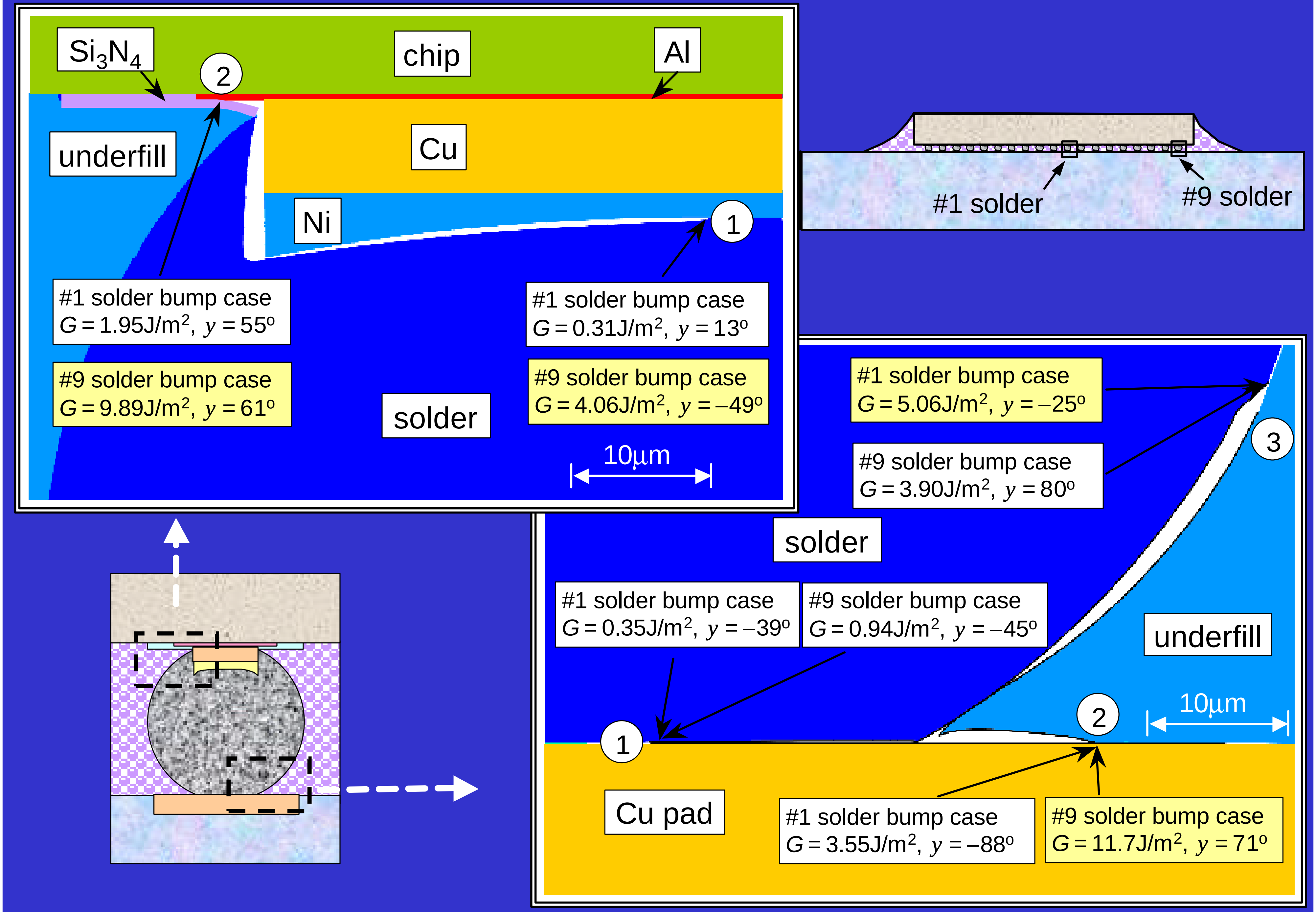
## Long Cracks

Investigate if sufficient crack driving force exist to form long delamination

⇒ *complete debonding leads to loss of electrical connection and chip failure*



# Other Long Cracks



#1 solder bump case $G = 1.95\mathrm{J/m^2}$, $y = 55^{\circ}$

#9 solder bump case $G = 9.89\mathrm{J/m^2}$, $y = 61^{\circ}$

#1 solder bump case $G = 0.31\mathrm{J/m^2}$, $y = 13^{\circ}$

#9 solder bump case $G = 4.06\mathrm{J/m^2}$, $y = -49^{\circ}$

#1 solder bump case $G = 5.06\mathrm{J/m^2}$, $y = -25^{\circ}$

#9 solder bump case $G = 3.90\mathrm{J/m^2}$, $y = 80^{\circ}$

#1 solder bump case $G = 0.35\mathrm{J/m^2}$, $y = -39^{\circ}$

#9 solder bump case $G = 0.94\mathrm{J/m^2}$, $y = -45^{\circ}$

#1 solder bump case $G = 3.55\mathrm{J/m^2}$, $y = -88^{\circ}$

#9 solder bump case $G = 11.7\mathrm{J/m^2}$, $y = 71^{\circ}$

## SUMMARY:

1. Multi-scale models are used to probe the stress state and fracture behavior near UBM and solder bumps of flip-chip packages.

2. Substrate thickness influences the deformation states surrounding solder bumps and UBM.

3. Large opening stresses observed at diagonal corners of solder bumps and they are most likely locations for delamination initiation.

4. Increasing $G$ for growing crack suggests a possibility of unstable crack propagation under thermal loading condition.

5. The long delamination models have shown various scenarios of interfacial delamination.

6. If weak interfacial strength exists between some materials, there is a sufficient crack driving force to cause separation of electrical current