Interfacial Delamination Near Solder Bumps and UBM in Flip-Chip Packages

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Using detailed finite element models, a fracture analysis of solder bumps and under bump metallurgy (UBM) in flip-chip packages is carried out. Our objective is to identify likely fracture modes and potential delamination sites at or near these microstructural components. In order to study flip-chips, whose dimension spans from sub-micron thickness UBM layers to several millimeters wide package, we have applied a multi-scale finite element analysis (MS-FEA) procedure. In this procedure, initially, deformation of whole thermally loaded package is analyzed. Then, the results are prescribed as the boundary conditions in a very detailed cell model, containing a single solder bump, to investigate micro-deformation surrounding UBM. Using the models with two different scales, accurate stress fields as well as fracture parameters of various interface cracks can be determined. The MS-FEA is ideally suited for the flip-chip packages since they contain many identical solder bumps. A cell model can be repeatedly used to probe stress and fracture behaviors at different locations. The computed results show high stress concentrations near the corners of solder bumps and UBM layers. Based on the energy release rate calculations, solder bumps located near the edge of chip are more likely to fail. However, our results also suggest possible delamination growth at solder bumps near the center of chip. In addition, we have observed increasing energy release rates for longer cracks, which implies a possibility of unstable crack growth. [DOI: 10.1115/1.1348338]

1 Introduction

Flip-chip and solder bump interconnects are increasingly used in the electronics industry primarily because of their high I/O density capability, small profiles, and good electrical performance (Lau [1]). The reliability of solder and UBM joints is of significant technological importance for the flip-chip growth. Many investigators have studied the mechanical integrity of flip-chips from various viewpoints. There have been studies in understanding roles of underfill materials and related interface reliability (Rzepka et al. [2], Rzepka et al. [3]), optimizing interconnect structure and its reliability evaluation (Wiegele et al. [4]), and thermal fatigue life prediction (Lau [5]). Fracture behaviors and the effect of process-induced stresses under real loading history with temperature and time-dependent materials were also studied recently (Gall et al. [6], Wang et al. [7]).

Many of these predecessors' works are based on overall simulations (i.e., using single model). But with one model to cover the entire package, the resolution of stress states near solder bumps is limited. Usually it is difficult to construct a model with extreme size differences among its various parts. However, in order to study failure behavior, precise modeling of sub-micron UBM layers is essential since fracture initiation and propagation may occur along these layers. Furthermore, in finite element analyses, very small elements are required for the computations of accurate fracture parameters. Recently Kay et al. [8] pointed out that ''Electronic packages can experience stress singularities due to the presence of dissimilar material properties, geometric discontinuities and plastic deformation. The conventional finite element method (FEM) is not capable of accurately capturing all the information, especially when applying to the small dimensions.'' Madenci et al. [9,10] have introduced the global/local analysis, and carried out finite element to study stress concentration near the interfaces of very small parts.

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In this paper, we propose an approach based on the multi-scale models and extend the global/local procedure to carry out the detailed fracture study of flip-chip packages. This procedure is straightforward but also computationally effective. Essentially, two models with different size scales are constructed and they are used in the stress and fracture analyses near solder bumps. First, a global model for flip-chip package is designed, and then, a refined local/cell model containing single solder bump and UBM layers is constructed. Unlike typical conventional multi-model analyses, the present cell model includes additional materials (for the UBM layers). The element sizes in the cell model are small enough to obtain accurate fracture parameters. This two-step procedure allows us to perform detailed stress and fracture analyses.

2 Inter-Facial Fracture Parameters

Various studies have demonstrated that the energy release rate G and the phase angle ψ are the most suitable set of fracture parameters to characterize the crack driving force and toughness of cracks in layered or multi-phase structures under mixed-mode loading conditions (Cao and Evans [11]). In the linear fracture mechanics or the elastic-plastic fracture mechanics without crack growth or large elastic unloading, the energy release rate is equivalent to the path-independent J-integral. Therefore, its value can be accurately and readily extracted from the finite element fields far from the crack tip. For a 2D crack with crack advancing in the x_1-direction, it is

$$G = \int_{\Gamma} (W n_1 - \sigma_{ij} u_{i,1} n_j) ds \tag{1}$$

here W is the strain energy density, σ_{ij} and u_i are the Cartesian components of the stress and displacement, respectively. The crack tip is enclosed by an arbitrary contour Γ and n_j denotes the components of unit vector normal to Γ.

The phase angle ψ represents the ratio of shear to normal traction ahead of the crack tip or the ratio of the shearing mode (Mode II) to the opening mode (Mode I). It is an important parameter in defining the fracture toughness or the critical energy release rate

G_c of a bimaterial interface. Various experiments have shown that G_c is strongly dependent on this mode ratio. For elastic interfaces, the phase angle can be determined by the mixed-mode stress intensity factors extracted from the interaction energy integral (Lo et al. [12]). But for elastic-plastic interfaces, the phase angle can be defined from the stresses ahead of the crack as,

$$\psi \approx \tan^{-1}\left\{\frac{K_{\mathrm{II}}}{K_{\mathrm{I}}}\right\} = \tan^{-1}\left\{\left(\frac{\sigma_{r\theta}}{\sigma_{\theta\theta}}\right)_{\theta=0^o,\ r=L}\right\} \tag{2}$$

Here K_{I} and K_{II} are the stress intensity factors of the in-plane opening and shear modes, respectively. Also $\sigma_{r\theta}$ and $\sigma_{\theta\theta}$ are the shear and opening stresses of ahead of the crack tip. In general, the phase angle must be defined in term of a characteristic length scale L. In our analysis, it is chosen as $L=0.8$ μm. Also the stresses are measured at the same L or about four-element length ahead of the tip. Under pure Mode I condition, $\psi=0$ deg, while $\psi=\pm 90$ deg corresponds to pure Mode II condition. In general, $G_c(\psi)$ is the lowest at $\psi=0$ deg, and increases with ψ. This means greater energy is needed for crack initiation under shear dominant condition. The energy release rate G as well as K_{I} and K_{II} (when both sides of an interface are elastic) are computed using the domain integral formulations. The detailed expressions and derivations of these integrals are shown by Lo et al. [12].

3 Multi-Scale Computational Procedure

3.1 Flip-Chip Geometry and Global Model. In the present investigation, a two-dimensional section of a flip-chip attached to a substrate is considered. Although 2D models idealize actual geometry of flip-chips, 3D study would require much more computational effort and also make the fracture analysis extremely complex. The 2D study should still reveal important mechanical characteristics of flip-chips. The present flip-chip represents a test specimen used by the Institute of Materials Research and Engineering in Singapore. The chip is 5 mm long and contains nineteen solder bumps in a single row as shown in Fig. 1(*a*). Each solder bump is numbered from the symmetric line at the center as indicated in the figure. Here #0 solder bump is located at the center while #9 solder bump is at the outermost edge of the chip. Each solder bump is nearly circular with the diameter of 100 μm and the bump pitch is 250 μm. The flip-chip is bonded to the substrate by an underfill material. The thickness of the substrate (t) is varied to study the effects of bending caused by various constraint conditions. Three different thicknesses are considered. They are $t=1.58$ mm, 3.16 mm, and ∞. The last case corresponds to the substrate being constrained from warping (i.e., the bottom plane is kept flat), which corresponds to a very thick substrate. Larger internal bending moment is expected for thicker substrate. Due to symmetry condition, only the right half of the overall package is modeled by finite elements. The finite element mesh is constructed with 12,551 four-node plane strain isoparametric elements as shown in Fig. 1(*b*). To carry out the multi-scale analysis, a significant care has been taken during the design of the mesh. First, small elements are placed near the solder bumps. Second, the mesh around every solder bump is set identical and shaped rectangular as shown. The rectangular enclosure, as depicted by the enlarged picture in the figure, is needed for the subsequent cell analysis. Within each rectangular region, there are about 600 elements. Only solder bump and copper pad are distinctly modeled in this model. The UBM and passivation layers are too small to be included in this model scale. A much finer cell model with these microstructural features is described next.

3.2 Cell Model. In the second step of the analysis, more detailed ''cell model'' is constructed for the region containing a single solder bump as shown in Fig. 2(*a*). Two layers of UBM, Ni with 2.2 μm thickness and Cu with 7.3 μm thickness, are also modeled here. Although, actual UBM contains additional layers (e.g., Au, Zn), these thin layers (<0.1 μm) are not included here because of their small scale and limited mechanical influence.

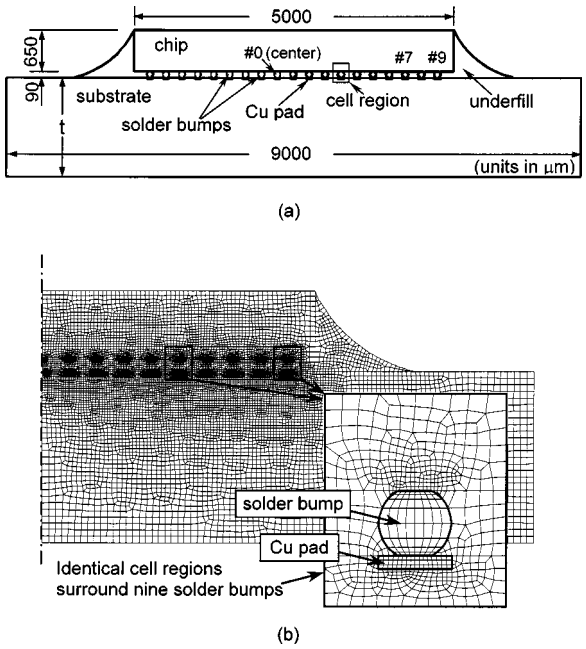
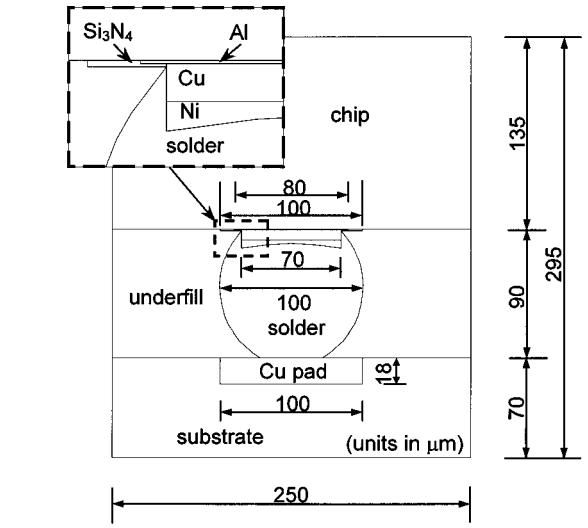


Fig. 1 (*a*) Overall geometry of the flip-chip package showing the locations of solder bumps. (*b*) Finite element mesh for the half model of the flip-chip package. A rectangular region surrounding a single solder bump is enlarged.

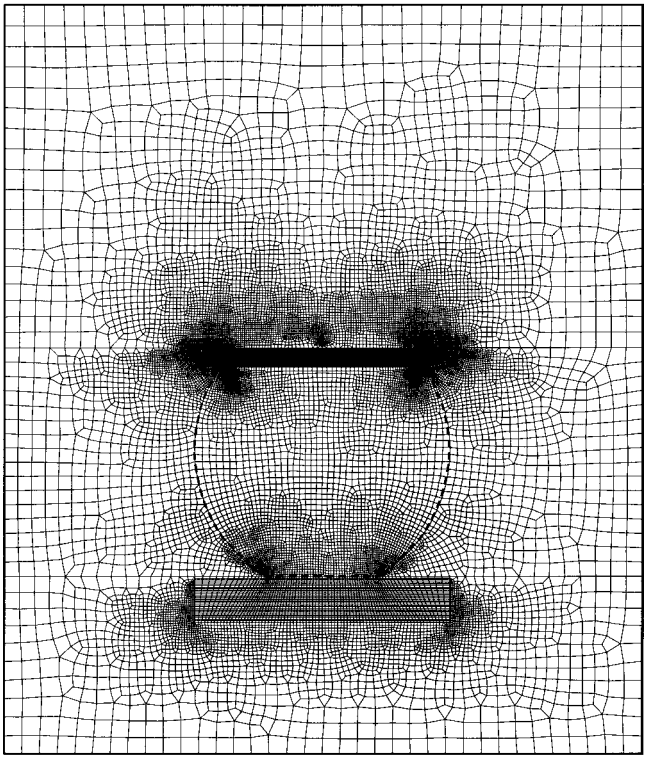
However, their presence can alter the interfacial fracture toughness in real materials and should be considered when the energy release rate is determined. On the chip side, the Al bond pad and the Si_3N_4 passivation layer are also modeled with respective thickness of 0.5 μm and 1.0 μm. In constructing the finite element mesh, elements along interfaces near the UBM are kept very small as shown in Fig. 2(*b*). Sufficiently small elements are necessary since this mesh will be used for the fracture analysis as well. The size of the smallest elements is about 0.15 μm. Once the mesh is made, it can be used to analyze any solder bumps (#0~9) in the flip-chip package. Only the boundary condition must be changed accordingly. In all, total of 28,443 plane strain elements is employed to construct the cell mesh.

3.3 Material Models. Many materials considered here are commonly used in various electronic package applications (Pecht et al. [13]; Information Science Institute [14]). At high temperature, these materials are usually sensitive to temperature. However, we assumed their properties to be independent of temperature and loading rate since these factors would make the fracture analysis extremely complex. As shown in Table 1, the eutectic solder (63Sn/37Pb) is the only material treated as elastic-plastic since its yield stress ($\sigma_0=20$ MPa) is far below those of other materials. The linear plastic hardening slope is set as 1.0 GPa for the solder. All the others are assumed to be linear elastic materials. In the table, E is the Young's modulus, ν is the Poisson's ratio, and CTE is the coefficient of thermal expansion.

3.4 Thermal and Boundary Conditions. In the present analysis, only a single temperature drop is considered although flip-chip packages are subjected to several temperature cycles during fabrication. The initial temperature is set at 180°C which is near the eutectic temperature of solder. At this temperature, it is assumed that there are very small residual stresses in the package and it is taken as the stress-free temperature. In the simulation, this temperature is gradually reduced to the room temperature at 20°C. Throughout the temperature drop, no transient heat transfer is considered and the temperature within the entire model is as-



(*a*)



(*b*)

Fig. 2 (*a*) Detailed cell model which includes UBM and thin layers attached to solder bump. (*b*) Refined mesh for solder bump and UBM region used the cell analysis. The outline of the solder bump is shown with dashed lines.

sumed to be uniform at every time increment. This temperature change is applied to both the global and cell models.

In the global model, the horizontal displacement along the symmetry is prescribed to remain zero. In addition, for the substrate thickness with $t=\infty$, the vertical displacement along the bottom plane of the model is also constrained. In the cell model, every nodal displacement on the perimeter of the model is prescribed. Initially the thermo-mechanical analysis is carried out with the global mesh. Then the displacement filed around a rectangular region that encloses a solder bump (shown in Fig. 1(*b*)) is extracted. These displacements are interpolated to determine magnitudes of prescribed displacements in the cell model. In the cell analysis, the prescribed displacements are gradually increased until the final values are reached. The temperature is also dropped simultaneously. According to these loading and thermal conditions, the sources of high stresses in the cell region can be operationally classified into two types. One is from the global deformation (through prescribed displacements along perimeter) and the other is from the internal material property mismatch (caused by the temperature drop as well as shearing due to modulus differences). The former contribution mainly arises from the shearing caused by the CTE mismatch between the chip and the substrate. The solder bump location and the substrate thickness control the magnitude of this contribution. However, the latter contribution is independent of solder bump location. It basically depends on the structural and material arrangements of the UBM and the solder bump.

Table 1 Properties of various materials used in the analysis. Only the solder is assumed to be elastic-plastic.

Materials	CTE (ppm/°C)	E (GPa)	ν	σ_0 (MPa)
chip (Si)	2.8	131	0.30	
passivation (Si_3N_4)	2.9	325	0.24	
bond pad (Al)	23.2	70	0.24	
UBM layer 1 (Cu)	16	117	0.30	
UBM layer 2 (Ni)	12.7	200	0.31	
solder bump (63Sn/37Pb)	21	30	0.35	20
underfill (FP2546)	33	8.5	0.28	
substrate (FR4)	18	22	0.28	

4 Stress State Near Solder Bump and UBM

4.1 Stress and Strain Analysis of Global Model. In the first step, the finite element calculation is carried out with the global model. Figure 3 shows the shades of constant von Mises/effective stress after 160°C drop (for $t=1.58$ mm substrate). White circular regions represent the solder bumps. Due to their low yield stress, all of them have undergone complete plastic flow. The largest stress (>210 MPa) is observed within the Cu pads attached to the bumps. As expected, the effective stress is higher as the distance from the symmetry line increases (i.e., left to right).

In order to quantify the deformation surrounding the solder bumps, an effective means is developed. We have determined the ''average strains'' of every solder bump and its neighboring region. Since each bump is enclosed in a rectangular region as shown in Fig. 1(*b*), the average strains within the cell can be approximated from the nodal displacements at the four corners. Three strain components, the normal strain in the horizontal direction ε_h, the normal strain in the vertical direction ε_v, and the shear strain γ are obtained at each of the nine solder bumps

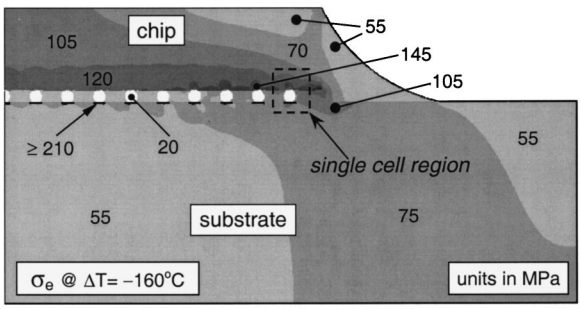


Fig. 3 Shades of constant Mises/effective stresses determined from the global model analysis. While circles represent to completely yielded solder bumps.

(#1~9). In Fig. 4, the average strains are shown as a function of the distance away from the center or symmetry line. Each symbol represents the mid-point location of solder bump (e.g., #1 solder bump is at 250 μm). In the figure, the two normal strains are always positive while the shear strain is negative. Some interesting results can be observed from these figures. First, the vertical strain (ε_v) is nearly uniform through the length and its magnitude is independent of the substrate thickness. This strain component acts perpendicular to the UBM layers and may promote internal delamination. Second, while the horizontal strain (ε_h) is also essentially uniform and independent of the substrate thickness, its magnitude is less than a half of ε_v. Third, the shear strain (γ) is smallest near the center and increases toward the edge. Although this trend was well expected, these figures clearly show the effect of substrate thickness. Essentially, the CTE mismatch between the chip and the substrate generates the shear deformation and its magnitude increases with thicker substrate (i.e., greater constraint). Based on these results, the edge solder bump (#9) appears to be most severely loaded in the thick substrate.

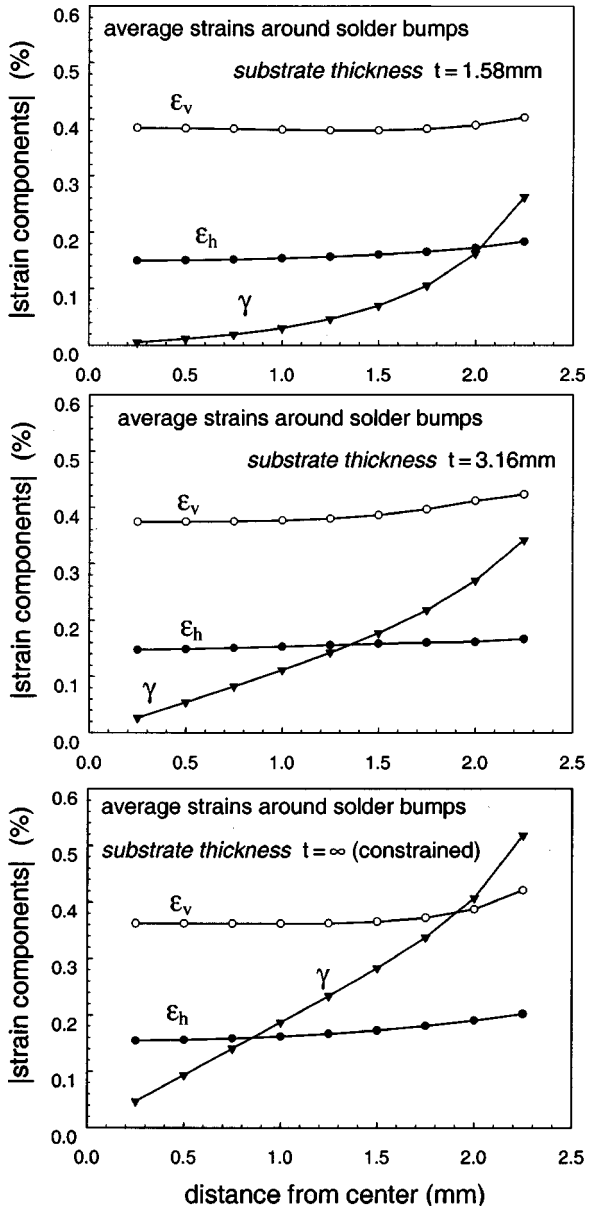


Fig. 4 Average strains surrounding various solder bumps. The mid-location of solder bump is measured from the center/symmetry line of the global model. The three in-plane components are shown for various substrate thicknesses. (*a*) t = 1.58 mm (*b*) t = 3.16 mm, (*c*) $t = \infty$ (very thick/constrained).

4.2 Consistency Check During Model Transition. In the multi-scale model analysis, computed solutions of the global model are transferred to the local/cell model as the boundary condition. In order to ensure this multi-step procedure is accurate, we have checked on the consistency of this transition process. The consistency analysis is important since the present global and cell models contain different sets of materials (i.e., additional UBM layers in the cell model), and also involve complex mechanical and thermal loading. Any errors or differences caused by mesh refinement and loading history dependence of elastic-plastic material must be kept minimal. To quantify the consistency of multi-scale analysis, we have measured two variables. One is the internal/reaction force along the perimeters and the other is the total internal energy.

First, the internal forces are calculated at every node on the perimeter of rectangular region in the global model as depicted in Fig. 1(*b*). Along each of four sides, the nodal forces are summed up to obtain the horizontal and vertical components of the net force through the side (each side has about 14 nodes). Second, the displacements are imposed on the outer boundaries of the cell model as shown in Fig. 2(*b*), and the finite element calculation is carried out to determine the reaction forces. Again the net force on every side is calculated by summing the nodal forces (each side has about 40 nodes). In the final step, the net forces on corresponding sides of the two models are compared. We have carried out this consistency check for the outermost solder bump (#9) since it is subjected to the largest shear deformation. The total difference in the forces acting on the four sides/boundaries is found to be 0.78 percent and 5.60 percent in the horizontal and vertical directions, respectively, for the substrate thickness $t = \infty$. The total internal strain energies within these models are also compared for the consistency. The energy difference between the rectangular region of the global model and that of the cell model is 3.1 percent. These results should represent acceptable levels of consistency in the multi-scale models. The possible sources of error are the large difference in element sizes (the smallest in the global model is about 5 μm while that of the cell model is 0.15 μm), and additional materials included in the cell model.

4.3 Cell Analysis to Identify Risk and Potential Fracture Sites. The cell analysis is carried out for various solder bumps with different substrate thickness. In each analysis, the displacements from the global model are transferred to the cell model boundary. During the calculation, their magnitude is gradually increased while the ambient temperature is simultaneously reduced by 160°C. The first objective of the cell analysis is to identify high stress regions where delamination and failure may occur. Since the average strains are the largest in the outermost #9 solder bump as shown in Fig. 4, this solder bump is chosen for the cell analysis first. Furthermore, we have focused in the case with the very thick substrate ($t = \infty$) where the largest shear strain exists.

In order to achieve our aim of determining possible fracture sites, we have closely investigated the opening stresses. Essentially, we seek for large stresses acting perpendicular to various interfaces. Shades of constant normal stresses in the horizontal and vertical directions determined from the cell analysis are shown in Fig. 5. Two risk regions can be identified from the horizontal stress (σ_h) plot in Fig. 5(*a*). One is the high stress along the interface of the solder and copper UBM layer as denoted by the location A in the figure. The other is the interface between solder and underfill at the location B. Although there is high concentration of stresses within the UBM, their interfaces are along in the horizontal direction and σ_h does not tend to open these interfaces. For the vertical stress (σ_v), high stresses occur at similar locations as shown in Fig. 5(*b*). At the location A, the interface between the underfill and the passivation layer (Si_3N_4) is subjected to large vertical stress. The next highest level of stresses

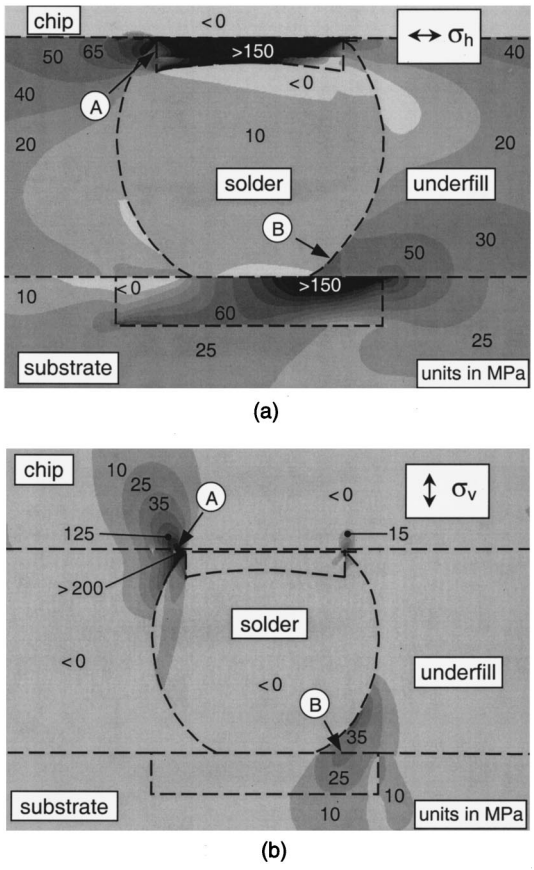


Fig. 5 Shades of opening stresses in the cell model for #9 solder bump for $t=\infty$ after $\Delta T=-160°C$. (*a*) Horizontal normal stress σ_h, (*b*) vertical normal stress σ_v. The locations of high stress regions are indicated by A and B.

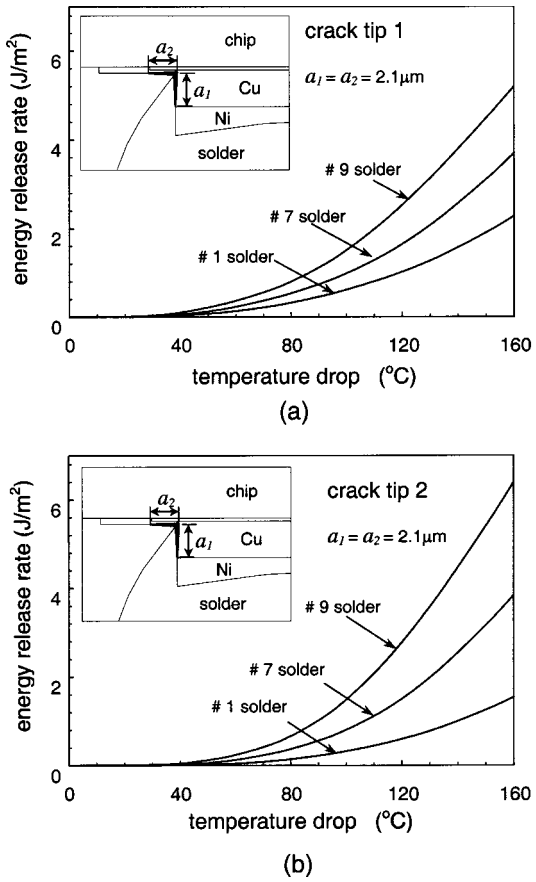


Fig. 6 Energy release rate of short corner delamination as a function of temperature drop for various solder bumps. (*a*) Crack tip 1 and (*b*) crack tip 2. The crack length are fixed at $a_1=a_2=2.1\ \mu$m near.

can be observed at the location B where the interface between the underfill and the Cu pad lies. These large opening stresses may initiate delamination and lead to failure of the solder bump and UBM components. We have also investigated other solder bumps (#1~8) using the identical cell model with corresponding boundary conditions. In general, risk locations based on high opening stresses are similar but the stress magnitudes are somewhat less than those of the solder bump #9.

5 Fracture Analysis of Solder Bump and UBM

5.1 Short Delamination. Based on the results of the previous stress analysis, the cell model is modified to include an interface crack at the location A. Extra nodes are added to form a ''L-shaped'' corner crack as indicated in the inset of Fig. 6. The vertical part of this crack is bounded by the solder bump and the Cu pad with the length a_1, while the horizontal part is between the passivation layer and the underfill with the length a_2. Initially both lengths are fixed at 2.1 μm. In order to quantify the crack driving force, the energy release rates of the two crack tips 1 and 2 are computed with the domain integral program. The energy release rate of the crack tip 1 is shown as a function of temperature drop in Fig. 6(*a*). The results are shown for the solder bumps #1, #7, and #9 with the substrate thickness $t=\infty$. In each case, a separate cell analysis is carried out. A similar plot for the crack tip 2 is shown in Fig. 6(*b*). In both cases, the crack tips in the outermost solder bump (#9) are subjected to significantly higher energy release rate than those of the solder bumps #7 and #1.

The crack driving force primarily arises from two sources. One is due to the local thermal stresses generated by CTE mismatch of various materials in the immediate vicinity of the solder bump, and the other is due to the shear deformation caused by the CTE mismatch of chip and substrate at global level. We have determined each contribution by carrying out additional analysis without any prescribed displacements (i.e., no contribution from the chip-substrate mismatch). The solutions show that the latter source contributes as much as 75 percent of G for the crack tips in #9 solder bump while it is only about 10 percent for #1 solder bump. This means the mismatch of chip and substrate materials causes the dominant crack driving force around solder bumps near the edge.

To study the effects of growing crack, simulations with different crack lengths are carried out. The energy release rates for the crack tips 1 and 2 are shown in Fig. 7(*a*). In each case, when the length of one crack is varied, the other crack length is fixed at 2.1 μm. Both cracks show increasing trends of G as their lengths increase. In fact when the lengths are about 6 μm, G reaches around 10 J/m^2. Although the fracture toughness of these interfaces is yet to be known, it is feasible that such a magnitude is sufficient to initiate delamination growth. Furthermore, increasing energy release rate under longer crack suggests a likelihood of unstable crack growth along these interfaces. We have also determined the phase angle ψ of these cracks and the results are shown in Fig. 7(*b*). The phase angle plays an important role in defining the fracture toughness and the delamination growth behavior along interface boundaries. For the crack tip 1, which lies between the elastic-plastic solder and the elastic copper layer, ψ is determined from the stresses ahead of the crack tip according to (2). On the other hand, ψ of the crack tip 2 is determined from the mixed-mode stress intensity factors since the crack lies between

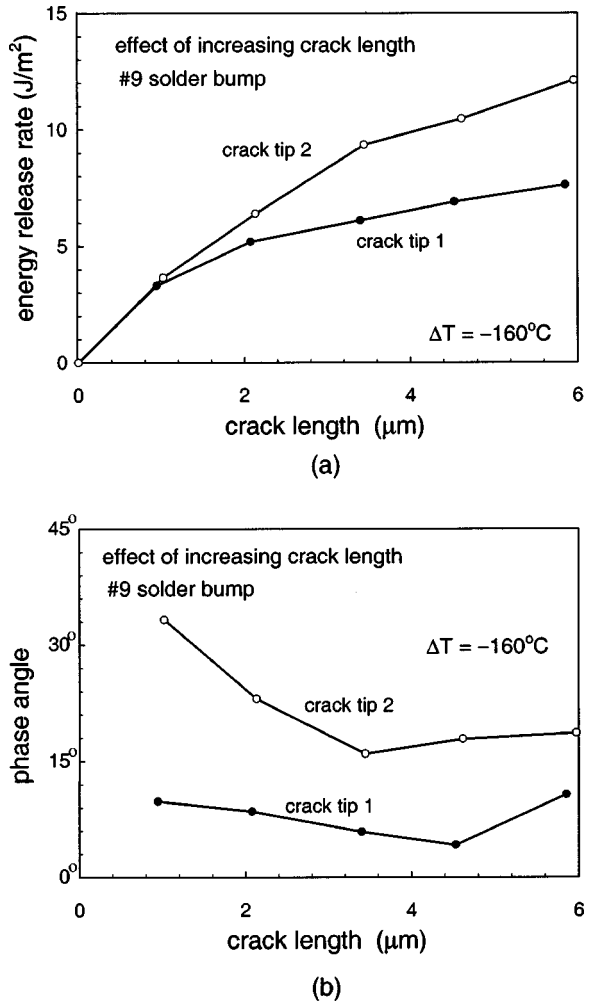


Fig. 7 Fracture parameters of crack tips 1 and 2 versus crack length. The results are for #9 solder bump. Note only one crack length is varied while the other is held at $a=2.1$ μm. (*a*) Energy release rate, (*b*) phase angle.

two elastic materials. The stress intensity factors are obtained from the interaction integrals. The changes of the phase angles under increasing crack lengths are moderate in both cases. The crack tip 1 (vertical crack) is close to pure Mode I while the loading state near the crack tip 2 (horizontal crack) includes to a small Mode II contribution.

5.2 Long Delamination. A small defect or crack may grow to form a longer delamination and ultimately cause chip/package failure (e.g., electrical shorts and disconnection). Using the cell model, we have investigated the long crack behavior in solder bump and UBM regions. Three cases are considered. The first model is an extension of the short delamination presented in the previous section. The corner crack is assumed to grow further along the underfill and Si_3N_4 interface at one end, and through the Cu and Ni layers at the other end. The schematic of this crack (with total length of 51 μm) is shown in Fig. 8. During finite element analysis, in order to avoid overlapping of materials, contact conditions are imposed along the crack surfaces. Afterward, the energy release rate and the phase angle at each crack tip are determined from the computed stress and displacement fields. The results are presented for #9 solder bump (near edge) as well as #1 solder bump (near center) for the substrate thickness $t=\infty$. At the crack tip 1, as indicated in the figure, the energy release rate is significantly higher for #9 solder case. However, at the crack tip 2, both G are comparable although their magnitudes are relatively

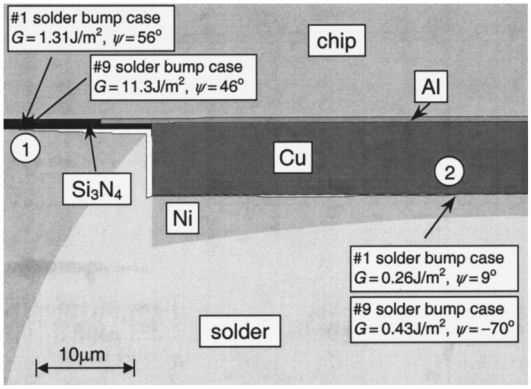


Fig. 8 Schematic of a long delamination near UBM. The crack is along the underfill-Si_3N_4, Cu-solder and Cu-Ni interfaces. The total crack length is 51 μm. The energy release rate and phase angle for #1 and #9 solder bumps are indicated at the two crack tips 1 and 2.

small. Furthermore, the mix-mode condition of #1 solder bump is nearly pure Mode I while that of #9 solder bump is close to Mode II. Since many experimental studies have shown the interface fracture toughness G_c is much less under pure Mode I condition, it is conceivable that first delamination may occur at #1 solder bump (provided G_c of the Cu-Ni interface is relatively small). In other words, under certain conditions, failure may not always initiate in the edge solder bump (#9). This contrasts with common understanding that edge solder bumps are most vulnerable due to high shear. However, the middle solder bumps are also subjected to high normal stresses which can be large enough to separate various UBM layers.

A similar delamination but at a different location is investigated next. Here the crack tip 1 lies between the Al bond and the Si_3N_4 passivation and the crack tip 2 lies between the solder bump and the Ni layer as shown in Fig. 9. The computed energy release rate and phase angle at the crack tip 1 are similar to those of the previous model. However, more interesting results are observed for the crack tip 2. While G and ψ are similar to those of Fig. 8 for #1 solder bump, the energy release rate of #9 solder bump is much higher than that of previous case. This significant jump in G is attributed to large plastic flow in the solder. Since #9 solder bump experiences much greater shear deformation than #1 solder bump does (see Fig. 6), the amount of plastic yielding is greater. Consequently, the interface crack lying between the highly yielded solder and Ni has much larger G. In the previous case (Fig. 8), the crack tip lies between two elastic materials Cu-Ni.

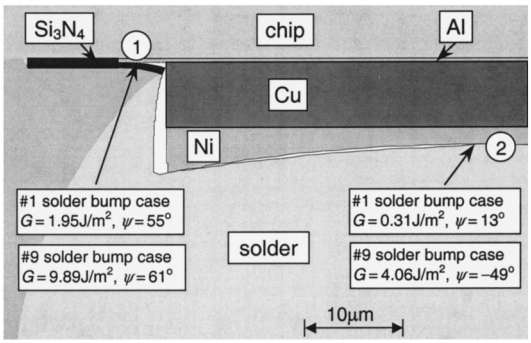


Fig. 9 Schematic of a long delamination near UBM. The crack is along the Si_3N_4-Al, Cu-solder and Ni-solder interfaces. The total crack length is 50 μm. The energy release rate and phase angle for #1 and #9 solder bumps are indicated at the two crack tips 1 and 2.

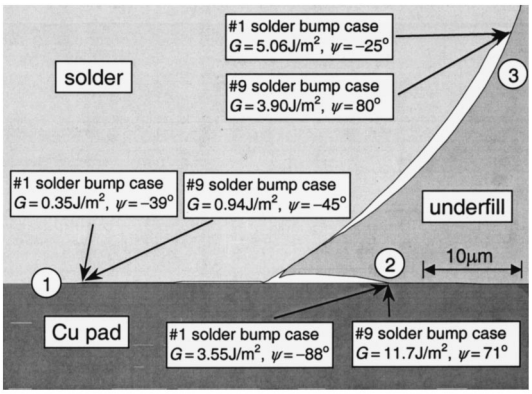


Fig. 10 Schematic of a long delamination near triple junction of solder, underfill and Cu pad. The crack is along the Cu pad-solder, solder-underfill and Cu pad-underfill interfaces. The total crack length is 73 μm. The energy release rate and phase angle for #1 and #9 solder bumps are indicated at the three crack tips 1, 2, and 3.

A different type of long delamination is also investigated. This crack is located at the other side of solder bump where a triple junction of solder, Cu pad and underfill exists (location B in Fig. 5). It contains three crack tips as shown in Fig. 10. A large energy release rate is observed at the crack tip 2 for #9 solder bump. In addition, at the crack tip 3 along the solder and underfill interface, the computed energy release rate is higher for the solder bump #1 than that of the solder bump #9. This result contrast with the other crack tips where the energy release rates are always higher in #9 solder bump than in #1 solder bump. Again the reason lies on the large horizontal stress observed in the middle solder bumps.

6 Summary and Conclusions

In order to investigate the fracture at the level of thin UBM layers, the multi-scale finite element procedure is utilized in this study. This procedure is ideally suited for the flip-chip packages that contain many identical solder bumps, and where large differences in the microstructural length-scales exist. The following failure characteristics are revealed in the current analysis.

1 Substrate thickness influences the deformation states surrounding solder bumps. A large shear deformation at the outermost solder bump occurs with a thick or constrained substrate while two components of normal deformation are nearly constant throughout.

2 Large opening stresses are observed at the diagonal corners of solder bumps. At these potential critical/risk sites, micro flaws and defects can be generated. Under various loading conditions, they can grow and initiate the failure of electronic components.

3 Even for short cracks (e.g., a few microns long), the energy release rate can reach to a significant level under 160°C drop in temperature. The current multi-scale models reveal that a major contribution of crack driving force arises from the shear deformation caused by the chip-substrate CTE mismatch.

4 Under a fixed temperature, increasing G for longer crack is observed. It suggests a possibility of unstable crack growth in the solder bump regions.

5 The long delamination models have shown several possibilities of interfacial delamination. Material separation is possible at various locations. Exact nature of failure depends on the interfacial toughness of actual materials.

6 Although our study supports that the outermost solder bump is the most likely location to fail, some UBM interfaces near the central solder bumps are also subjected to large opening stresses. Any initial defect or weak bonding can cause these solder bumps to fail prior to the outermost solder bump.

Our analysis elucidated possible mechanical failure modes in a very complex flip-chip package. Relevant fracture parameters were deduced with the multi-scale models. Using similar models, one can optimize geometry and/or materials to lower crack driving energy. However a better prediction of failure near the solder bumps and UBM requires the knowledge of various interfacial fracture resistances. Furthermore, the models can be refined to include temperature and rate effects.

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