AN EXACT ANALYSIS OF CLASS-E POWER AMPLIFIERS FOR RF COMMUNICATIONS

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Abstract - An exact analytical approach to the design of a Class-E high frequency power amplifier is presented. The analysis will optimize the load network parameters at the output of the switching transistor, while accounting for harmonics injected into the circuit from the choke inductor, finite quality factor of the output load network, and an exponential decay of the drain/collector current during OFF state. Calculated power performances in terms of efficiency and Total Harmonic Distortion (THD) as a function of decay angle and finite choke inductance are presented.

1. INTRODUCTION

Class E power amplifiers are used for narrow band RF applications where high efficiency is required. In an ideal case, these amplifiers can be shown theoretically to be 100% efficient. The ideal case is defined under the following assumptions:

1) Infinite choke inductance to suppress all harmonics of the current feeding the amplifier from DC power supply.
2) The transistor works as an ideal switch with no decay time for current during turn OFF, zero ON and infinite OFF resistance.
3) The tuned network at the output only passes the fundamental frequency and blocks all other harmonics.

Gaudo *et al*. and Li *et al.* [1-2], have accounted for the finite choke inductance, while the finite decay time of the transistor output current has been modeled by Kazimierczuk [3]. Tu *et al*. [4] have accounted for both the transistor decay and the finite quality factor of the output load network. For accurate analysis, non-idealities due to finite choke inductance, transistor current decay rate, and quality factor of the load network inductance have to be considered. Such a comprehensive analysis is not reported yet and is the topic of this paper. The proposed analysis employs an iterative technique to calculate the amplifier performances and load network parameters.

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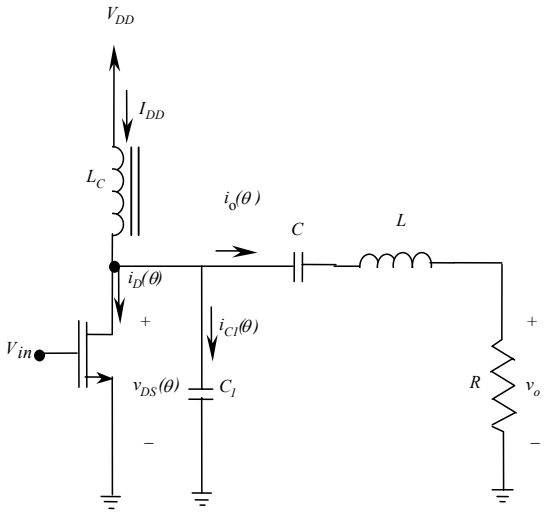

Fig. 1. Class E amplifier

2. ANALYSIS

The proposed analysis uses an iterative scheme and the first iteration begins with the initial conditions being those of the ideal case. An iteration will provide one solution to a series of equations whose solution will be reentered as the initial conditions to the subsequent iterations.

In this simulation, the operating frequency is assumed to be 2.4GHz. The output is assumed to be a sinusoidal signal given in eq. (1)

$$i_o = \frac{a}{R}\sin(\omega t + \phi) \tag{1}$$

where a is the amplitude of the output voltage, R is the load resistance, and ϕ is the initial phase shift of the fundamental frequency at the output. The load resistance is assumed as 10Ω to provide sufficient power to the load. A matching circuit is required to match this load resistance to a standard 50Ω resistance. In the first

iteration, the phase of the output, ϕ, is assumed as

$$\phi = \tan^{-1}\left(2/\pi\right) \tag{2}$$

when zero fall time for the transistor turn off current is assumed [5]. This is only valid for the first iteration when the choke current is still assumed to be a DC value. For subsequent iterations and for the first iteration when transistor decay is assumed, the phase will be set to produce the desired switching conditions as discussed later.

The current through the shunt capacitor can be defined as I_{DD}-i_o when the transistor is OFF ($0 < \omega t < \pi$), and zero when the transistor is ON ($\pi < \omega t < 2\pi$). Assuming a 50% duty cycle of the input signal, the capacitor current is given by,

$$\begin{aligned} i_{C1} &= I_{DD} - i_o - i_{C1}(0)\exp(-\tau \cdot t) && 0 < \omega t < \pi \\ i_{C1} &= 0 && \pi < \omega t < 2\pi \end{aligned} \tag{3}$$

where I_{DD} is the DC choke current and ω is the angular frequency.

The drain current can then be defined in a similar manner, except conducting for the other half of the period,

$$\begin{aligned} i_D &= i_{C1}(0)\exp(-\tau \cdot t) && 0 < \omega t < \pi, \\ i_D &= I_{DD} - i_o && \pi < \omega t < 2\pi. \end{aligned} \tag{4}$$

Here it is assumed that the transistor has zero ON resistance. The voltage at the drain can then be found by integrating the current through the capacitor:

$$v_{DS} = \frac{1}{\omega C_1}\int_0^t i_{C1} \cdot dt\,. \tag{5}$$

Since no power is consumed in the choke inductor, C_1 is set so that the average value of the drain voltage is equal to the power supply voltage. The Fast Fourier Transform (FFT) of v_{DS} yields the amplitude and phase of the signal entering the load network. In the first iteration, L and C can be found to produce the desired phase shift given in eq (2). It is important to note that non-desired harmonics at the output will be better attenuated with larger values of L. For this reason, L is assumed and C is calculated. The output can then be calculated using the loaded Q of the network and the amplitude and phase of the harmonics going into it. Each nth harmonic will be attenuated by a factor of $\left(1 + Q^2(n)\right)^{-1/2}$, and is shifted by a phase $\theta(n)$ as calculated by the equations -

$$Q(n) = \frac{n\omega L - \frac{1}{n\omega C}}{R}\,, \text{ and} \tag{6a}$$

$$\theta(n) = \tan^{-1}\left(Q(n)\right). \tag{6b}$$

Verification of the initial conditions and the optimal switching conditions is now performed. The amplitude of the output current that was used initially to calculate i_{C1} (see eq. (3)) should equal the calculated output current, and v_{DS} and its derivative ($\frac{i_{C1}}{\omega \cdot C_1}$) should equal zero at $\omega t = \pi$ [5]. One set of solutions of ϕ and a exists that can satisfy these conditions, and is used in the subsequent iteration.

In the second iteration, i_{C1} will be calculated using the i_o found after eq. (6) which now includes the harmonics at the output. However, the choke current will no longer be assumed DC, but will be found from the equation for v_{DS} -

$$i_{L_C} = \frac{1}{\omega L_C}\int_0^t (V_{DD} - v_{DS})dt\,. \tag{7}$$

In the above equation, V_{DD} is the power supply voltage, and is assumed as 3.3V in this simulation. L_C is varied from 1nH to 5nH to see its effects on the amplifier's performance. a and ϕ are then recalculated following equations (3) through (6) and optimal switching conditions, as mentioned above, are verified. The calculation is repeated until convergence, which typically occurs after the third iteration. For this solution, the exponential decay is accounted for in i_{C1} (eq. 3), the output Q is accounted for in i_o (eq. 6), the finite choke inductance is included in i_{Lc} (eq.7).

3. RESULTS

The simulation was performed using choke and load network inductor values of 1nH, 3nH, and 5nH, and decay angles of 0, 30, and 60 degrees (represented by τ of infinity, 5.9, and 2.95 respectively). The decay angle is calculated as the value of ωt when the exponential drain current reaches three time constants of its initial amplitude. It was observed through simulation that all three of the non-idealities made a noticeable impact on the performance of the amplifier, the optimal phase of the output, and the calculation of circuit parameters.

3.1. Effects of Finite Inductors

As we decrease the choke inductance, the most prominent

result is the increase in the ripple on I_{DD}. As seen in Figure 2, this ripple can become quite significant for inductor values reasonable in modern CMOS processes. A large portion of the energy in the ripple resides in the first harmonic, and when this is passed to the output, efficiency is slightly increased and Total Harmonic Distortion (THD) is decreased as seen in Figure 3. The load network inductor L does not affect the waveforms as such, but has a drastic effect on the distortion of the output. This is because L only affects the magnitude of the harmonics reaching the output i_o. Even though i_o is seen in the i_{C1} calculation, the dominant factor in the shape of the waveform is the fundamental frequency. We can also see from Figure 4 that varying the inductors has a drastic effect on the phase of the tuned network resulting

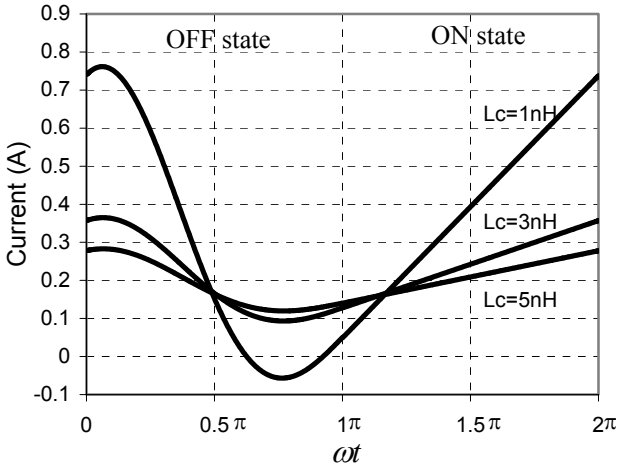

Fig. 2. Variations in the choke current due to changes in Lc. Here, L = 1nH and transistor decay angle is 0.

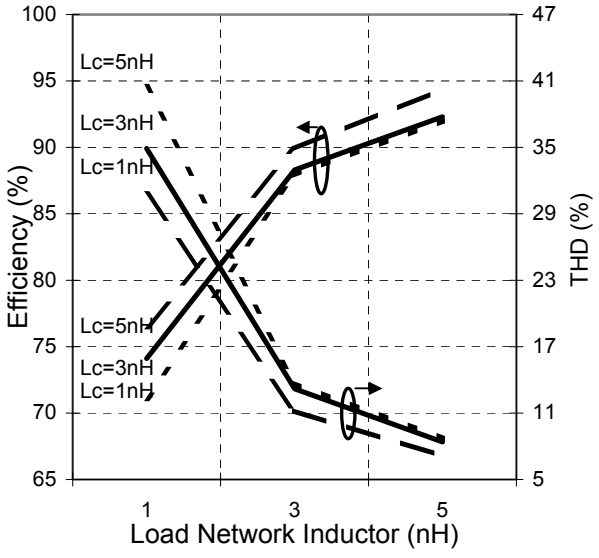

Fig. 3. Variations of percent efficiency and THD with choke and load network inductors. Here, ideal transistor switching was assumed.

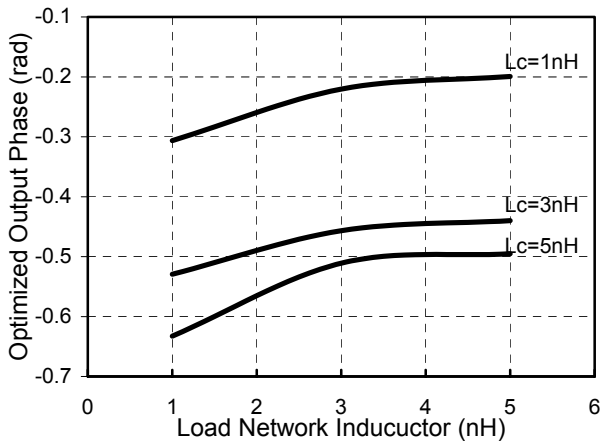

Fig. 4. Effects of inductors on optimal output phase. All points were simulated with no transistor decay angle.

in a modification of the desired load network capacitor. Note that in the ideal case, the phase should be approximately –0.567 radians [5].

3.2. Effects of Decay Angle

Without a decay angle, all of the power is consumed in the load. The only loss of efficiency is power consumed by the load at undesired frequencies. This is due to the fact that in ideal operation, the transistor voltage and current are never non-zero at the same time. When decay is introduced, there may be significant overlap between the voltage and the current, and the efficiency decreases. However, THD decreases because there is less harmonic power from a gradual change from the ON state to the OFF state as apposed to the discontinuity in the current seen in the ideal case. THD was calculated as the sum of magnitudes of all non-desired harmonics divided by the fundamental.

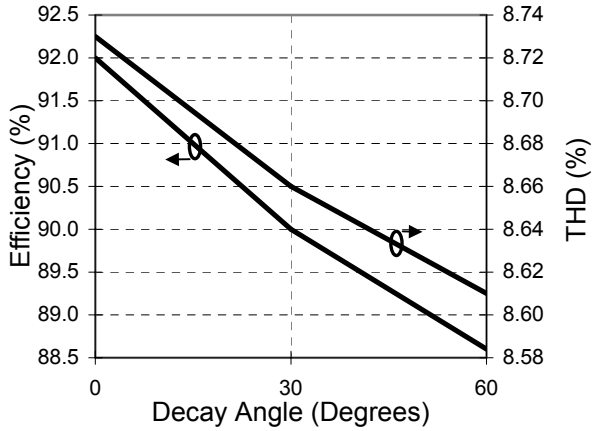

Fig. 5. Effects of decay angle on efficiency and THD. Here, L_C =L=5nH.

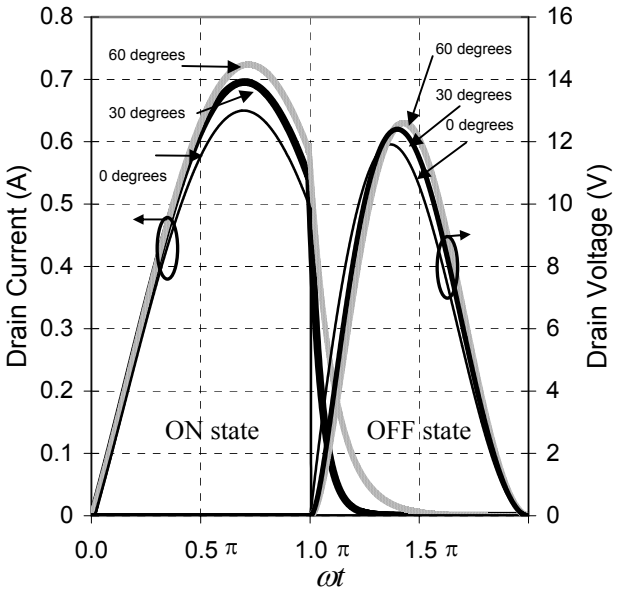

Fig. 6. Variations of drain current and drain voltage with respect to transistor decay angles of 0, 30, and 60 degrees. Here, L_C =L=5nH.

In Figure 6 it is shown that the overlap region between v_{DS} and i_D becomes more significant at lager values of decay angle. The area of this overlap region represents the power lost within the transistor. An observable shift in the v_{DS} curve at higher decay angles is also represented, and is correlated to a shift in the desired output phase as seen in Figure 7.

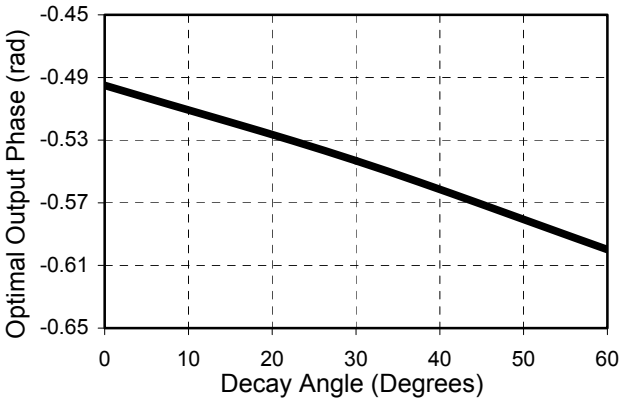

Fig. 7. Variations in the optimal phase of the output due to the decay angle of the transistor. Here, L_C =L=5nH.

4. CONCLUSIONS

A complete analysis of a Class-E power amplifier has been presented accounting for the three most prevalent non-idealities including harmonics in the choke current due to finite choke inductance, finite decay time of the transistor current at turn off, and harmonics at the output due to finite loaded Q of the load network. It is shown that the greatest impact on the desired phase of the output is due to the finite choke inductor, followed by the decay angle, and lastly the load network inductor. This phase difference will affect the value of the load network capacitor required to achieve optimal results. The load network inductor, however, has the greatest effect on the efficiency and the distortion at the output, while the choke inductor has the least impact.

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