EEE523 Project #1

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Registered at Intel site

1. Design specification and goals

The purpose of this project is to design and simulate a CMOS current mirror to meet certain criteria for output resistance, minimum output voltage, size and power consumption. All work on this project must be done on an individual basis, and each person must turn in a separate report.

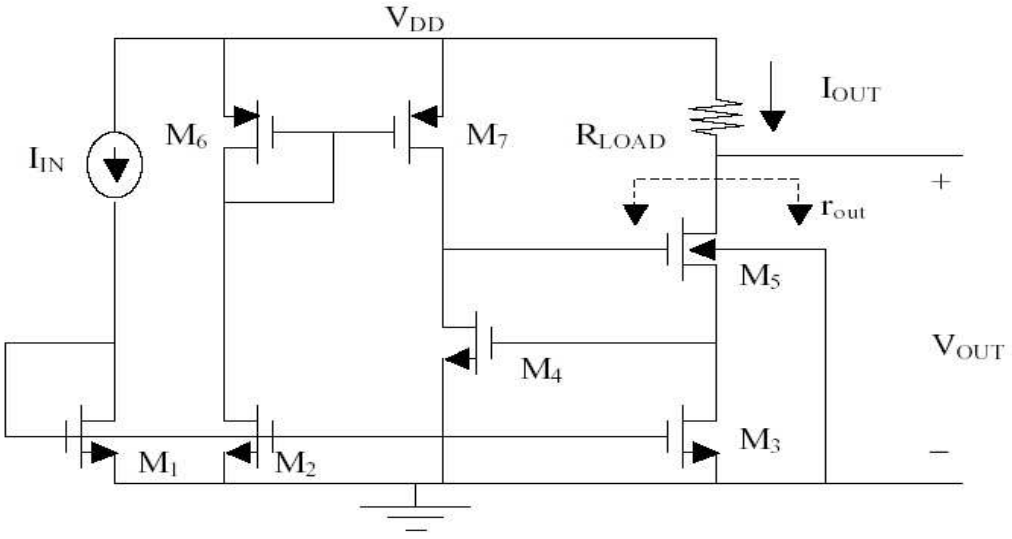

Fig.1 Regulated cascode current mirror

Device Models:

- Use the MOSIS AMI 0.6um technology (Run: N8BN), http://www.mosis.org/cgi-bin/cgiwrap/umosis/swp/params/ami-c5/n8bn-params.txt
- Assume this is an n-well process. Also, we can tie the well (body) of the PMOS device to the source.
- Nominal temperature T = 25^{O}C.

DESIGN AND REPORT REQUIREMENTS

1. Use a power supply voltage of 5V in your simulations. The quiescent DC power dissipation (with $I_{OUT} = I_{IN} = 100uA$) should be 5mW or less.
2. The nominal ration of I_{OUT} to I_{IN} must equal 1.00±0.01 for $25uA \leq I_{IN} \leq 200uA$. Over this range V_{OUT} should be greater than or equal to 2V.
3. The midband small-signal output resistance should be at least 10GΩ with I_{OUT} = 100uA and V_{OUT}= 2.5V. You must also perform an AC simulation of the small-signal output resistance with respect to frequency at this DC bias point and determine r_{out}'s –3dB bandwidth.

4. The minimum output voltage (V_{MIN}) at I_{OUT} = 100uA must be at least 1.5V. For the purposes of this design project, V_{MIN} will be considered the output voltage at which I_{OUT} falls to 95% of its nominal value.
5. The layout area of the amplifier must be less than 0.2mm^2. Use the following formula to determine the circuit area:

   Total area = 10 × (Area of all MOSFET gates)

   The areas of the R_{LOAD} resistor and the I_{IN} current source should not be considered in the calculation.

2. Design procedure

Obviously this circuit use negative feedback technique to stabilize the output current and boost the output impedance to a higher value, which is called "regulated cascade current mirror"[1]. If transistors M4 is not there, M3 and M5 form the conventional cascade current mirror. With the feedback through M4, the output impedance of this topology is similar to a triple cascode, without the expanse of voltage headroom. The transistors M4 and M5 make up the negative feedback loop, which stabilize Iout. If Iout were to increase, then since a constant bias of M3 due to the constant input current Iin, the voltage at the drain of M3 would rise, which in turn increase the current through M4. Since the current through is also constant, the voltage at the drain, or the gate of M5, would drease, thereby offsetting the increase in Iout by decreasing V_{GS5}.

Now we do some quantitive analysis on this circuit. The small-signal equivalent circuit of transistors M3, M4, M5 and M7 (which is treated as an idea current source), which is used to calculate the output impedance, is shown in Fig.2.

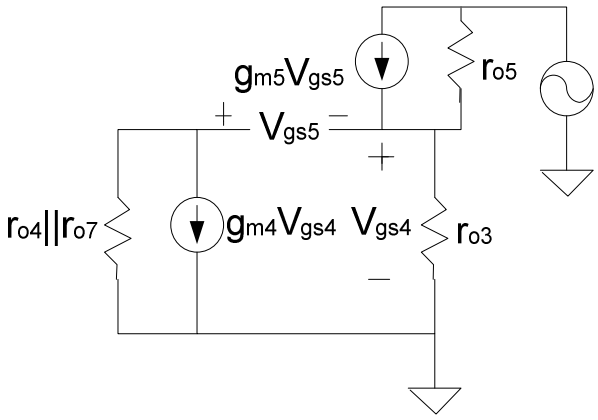

Fig.2 Small-signal test circuit to calculate the output impedance of the regulated cascode current mirror

$$V_{gs4} = i_t \cdot r_{o3} \tag{1}$$

$$V_{gs5} = -V_{gs4}[1 + g_{m4}(r_{o4} \parallel r_{o7})] = -i_t \cdot r_{o3}[1 + g_{m4}(r_{o4} \parallel r_{o7})] \tag{2}$$

$$i_t = g_{m5}V_{gs5} + \frac{v_t - V_{gs4}}{r_{o5}} \tag{3}$$

From (1), (2), (3), we can get:

$$R_{out} = \frac{V_t}{i_t} = g_{m4}(r_{o4} \parallel r_{o7}) g_{m5} r_{o3} r_{o5} \tag{4}$$

We can calculate the output impedance in another way. M4 and M7 form the feedback amplifier with gain of:

$$A_{fb} = g_{m4}(r_{o4} \parallel r_{o7}) \tag{5}$$

The output impedance of the cascoded transistor without feedback amplifier is:

$$R_{om3,5} = g_{m5} r_{o3} r_{o5} \tag{6}$$

With the feedback amplifier, the output impedance will be boosted by a factor of A_{fb}, then the output impedance will:

$$\boxed{R_{out} = A_{fb} \cdot R_{om3,5} = g_{m4}(r_{o4} \parallel r_{o7}) g_{m5} r_{o3} r_{o5} \approx \frac{g_m{}^2 r_o{}^3}{2}} \tag{7}$$

Now let's have a look at the relationship between the output impedance and bias current. We have:

$$r_o = \frac{1}{\lambda I_D} \tag{8}$$

$$g_m = \sqrt{2 u_n C_{ox} \frac{W}{L} I_D} \tag{9}$$

Plugging (8) and (9) into (7), we have:

$$R_{out} = \frac{u_n C_{ox} W}{L \lambda^3 I_D{}^2} \tag{10}$$

We can see that as the bias current (I_{out}) increases, the output impedance actually decreases! It means that if Rout meet the requirement at the highest bias current, which in this project is 100uA, then it will meet the requirement at low bias current.

We totally have 7 transistors, 2 PMOS and 5 NMOS. Let Wp=3Wn, all the transistors have same channel length, L, all the NMOS have channel width Wn, for PMOS Wp=3Wn. Then the total gate area is: (5Wn+2·3Wn)L=11WnL. For the upper limit of WnL, we have:

$$10 \cdot 11 WnL = 0.2 mm^2 = 2 \times 10^5 um^2 \tag{11}$$

$$WnL \le 1800 um^2 \tag{12}$$

Normally for good analog circuit, $L \geq 3L_{min}$, for a 0.6um technology, we can let $L \geq 2$um, for example, L=3um. For a large gm, we would like small L, but if L is very small, second order effects, for example, short channel effects, may play a big role, so r_o begins to decrease.

3. DC and AC simulations results

Following Fig.3 shows the test bench of the current mirror.

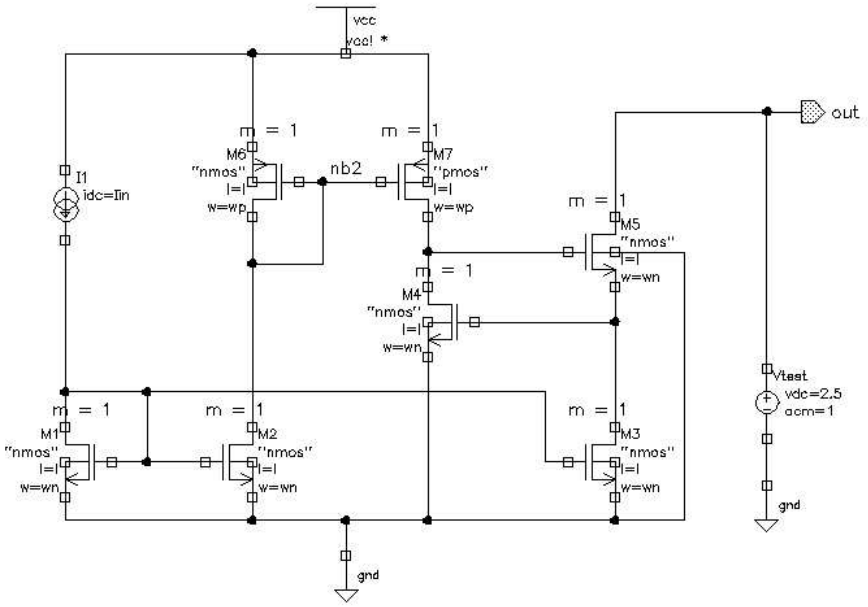

Fig.3 Simulation circuit of the regulated cascode current mirror

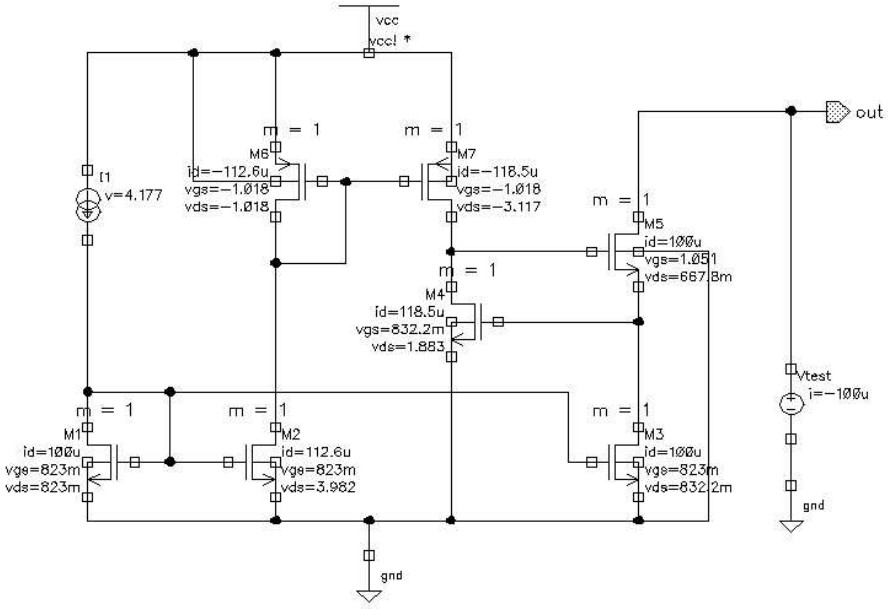

Fig.4 DC operating point of the current mirror

Fig.4 shows the DC operating point of this circuit with a bias current of 100uA. From Fig.4 we can find that all transistors operate in the saturation region, which is a basic requirement of this current mirror. We also can find that the total DC current is about 400uA. The power supply is 5V, so 400uA DC current corresponds to a power dispassion of 2mW, far below the design requirement of 5mW.

Next we test the input output current ratio. We swept the input current from 25uA to 100uA in about 1ms to see the output current. Fig.5 shows the results. It can be see that the current ratio is less than 0.6m, which is below the requirement of 0.01=10m.

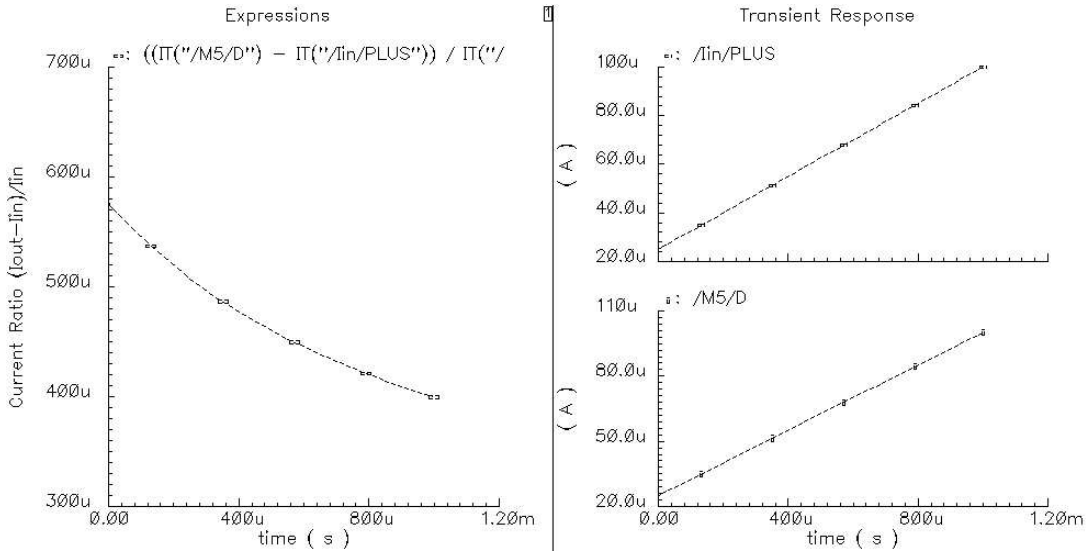

Fig.5 Input output current ratio

Now let's have a look at the output resistance. Fig.6 shows the simulated results using AC analysis with vout=1.5V. When vout=2.5V, the output resistance is even larger. It can be seen that when the bias current is larger, the output resistance is smaller. For this design, at Iin=100uA, the (DC) output resistance still can meet the requirement, which is 10GOhms. The -3 dB bandwidth is 36Hz for Iin=25 and 100Hz for Iin-100uA.

At last we also checked if the output voltage swing meets the specification or not. Simulations shows even when the output voltage is 1.5V and Iin=100uA, Iout=100.04uA, which is still very close to Iin.

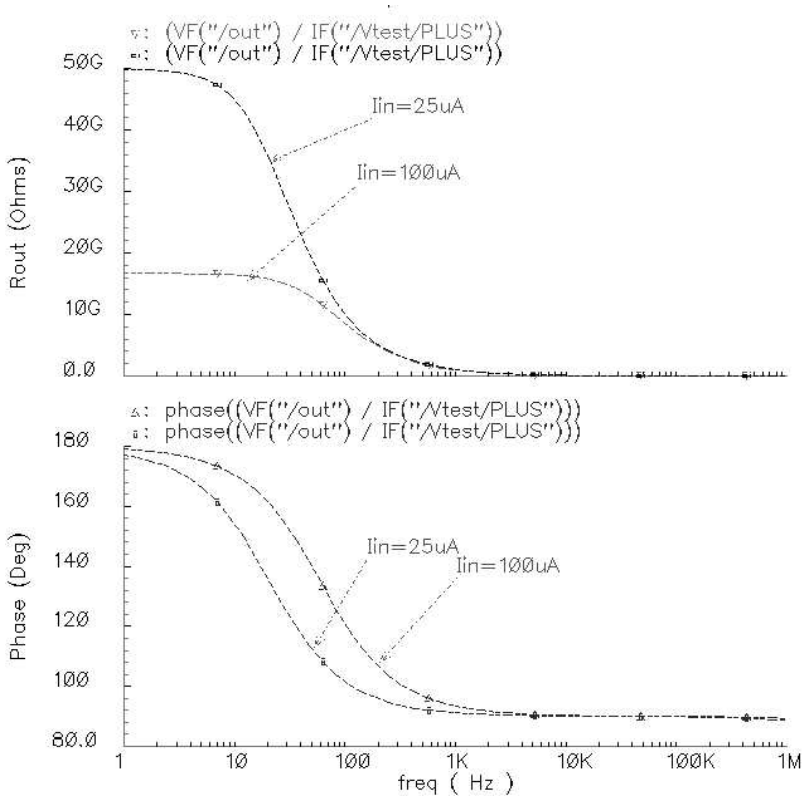

Fig.6 Simulation output impedance Rout of the regulated cascode current mirror

4. Schematics with device size, layout area

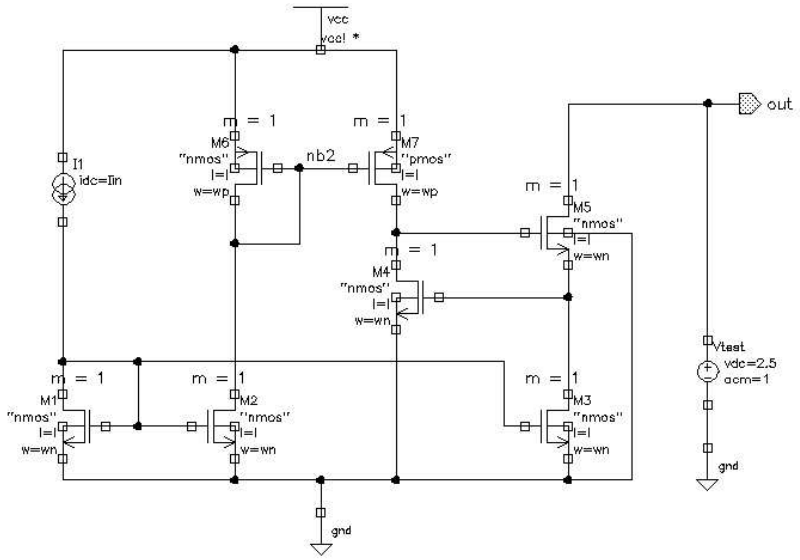

Fig.7 Schematic with device size

Fig.7 shows the device size, which are represented with parameters. All the NMOS transistors are of the same size L=3um and Wn=600um. The two PMOS transistors are of a size L=3um, and Wp=1800um. With these device sizes, the layout area of the circuitry is around 0.2mm^2.

5. Summary and Discussion

In this project, we first analyzed regulated cascode current mirror circuitry, derived the necessary equations for the design, and roughly estimated the transistor size. Then following this analysis, we successfully designed a regulated cascode current mirror with all requirements, power, Rout, Iin and Iout mismatch, area, met. See the following table.

Table.1 Summary of the designed regulated cascode current mirror circuitry

Item	Requirement	Design Value	Comments
Transistor size NMOS		W/L=600u/3u	
Transistor size PMOS		W/L=1800u/3u	
Ratio of Iout to Iin	<1.00+0.01	<1.000+0.001	
Rout	>10G Ohm	Much larger than 10G Ohm with all operation conditions	
Area	$<0.2mm^2$	$<0.2mm^2$	Depending on the application, the area can be reduced
Power	<5mW	2mV	
-3dB bandwidth	n/a	36 Hz (Iout=25uA) 100Hz (Iout=100ua)	Bandwidth can be improved based on appliaction

Every design is a trade off between performance, area, power etc. This design could be modified to meet different application requirements. For example, we could decrease the transistor size to improve the bandwidth at the expense of output resistance. The following figure shows the simulated results with vout=2.5V. We can see that when we decrease the transistor size from Wn/L=600u/3u to 300u/2u (Wp=3Wn), the output resistance decreases too, but with lot of bandwidth improvement.

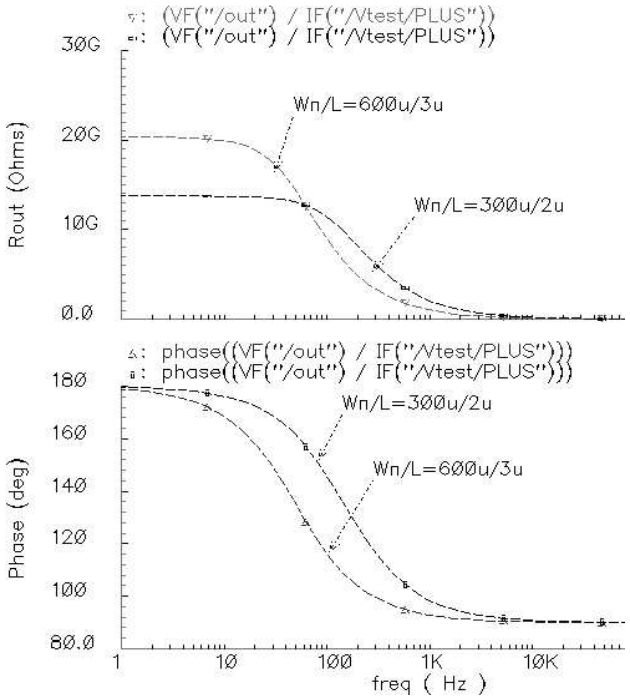

Fig.7 Bandwidth VS Transistor size

Reference

[1] R. Jacob Baker, Harry W. Wu, David E. Boyce, CMOS circuit design, layout, and simulation, IEEE Press, 1998, New York