

# Accurate low power bandgap voltage reference in 0.5μm CMOS technology

M.A.T. Sanduleanu, A.J.M. van Tuijl and R.F. Wassenaar

In mixed level applications, accurate voltage references are difficult to realise due to the lack of lateral *pnps* and the large offsets inherent to CMOS opamps. If low power is essential, the accuracy is mainly impaired by the increased offset of the opamps. It is shown that by using chopping techniques, the accuracy of a bandgap voltage reference can be improved by about ten times without laser trimming, with the added benefit of reducing the  $1/f$  noise of the amplifier.

**Introduction:** The voltage of a bandgap reference is based on the bandgap voltage  $V_{gap0}$  of a semiconductor: a well defined, temperature independent, physical value. In submicron CMOS digital processes, the lack of lateral *pnps* can be seen as a disadvantage. Without these components, we must rely on the well-known solution for a bandgap reference as shown in Fig. 1a, which requires the use of an opamp. In bipolar technologies, simple solutions for voltage references have been considered [1, 2]. For CMOS processes the large offset of the opamp will reduce the accuracy of the output voltage  $V_0$ . To achieve better accuracy, laser trimming is a well-known solution although an expensive one. At low currents, the offset increases, and the challenge would be the realisation of a low power and accurate bandgap voltage reference in CMOS without laser trimming techniques. Furthermore, the available area is limited, so obtaining better resistor matching by increasing the area is not an option.

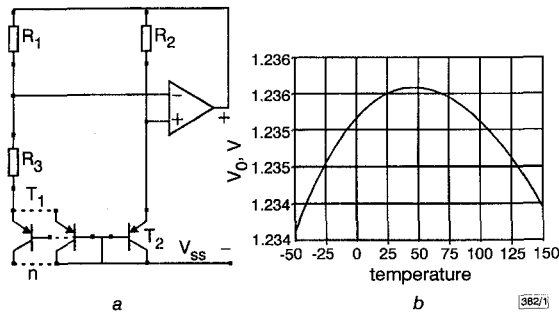


Fig. 1 Basic bandgap reference and plot of eqn. 1

a Bandgap reference  
b Plot of eqn. 1  
 $R_1 = R_2 = 113\text{K}$ ,  $R_3 = 16.2\text{K}$

**Principle:** In Fig. 1b, the output voltage  $V_0$  can be related to the absolute temperature by

$$V_0(T) = V_{gap0} + \frac{kT}{q}(\gamma - 1) \left[ 1 - \ln\left(\frac{T}{T_0}\right) \right] \quad (1)$$

$V_{gap0}$  denotes the extrapolated bandgap voltage of a semiconductor,  $\gamma$  is the mobility temperature exponent of the charge carriers in a bipolar transistor and  $T_0$  is the reference temperature. This condition holds true for a well chosen resistance ratio  $R_1/R_3$ . If  $n$  is the ratio between the emitter areas of  $T_1$  and  $T_2$ ,  $U_T$  is the thermal voltage  $kT/q$  and  $C_1$  is a process constant, then:

$$\frac{R_1}{R_3} = \frac{1}{\ln n} \left[ (\gamma - 1) - \ln\left(\frac{U_T \ln n}{C_1 R_3 T T_0^{\gamma-1}}\right) \right] \quad (2)$$

In Fig. 1b, a plot of eqn. 1 centred around  $T_0 = 50^\circ\text{C}$  is shown. The accuracy of the output voltage, at the reference temperature  $T_0$ , depends on the process spread, offset voltage of the opamp and matching of the resistors. Consider the deviation of the output voltage from the nominal voltage ( $\Delta V_0$ ) owing to the deviation of the resistances and the offset of the opamp  $V_{off}$ . To reduce the ratio between  $R_1$  and  $R_3$ , the transistor  $T_1$  is made from  $n$  identical transistors as shown in Fig. 1a.  $R_N$  denotes nominal values,  $R$  the actual values of the resistors and  $U_T$  the thermal voltage. The absolute error of the reference voltage is given by

$$\Delta V_0 = -U_T \frac{\Delta R_3}{R_{3N}} + U_T \frac{R_{1N}}{R_{3N}} \left[ \frac{\Delta R_1}{R_1} (1 + \ln n) - \frac{\Delta R_2}{R_2} \ln n \right]$$

$$+ V_{off} \left( 1 + \frac{1}{\ln n} + \frac{R_{1N}}{R_{3N}} \right) \quad (3)$$

The first term is generated by the process spread of  $R_3$ . The second term comes from the mismatches of the resistors  $R_1$  and  $R_2$ . The last term is generated by the offset of the opamp. We can now find the spread of the output voltage  $\sigma^2(V_0)$  as a function of the individual terms  $\sigma_{1..4}$ .

$$\sigma^2(V_0) = \sigma_1^2 + \sigma_2^2 + \sigma_3^2 + \sigma_4^2 \quad (4)$$

where

$$\begin{aligned} \sigma_1^2 &= U_T^2 \sigma^2 \left( \frac{\Delta R_3}{R_3} \right) \\ \sigma_2^2 &= \left[ (1 + \ln n) U_T \frac{R_{1N}}{R_{3N}} \right]^2 \sigma^2 \left( \frac{\Delta R_1}{R_1} \right) \\ \sigma_3^2 &= \left[ \frac{U_T R_{1N}}{R_{3N}} \ln(n) \right]^2 \sigma^2 \left( \frac{\Delta R_2}{R_2} \right) \\ \sigma_4^2 &= \left( 1 + \frac{1}{\ln n} + \frac{R_{1N}}{R_{3N}} \right)^2 \sigma^2(V_{off}) \end{aligned} \quad (5)$$

Comparing  $\sigma_{1..4}$  in eqn. 5, the dominant term by far is  $\sigma_4$ . For a resistor ratio  $R_{1N}/R_{3N}$  of  $\sim 7$  the opamp offset voltage spread  $\sigma^2(V_{off})$  is amplified  $\sim 70$  times. An offset of 3.8mV gives a spread in  $V_0$  of 32mV. Hence, in order to achieve better accuracy, it should be possible to decrease the offset of the opamp.

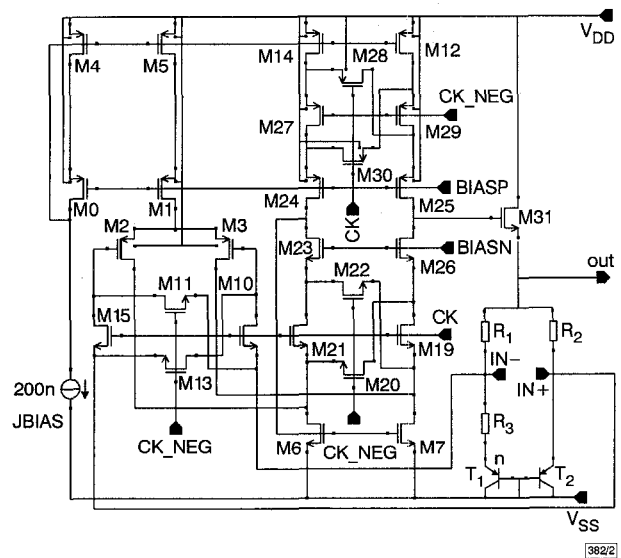


Fig. 2 Bandgap reference with chopped amplifier

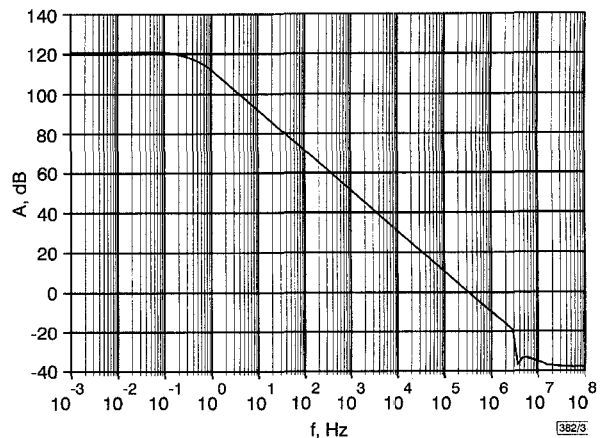


Fig. 3 Open loop gain of opamp

**Accuracy improvement:** Fig. 2 shows a version of the bandgap reference based on the principle shown in Fig. 1a with a chopped opamp. The voltage difference between the nodes IN- and IN+ is applied to the input chopper. M10, M11, M13 and M15. The offset of the input pair M2, M3 and the offset of the mirror M6 and M7 is cancelled out in the second chopper, M19, M20, M21 and

M22. The offset of the current sources M12 and M14 is eliminated by transposition at the third chopper M27, M28, M29 and M30. The source follower M31 provides the output voltage  $V_o$ , which is bandgap referenced. Simulation shows that the spread of the opamp offset without chopping is 3.8mV ( $1\sigma$ ). With chopping at 10KHz, the offset is reduced to 10 $\mu$ V ( $1\sigma$ ). The current consumption of the opamp is 3 $\mu$ A from a 2.5V power supply voltage. Fig. 3 shows the open loop gain of the opamp. The low frequency gain is 120dB, the gain-bandwidth product of the opamp is 300kHz and the phase margin is 74°. The resistors  $R_1$ ,  $R_2$  and  $R_3$  are polysilicon resistors with a low temperature coefficient. To decrease the spread, parallel-series configurations of equal sized resistors have been used. The area of the circuit is ~0.035mm<sup>2</sup>, being dominated by resistor area. Without chopping, the cumulative effect of the spread contributions gives 32mV ( $1\sigma$ ) spread at the output. Chopping, reduces the total spread to 3.2mV ( $1\sigma$ ). The accuracy can be increased, in principle, by increasing the area of the resistors. Simulations show when the area is increased 16 times, the spread of the reference voltage is 1.8mV ( $1\sigma$ ). The bias current can be derived from the bandgap referenced output. To prevent the zero solution of the output voltage, we need to add a start-up circuit. The total power consumption of the circuit is 7.5 $\mu$ W.

*Noise properties:* Owing to the low current levels, the transconductance of the input stage of the opamp is low and the noise properties of the bandgap are dominated by the opamp white noise. The  $1/f$  noise is reduced by the chopping mechanism [3] and therefore the power spectral density of the noise at the output depends on the noise properties of the opamp.  $NEF$  denotes the noise excess factor of the opamp and  $r_D$  the incremental resistance of the diode connected transistor  $T_1$ . The power spectral density of the output noise can be approximated with

$$S_{V_o} \approx \frac{8kT}{g_{m2}} NEF \left( 1 + \frac{R_1}{r_D + R_3} \right)^2 \quad (6)$$

The closed loop bandwidth is 30kHz and the RMS value of the integrated voltage noise in this frequency band is ~67 $\mu$ V RMS for an opamp noise excess factor  $NEF$  of 2.2.

*Conclusions:* An accurate, low power bandgap voltage reference has been presented. It is shown that the offset of the opamp dominates the precision of the bandgap voltage reference. Hence, for low current applications, it should be possible to decrease the offset of the opamp. Using chopping techniques, the precision of the output voltage is 3.2mV ( $1\sigma$ ). Without chopping, the accuracy would have been 32mV ( $1\sigma$ ). The total power consumption is 7.5 $\mu$ W. The power needed for chopping is negligible.

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## References

- 1 VAN STAVEREN, A., VAN VELZEN, J., VERHOEVEN, C.J.M., and VAN ROERMUND, A.H.M.: 'An integratable second-order compensated bandgap reference for 1V supply', *Analog Integr. Circuits Signal Process.*, 1995, (8), pp. 69–81
- 2 GUNAWAN, M.: 'A curvature-corrected low-voltage bandgap reference', *IEEE J. Solid-State Circuits*, 1993, **SSC-28**, pp. 667–670
- 3 SANDULEANU, M.A.T., NAUTA, B., and WALLINGA, H.: 'Low-power low-voltage chopped transconductance amplifier for noise and offset reduction'. Proc. 23rd European Solid-State Circuits Conf., October 1997, pp. 204–207

## Electron trapping in Si implanted SIMOX

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The implantation and annealing processes of SIMOX fabrication may result in excess silicon atoms located in the buried oxide. These excess silicon atoms have been postulated by various researchers to be responsible for the formation of silicon clusters and associated defects in SIMOX [1–3]. This work was performed to test this postulate. These defects result in a higher refractive index [4], an increase in the number of electron traps, and the production of traps with very large capture cross-sections. It is also known that excess silicon introduced by ion implantation creates electron traps in thermal oxides [5, 6]. This work supports the above postulate by implanting a large range of silicon concentrations into low defect multiple implant SIMOX and measuring the resulting electron traps by the avalanche injection technique.

Silicon-on-insulator (SOI) technology is becoming increasingly important for ultra-large-scale integration. SOI technology offers increased speed (owing to reduced capacitance) dielectric isolation (prevents latch-up), high temperature operation, higher packing density, and enhanced performance in radiation environments. The leading SOI technology is separation-by-implantation-of-oxygen (SIMOX) because the SIMOX process offers better control of top silicon thickness uniformity. However, the performance of devices fabricated in the top silicon layer is highly dependent on the electrical properties of the buried oxide (BOX).

Oxide degradation due to charge trapping, interface state generation, and bulk trap generation influences SIMOX BOX reliability. Oxide trapped charge is associated with defects in the oxide. It has been speculated that the implantation and annealing processes leave behind clusters of silicon atoms and associated defects. It has been reported that these silicon clusters could result in traps with very large cross-sections. In an effort to reduce or eliminate these traps, supplemental oxygen atoms have been implanted into the buried oxide with some success. This Letter supports the proposition that silicon clusters are indeed the cause of electron traps in SIMOX. The approach taken to test this hypothesis was to fabricate SIMOX wafers with a low electron trap density, implant Si atoms, and measure electron trap densities and cross-sections in the control and Si implanted wafers. Low electron trap SIMOX wafers were fabricated by the multiple implantation of oxygen. Avalanche electron injection was used to determine the trap densities and capture cross-sections in the SIMOX buried oxide.

The buried oxide was formed by multiple implantation of oxygen at doses of  $5 \times 10^{17}$ ,  $5 \times 10^{17}$ , and  $8 \times 10^{17}$  cm<sup>-2</sup> respectively at 190keV, followed by a 1310°C anneal for 5h in an Ar plus 0.5% oxygen ambient for each implantation. The virgin silicon wafer was  $p$ -type with a resistivity of 10 $\Omega$ cm. The resulting oxide was ~350nm thick with a top silicon layer 200nm thick as determined by spectroscopic ellipsometry [7]. Five low defect samples received doses of  $1 \times 10^{15}$ ,  $3 \times 10^{15}$ ,  $1 \times 10^{16}$ ,  $3 \times 10^{16}$ , and  $1 \times 10^{17}$  cm<sup>-2</sup> Si respectively, implanted at 190keV, followed by a one hour anneal in a 100% Ar ambient. For avalanche injection purposes the top silicon for both the control and low defect SIMOX received a  $2 \times 10^{12}$  cm<sup>-2</sup> boron implant at 40keV, resulting in a doping density of ~ $10^{17}$  cm<sup>-3</sup>. This highly doped silicon layer is required to avoid edge injection effects, to lower the silicon breakdown voltage, and to lower the field across the oxide during injection [8]. Capacitors with areas of 0.0456 and 0.05cm<sup>2</sup> were fabricated by depositing aluminium dots on the top silicon. A hydrazine etch was used to form isolated silicon mesa structures.

Electron trap density was evaluated using avalanche electron injection. In this procedure electrons in the depletion region of the superficial layer are formed into an avalanche plasma and are injected into the oxide. The carrier injection rate is controlled by varying the applied voltage and repetition rate of the exciting gate pulse. The injection was performed using a constant current technique with a saw tooth waveform at 50kHz. The amplitude of the saw tooth waveform was automatically adjusted to maintain a constant, preset current density in the oxide. Electron trapping was monitored by stopping the injection at intervals to plot a C-V curve and to record the data in a computer. Trapped charge results in a change in the surface potential and a corresponding shift in the C-V curve. For electron injection the C-V curve shift is positive. Data collection on the change in mid-gap voltage as a