PRELIMINARY

QF4A512

4-Channel Programmable Signal Converter (PSC)

APPLICATIONS

- **Industrial Control**
- **Machine Monitoring**
- **Smart Sensors**
- **Medical Monitoring and Diagnostics**
- **Industrial Wireless Sensor Networks**
- **Homeland Security**

DESCRIPTION

The QF4A512 Programmable Signal Converter is a 4-channel, signal conditioner and signal converter. Each channel can be individually programmed for the gain, anti-aliasing filter cutoff frequency, A-to-D sampling frequency, and unique filter requirements. This is accomplished with 4 separate high-precision 512-tap FIR filters.

Quickfilter Pro software has been created for rapid device configuration and filter design at performance levels unattainable with analog components.

ORDERING INFORMATION

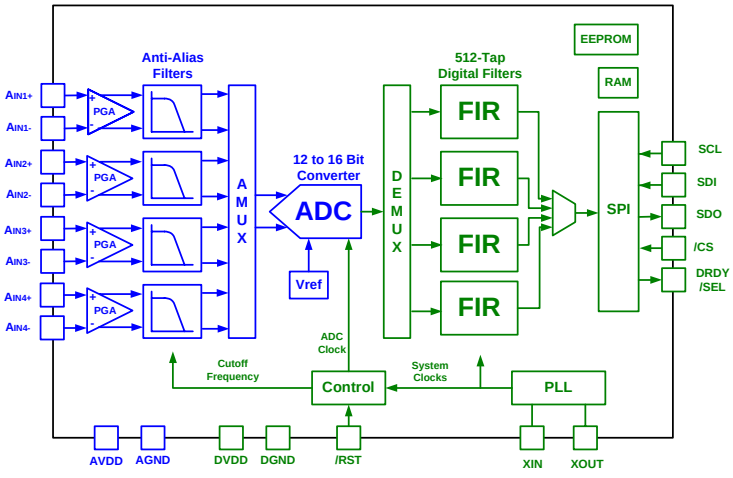
Device	Package
QF4A512ALQ--T QF4A512ALQ--B	32-Pin LQFP - Tape & Reel (Reel qty 1000) - Trays
QF4A512-DK	Development Kit

FEATURES

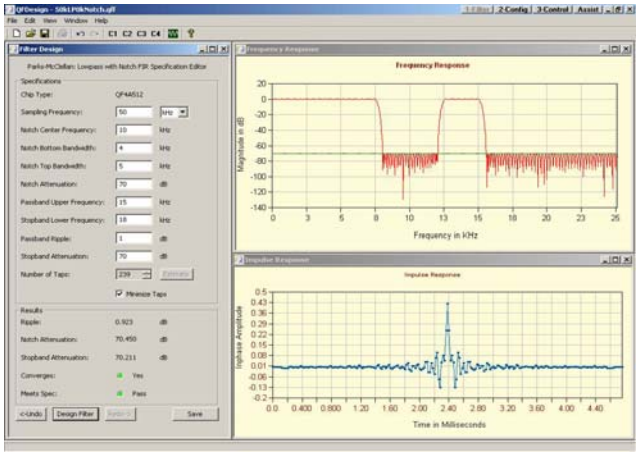
- **4 Channel Analog Differential or Single Ended Inputs**
- **4 Programmable (1x, 2x, 4x, 8x) Gain Amplifiers**
- **Anti-Aliasing Filter Per Channel, 3rd Order Bessel**
- **16-bit Programmable A/D Converter**
- **Internal Precision Voltage Reference**
- **4 Individual Programmable 512-tap Digital FIR Filters**
- **SPI Port Interface**
- **3.3V Digital I/O, 5 Volt Tolerant**
- **4K Byte EEPROM for filter coefficient, chip configuration and calibration.**
  - 128 bytes of EEPROM User Data Space
  - 384 Bit Masks for IEEE 1451.4 TEDS on 4 Channels
- **3.3V & 1.8V Supplies**
- **Industrial Temp -40C to +85C**
- **32-Pin LQFP Package**

QUICKFILTER DEVELOPMENT KIT (QF4A512-DK)

- **Quickfilter Pro Windows®-based Software for Rapid Filter Design and IC Configuration**
- **In-System Programmability (ISP) trough SPI Port**
- **Evaluation board for verification of device performance**



Functional Block Diagram



Filter Design Screen

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1. SPECIFICATIONS

1.1 Absolute Maximum Ratings

Stresses above those listed under Absolute Maximum Ratings can cause permanent device failure. Functionality at or above these limits is not implied. Exposure to absolute maximum ratings for extended periods may affect device reliability.

Parameter	Min	Max	Units
Storage Temperature	-60	125	ºC
Supply Voltage, V_{DD18} to DGND	-0.2V	2.2V	V
Supply Voltage, V_{DD33} with respect to DGND	-0.2V	4.0V	V
Digital Input Voltage with respect to DGND - XIN	-0.3	2.5	V
Digital Input Voltage with respect to DGND – all others	-0.3	7	V
Analog Input Voltage with respect to AGND	-0.3	V_{DD33} + 0.3	V
ESD Immunity (Human Body Model, JESD222 Class 1C))	1000		V

This integrated circuit can be damaged by ESD. Quickfilter Technologies recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

1.2 Package Assembly

The QF4A512 is offered in a “green” package (RoHS & no Sb/Br), assembled with enhanced environmentally compatible Pb-free and halide-free materials. The leads possess a matte-tin plating which is compatible with conventional board assembly processes or newer lead-free board assembly processes. The peak soldering temperature should not exceed 260°C during printed circuit board assembly.

1.3 Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Supply Voltage 1.8	V_{DD18}	1.6	1.8	2.0	V
Supply Voltage 3.3	V_{DD33}	3.0	3.3	3.6	V
Digital Input Voltage	XIN	0		2	V
	all others	0		5.5	V
Analog Input Voltage	A_{IN}	0.2		2.5	V
Clock Frequency	f_0	5	20	100	MHz
Ambient Temperature	T_A	-40	25	85	ºC
ADC Clock Rate	f_{ADC}			100	MHz

Note: Quickfilter guarantees the performance of this device over specified ranges by conducting electrical characterization over each range and by conducting a production test with single insertion coupled to periodic sampling.

1.4 Electrical Characteristics

Symbol	Parameter (Condition)	Min	Typ	Max	Units	Note
Resolution						
N	Resolution, Nominal	16			Bits	
NMC	No Missing Codes Guaranteed	16			Bits	
DC Accuracy						
PSRR	Power-supply rejection ratio		tbd		dB	
G_{ERR}	Gain Error (Uncalibrated)			1	%FSR	1
V_{OS}	DC Offset Error (Uncalibrated) - Chopper Off - Chopper On		±10	 ± 0.01	mV	1
V_{REF}	Internal Voltage Reference	TBD	1.2	TBD	V	
TCV_{REF}	Internal Voltage Reference Drift over temp		100		ppm/°C	2
INL	Integral Non-linearity (PGA = x1)			0.02	%FS	
DNL	Differential Non-linearity (PGA = x1)			1	LSB	
AC Accuracy						
SNR	Signal To Noise Ratio, f_S = 2kHz f_S = 20kHz f_S = 200kHz f_S = 2MHz		82 81 77 69		dBFS	3
SINAD	Signal To Noise and Distortion, f_S = 2kHz f_S = 20kHz f_S = 200kHz f_S = 2MHz		81 80 76 69		dBFS	3
SFDR	Spurious Free Dynamic Range, f_S = 2kHz f_S = 20kHz f_S = 200kHz f_S = 2MHz		89 88 88 87		dBc	3
THD	Total Harmonic Distortion, f_S = 2kHz f_S = 20kHz f_S = 200kHz f_S = 2MHz		-89 -88 -85 -83		dBc	3
ENOB	Effective number of bits f_S = 2kHz f_S = 20kHz f_S = 200kHz f_S = 2MHz		13.2 13.0 12.4 11.2		Bits	3
Analog Inputs						
V_{FSR}	Input Differential Voltage Range		1.6	2.0	V_{P-P}	
V_{CM}	Input Common Mode Voltage Range	0.2	1.2	2.5	V	
CMRR	Common Mode Rejection Ratio		55		dB	
C_{IN}	Input Capacitance (Single Ended)		5		pF	
R_{IN}	Input Resistance (Single Ended)	9.2	10.0	10.8	kΩ	

	Differential Input Capacitance		10		pF	
	Differential Input Resistance	4.6	5	5.4	kΩ	
AV_PB	Passband Attenuation (DC to 500 kHz)			0.2	dB	
GD	Group Delay Variation (DC to 500 kHz)			5	%	
CI	Channel Isolation, f_{ADC} = 50MHz f_{ADC} = 100MHz		75 35		dBc	
AN	Alias Noise Attenuation	45			dB	
	Anti-aliasing Filter Cutoff Frequency, aaf_freq=0 aaf_freq=1			500 3	kHz MHz	
Supply Current & Power Dissipation						
I_{DD18}	1.8V Supply Operating Current - f_S = 1kHz (four channels) - f_S = 100kHz (four channels) - f_S = 2.5MHz (single channel) - Standby - Power down		98 129 147 1.1 0.5		mA	4
I_{DD33}	3.3V Supply Operating Current - f_S = 1kHz (four channels) - f_S = 100kHz (four channels) - f_S = 2.5MHz (single channel) - Standby - Power Down		17 17 4.3 0.6 0.2		mA	4
P_{DD}	Power Dissipation, Active - Single channel, f_S = 100kHz - Standby - Power Down		87 4 1.6		mW	4
Digital Inputs (SCLK, SDI, /CS, /RST) †						
V_{IH}	High-level Input Voltage, DV_{DD33} = 3.6V	2		5.5	V	
V_{IL}	Low-level Input Voltage, DV_{DD33} = 3.0V	-0.3		0.8	V	
I_{IN}	Input (leakage) current (SCLK, SDI)		tbd		nA	
R_{IN}	Pull-up Resistance (/CS, /RST) Pull-down Resistance (DRDY)		31		kΩ	
C_{IN}	Input Capacitance		tbd		pF	
Digital Input (XIN)						
V_{IH}	High-level Input Voltage, DV_{DD18} = 2.0V	1.4		2	V	
V_{IL}	Low-level Input Voltage, DV_{DD18} = 1.6V	0		0.4	V	
I_{IN}	Input (leakage) current		tbd		nA	
C_{IN}	Input Capacitance		tbd		pF	
Digital Outputs (SDO, DRDY/SEL) †						
V_{OH}	High-level Output Voltage, DV_{DD33} = 3.0V, I_{OH} = -100uA	2.8			V	
V_{OL}	Low-level Output Voltage, DV_{DD33} = 3.0V, I_{OL} = 100uA			0.2	V	
C_O	Output Capacitance		tbd		pF	
C_L	Load Capacitance			30	pF	
Digital Output (XOUT)						

V_{OH}	High-level Output Voltage, DV_{DD18} = 1.6V, I_{OH} = -100uA	1.4			V	
V_{OL}	Low-level Output Voltage, DV_{DD18} = 2.0V, I_{OL} = 100uA			0.2	V	
C_O	Output Capacitance		tbd		pF	
C_L	Load Capacitance			20	pF	

1. System calibration will reduce these errors to below the noise level.
2. System calibration at any temperature will eliminate this error.
3. Programmable Gain Amplifier set at a gain of x1, $f_{IN} = f_s / 25$
4. Standby is with all channels inactive, and analog front end turned off. Power down is when the oscillator/PLL is turned off.

† The digital input and output pins (except XIN & XOUT) are 5V-tolerant. Inputs may be driven with 5V signals, outputs can be connected via pull-ups to 5V levels.

Note: Current device revision is QF4A512A. Only difference between this revision and previous revisions is a reduction in standby power (P_{DD}) and correct implementation of the ADC overflow flags (Section 10.3)

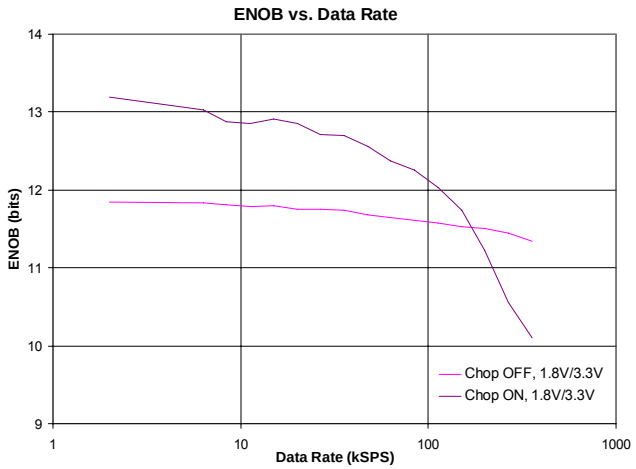
1.5 Timing Requirements

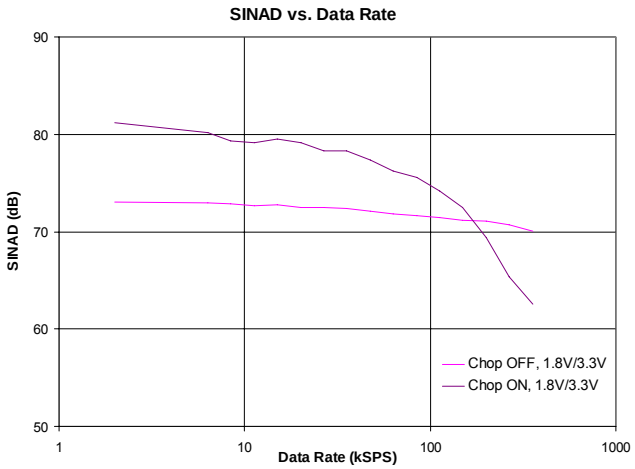
Parameter	Min	Max	Units	Note
Input Clock Frequency, f_0	5	100	MHz	
Serial Port Clock Frequency, f_{SCLK} (Run and Configure Modes)		40	MHz	
Serial Port Clock Frequency, f_{EE} (EEPROM Mode)		5	MHz	
PLL Clock Frequency, PLL_CLK	20	200	MHz	
Chip select low pulse width	2/SYS_CLK		ns	
SYS_CLK frequency (User filters, sampling rates)	$(((N_{TAPS} + 1)/2)+1)*f_S$	PLL_CLK		5, 8
SYS_CLK frequency (Fixed G and H filters)	103* f_S	PLL_CLK		6, 8
SYS_CLK frequency (relative to SCLK) - 16-bit output - 24-bit output	3*SCLK/16 SCLK/(8*N)	PLL_CLK		7, 8
Setup time, Chip Select (/CS) low to SCLK↑	tbd		ns	
Setup time, SDI before SCLK↑	tbd		ns	
Hold time, SDI after SCLK↑	tbd		ns	

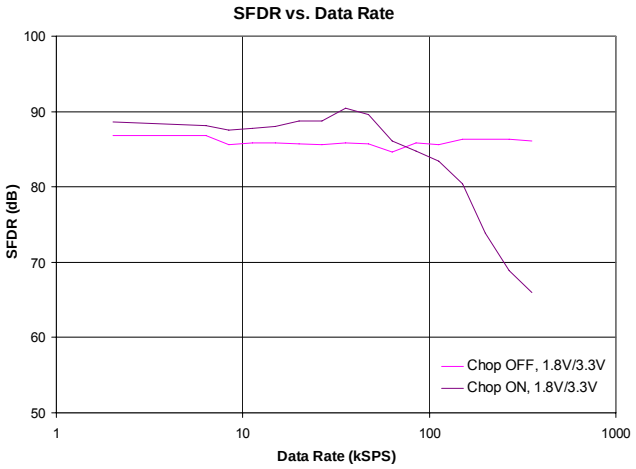
5. f_S is the sampling rate for any given channel and N_{TAPS} is the number of taps used in the associated FIR. The highest value of the expression for any active channel defines the minimum frequency for SYS_CLK.
6. This parameter is derived in similar fashion to the previous one and is determined by the fixed number of taps used in the G and H filters.
7. This limit is caused by the requirement for DRDY to be cleared before /CS returns to a high level after a data transfer. Two SYS_CLKS are required to clear DRDY this must occur before the data transfer is completed. N is the number of channels active in the output data.
8. All three of the minimum conditions must be satisfied for correct device operation.

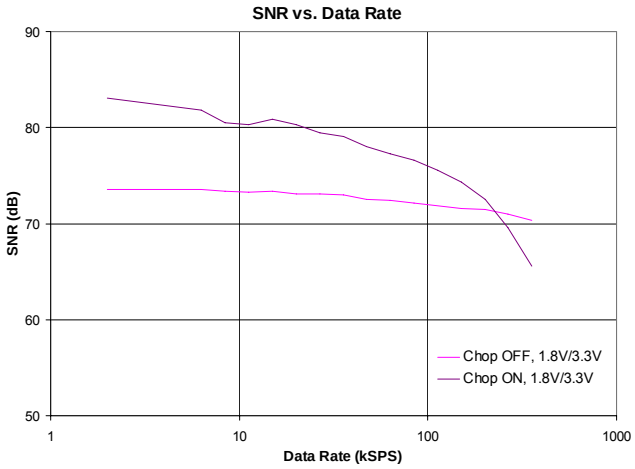
1.6 Typical Performance Characteristics

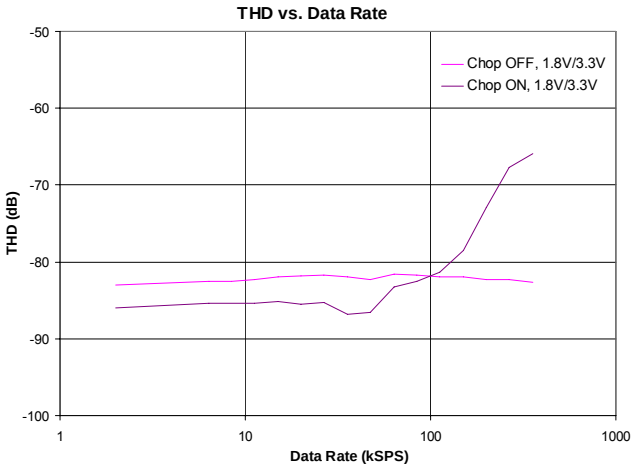
Default Conditions: T_A = 25 C, V_{DD18} = 1.8V, V_{DD33} = 3.3V, unless otherwise noted.

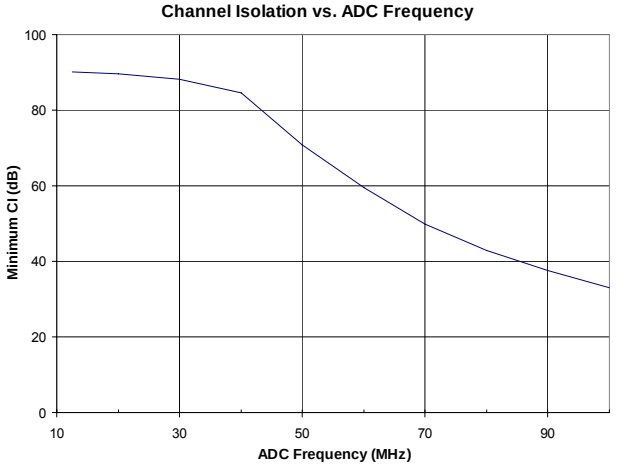


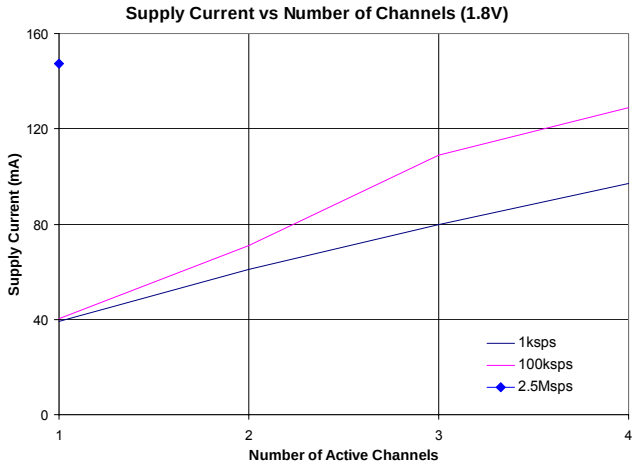


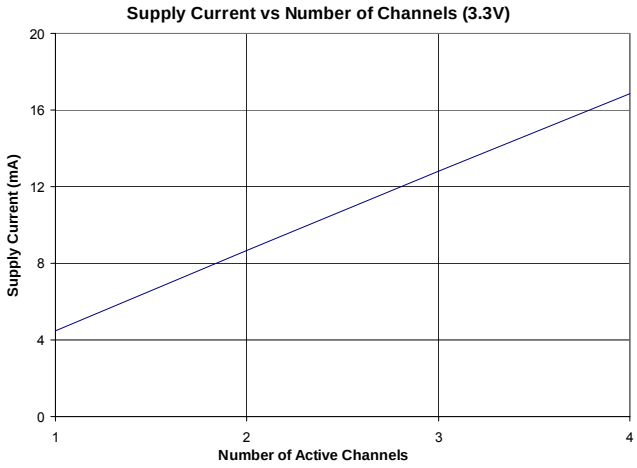






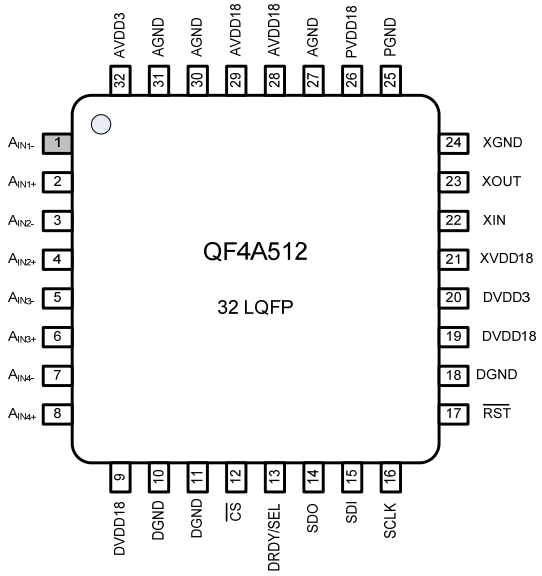






2. PINOUT and PIN DESCRIPTIONS

2.1 Pinout



2.2 Pin Descriptions

Pin #	Pin Name	Type	Description
1	A_{IN1-}	Input	Analog Input Channel 1 Differential-, or DC bias input (SE)
2	A_{IN1+}	Input	Analog Input Channel 1, Single-Ended or Differential+ (No phase shift)
3	A_{IN2-}	Input	Analog Input Channel 2 Differential-, or DC bias input (SE)
4	A_{IN2+}	Input	Analog Input Channel 2 , Single-Ended or Differential+ (No phase shift)
5	A_{IN3-}	Input	Analog Input Channel 3 Differential-, or DC bias input (SE)
6	A_{IN3+}	Input	Analog Input Channel 3, Single-Ended or Differential+ (No phase shift)
7	A_{IN4-}	Input	Analog Input Channel 4 Differential-, or DC bias input (SE)
8	A_{IN4+}	Input	Analog Input Channel 4, Single-Ended or Differential+ (No phase shift)

9	DV_{DD18}	Power	+1.8V DC Power (Digital)
10	DGND	Ground	Digital Ground
11	DGND	Ground	Digital Ground
12	/CS	Input	Chip Select from SPI Bus (Low logic selects chip). Internal pull-up.
13	DRDY/SEL	Input/Output	High when new data is ready, if pulled high accesses EEPROM direct. Internal pull-down.
14	SDO	Output	SPI Serial Data Output
15	SDI	Input	SPI Serial Data Input
16	SCLK	Input	SPI Clock (Maximum 40 MHz)
17	/RST	Input	Chip RESET (Low logic resets chip). Internal pull-up.
18	DGND	Ground	Digital Ground
19	DV_{DD18}	Power	+1.8V DC Power (Digital)
20	DV_{DD33}	Power	+3.3V DC Power (Digital)
21	XV_{DD18}	Power	Filtered +1.8V DC Power for Internal Oscillator
22	XIN	Input	Crystal connection or external clock input (10-20 MHz)
23	XOUT	Output	Crystal connection (10-20 MHz)
24	XGND	Ground	Ground for Internal Oscillator
25	PGND	Ground	Ground for Phase Lock Loop
26	PV_{DD18}	Power	+1.8V DC Filtered Power for Phase Lock Loop
27	AGND	Ground	Analog Ground
28	AV_{DD18}	Power	+1.8V DC Power (Analog)
29	AV_{DD18}	Power	+1.8V DC Power (Analog)
30	AGND	Ground	Analog Ground
31	AGND	Ground	Analog Ground
32	AV_{DD33}	Power	+3.3V DC Power (Analog)

3. GENERAL DESCRIPTION

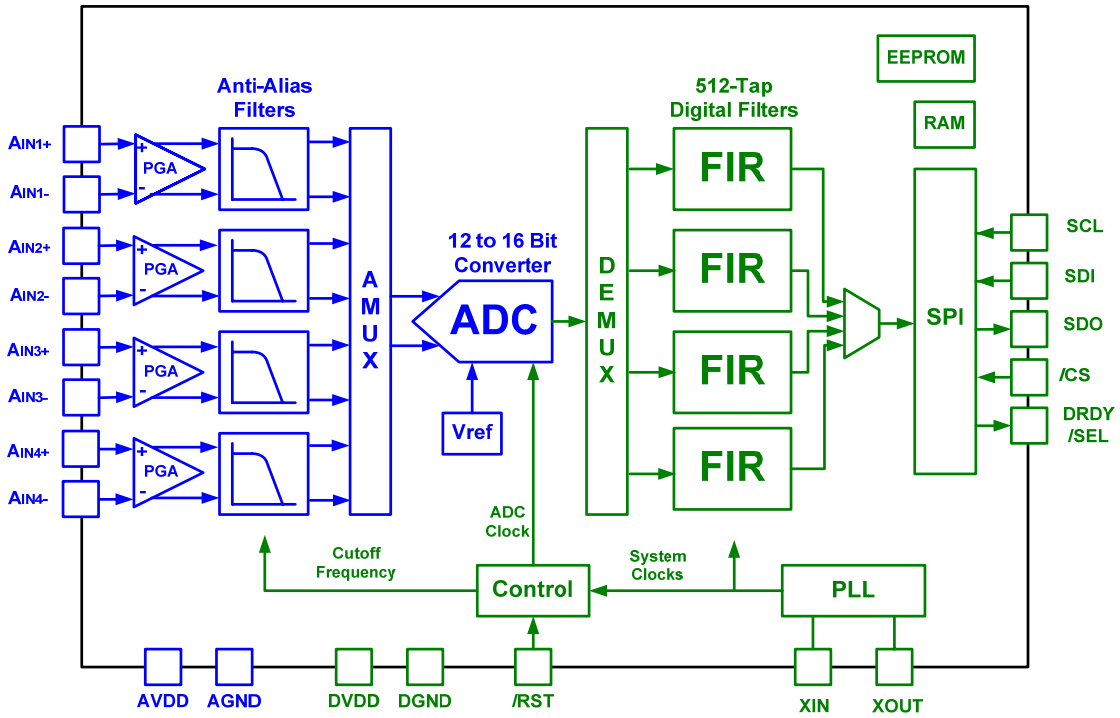


Figure 1. Functional Block Diagram

3.1 Analog Front End (AFE)

The AFE consists of a Programmable Gain Amplifier (PGA), a chopper-stabilized amplifier and an Anti-Aliasing Filter.

Programmable Gain Amplifier (PGA)

The PGA can be set at gains of 1X, 2X, 4X, and 8X. The input impedance of the PGA is 10kΩ on both the positive and negative inputs. The PGA can be configured as either single ended or differential and can receive inputs of up to 2.0V p-p directly. With a single scaling resistor in each channel, two if configured differentially, the PGA can receive signals of up to +/- 10Vp-p or higher.

Chopper-stabilized Amplifier (not shown in diagram)

This circuit minimizes correlated (1/f) noise and dc offset within the chip. For sampling rates less than 200kHz this circuit will maximize signal-to-noise performance, and hence SINAD and ENOB. (see Section 6.2)

Anti-Aliasing Filter (AAF)

The Anti-Aliasing Filter is designed to reject frequencies that are higher than the band of interest. If those frequencies are sent to the ADC, they can alias back into the band of interest and can cause erroneous readings to result. The AAF is a 3rd order Bessel function (linear phase) and is set to the appropriate cut-off frequency based on the filter design that is implemented. The AAF has two available cut off frequencies, 500kHz and 3MHz.

3.2 Analog to Digital Converter (ADC)

The ADC has a pipeline architecture that is 12 bits in hardware and runs at up to 100Msps. Resolutions of up to 16 bits are achieved by oversampling the input and averaging the resultant conversions. During Chip Configuration and Filter Design, the exact sampling speed of the ADC is determined (based on the highest sampling rate required for any one of the four channels).

Not shown in the block diagram are the following sub-blocks which handle decimation/down-conversion of the oversampled data:

CIC (Cascaded Integrator Comb Filters)

The purpose of the CIC stage is gain and offset correction. The digitized signal is then processed in the CIH (Cascaded Integrator Halfband Filters)

CIH (Cascaded Integrator Halfband Filters)

The purpose of the CIH stage (not shown in block diagram) is the integration of 16 bits, and adjustment of the proper sample rate through decimation. Gain correction and droop recovery is performed as well. After moving through the CIH, the signals are sent into the FIR (Finite Impulse Response Filter) for user filtering.

3.3 Finite Impulse Response filter (FIR)

The four FIR filters consist of 512 taps each and are individually programmable. A different filter design may be implemented in each of the 4 filters and may include lowpass, notched lowpass, highpass, bandpass, dual bandpass, bandstop, and dual bandstop. Currently available filter algorithms include Parks-McLellan and Windowed Sinc.

3.4 Serial Interface - Serial Peripheral Interface (SPI)

The serial interface is fully compatible with a standard SPI bus. The serial bus on the QF4A512 is capable of running at up to 40 MHz, although it may be run at much lower speeds. The QF4A512 operates in a SLAVE mode.

Two main modes of operation are used by the bus:

“Configure” mode is used to setup and program the QF4A512 Coefficient RAMs and control registers. Read access to the data RAMs is also available.

“Run” mode provides up to 4 channels of 16-bit multiplexed data out the SPI port. The format is 24-bit (New Data Flag + Over Flow Info + Channel ID + 16-bits of data) multiplexed data. The chip will arbitrate between the incoming channels from the FIRs by monitoring each channel's internal data ready signal. If new data for a given channel is ready in time, it will be inserted on the serial output stream at the appropriate place for that channel and the new data flag will be set in the header. Otherwise the old data will remain in the time slot and the new data flag will not be set. The highest channel sample rate is used as the data rate output for a Data Ready signal, which can be used to maximize bus throughput.

3.5 Startup Modes

The behavior of the QF4A512 during power up or after a reset can be determined by the configuration of 2 bits in the **STARTUP_1** register (07h). The **auto_config** bit, if set, will initiate transfer of EEPROM contents to the control registers and FIR filter coefficient RAMs.

The **auto_start** bit will determine whether the chip starts in Run mode, filtering and sending data out on the SPI bus (**auto_start**=1), or the chip will wait in configure mode until manually started (**auto_start**=0).

If the **auto_config** bit is not set, the chip will wait in configure mode until externally programmed.

An Extended Initialization mode is also available to perform sequences of data transfers from EEPROM to chip control registers (See Chapter 5).

3.6 Memory

The QF4A512 features on-chip Control Registers, RAM and EEPROM. Important device configuration data and filter coefficients can be copied to EEPROM to provide non-volatility. These data can be copied back from EEPROM when the chip is powered up making it unnecessary to reprogram the device at each power up or reset.

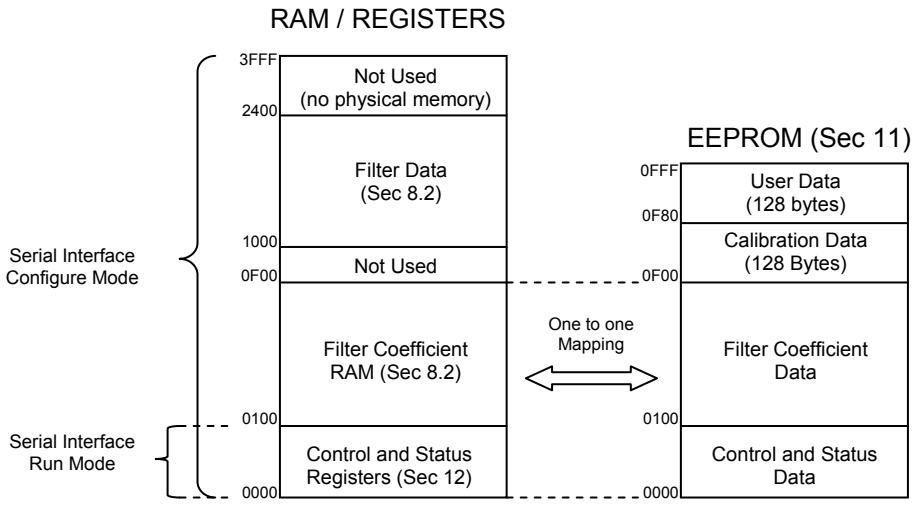


Figure 2. Memory Map

Within EEPROM, 128 bytes of user space are provided for storing application-specific information. This data could include, for example, Transducer Electronic Data Sheets (TEDS, IEEE P1451.4).

The full 14-bit address space can be accessed via the SPI interface in the "Configure" mode. In the "Run" mode only 8-bits of address space can be accessed, which include the command registers and other general configuration registers.

4. SOFTWARE

4.1 Device Configuration

Before useful data can be output from the QF4A512 it must first be correctly configured. Configuration parameters include the following:

1. Startup mode. Options include copying configuration parameters and filter coefficients from EEPROM and then immediately running or waiting for an external command.
2. Number of channels to be active.
3. Gain of the PGA for each input channel.
4. Cutoff frequency of the anti-aliasing filter for each channel.
5. Analog to digital converter sampling rate and decimation/down conversion rate for each channel.
6. FIR filter coefficients.
7. Output data format.

4.2 Quickfilter Development Kit (QF4A512-DK)

The Development Kit is a complete hardware and software combination which allows for rapid development of the QF4A512 configuration parameters for a specific application.

The Quickfilter Pro Design Software tool allows all the necessary parameters to be generated in a quick and user-friendly manner. The user enters the desired characteristics (e.g. sampling rates, type of filter, cut-off frequencies etc.) for each channel and the software generates a configuration file for the device. The configuration file can be immediately downloaded into the QF4A512 on the development board, and the *actual hardware device performance* can be monitored - either in response to a PC-generated noise source or to a user-applied signal. Device configuration parameters can be further adjusted, if necessary, until the optimum system performance is reached.

Once satisfied with the performance the configuration file can be saved for future use, for example to program devices in bulk prior to volume board manufacturing.

4.3 In-circuit (Re)configuration

The Quickfilter Pro Design Software is the recommended method to derive the configuration data for the device. However, it may sometimes be desired to verify the configuration written to the device. Or, in certain applications, it may be desired to re-configure the device in circuit from a host MCU, for example to switch channels on/off, change gain values etc. Therefore, more detailed descriptions of device operation and descriptions of various register settings etc. can be found in sections 5 – 12. For most applications the software alone will be sufficient to provide optimum device performance and reference to these sections will be unnecessary.

5. STARTUP

The behavior of the QF4A512 during power up or after a reset can be determined by the configuration of 2 bits in the **STARTUP_1** register. The **auto_config** bit, if set, will initiate transfer of EEPROM contents to the control registers and FIR filter coefficient RAMs.

The **auto_start** bit will determine whether the chip starts in Run mode, filtering and sending data out on the SPI bus (**auto_start**=1), or the chip will wait in configure mode until manually started (**auto_start**=0).

If the **auto_config** bit is not set, the chip will wait in configure mode until externally programmed.

5.1 Power up / Reset Sequence

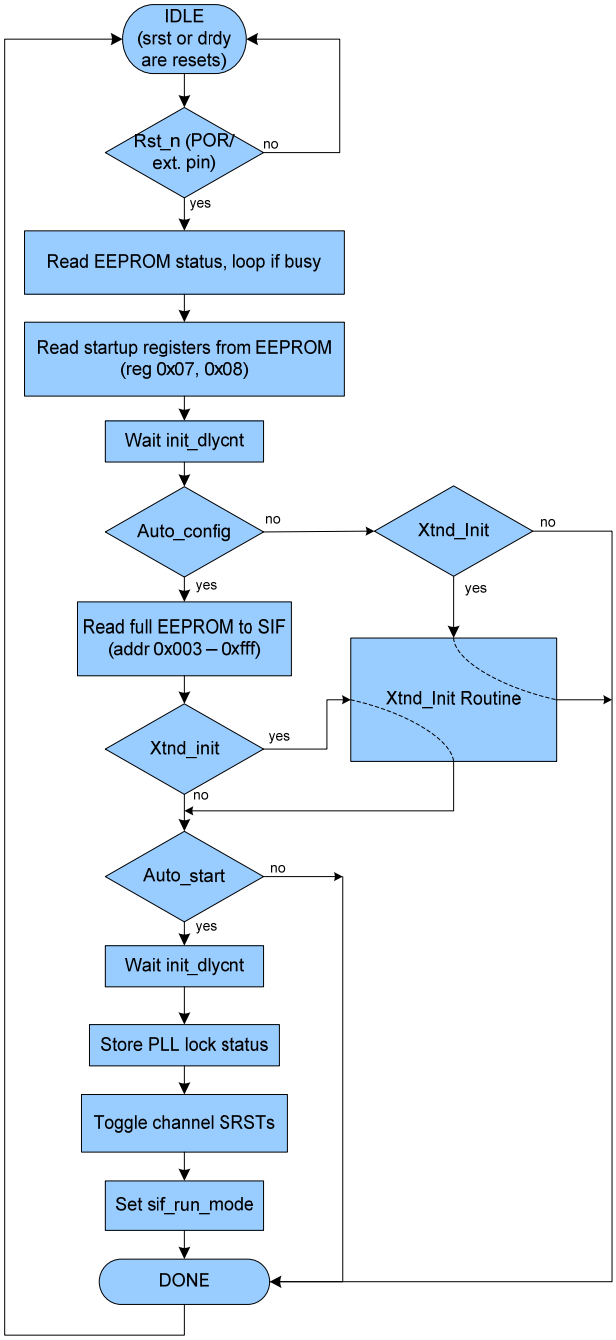


Figure 3. Power up / Reset Sequence

The sequence of events that occurs after a hardware reset is detailed in the preceding diagram. The hardware reset will be applied at power-up or when the external /RST pin is toggled low. If the DRDY pin is held high (for example to write directly to EEPROM) the startup sequence is bypassed.

5.2 Extended Initialization

There is an option to perform an Extended Initialization regardless of the setting for **auto_config**. The Extended Initialization comprises a series of programmable block transfers from the EEPROM to the on-chip registers. To invoke Extended Initialization the **alt_startup1** bit must be set in the **STARTUP_1** register (07h). This will cause the chip to read the **xtnd_init** bit in the **STARTUP_2** Register (Bit 2, register 08h) to determine if an Extended Initialization will occur. If **xtnd_init** is set the chip will then read the starting address for the sequence(s) in EEPROM, **initseq_addr,** from registers **IGC_SEQADDR** (EBh, ECh).

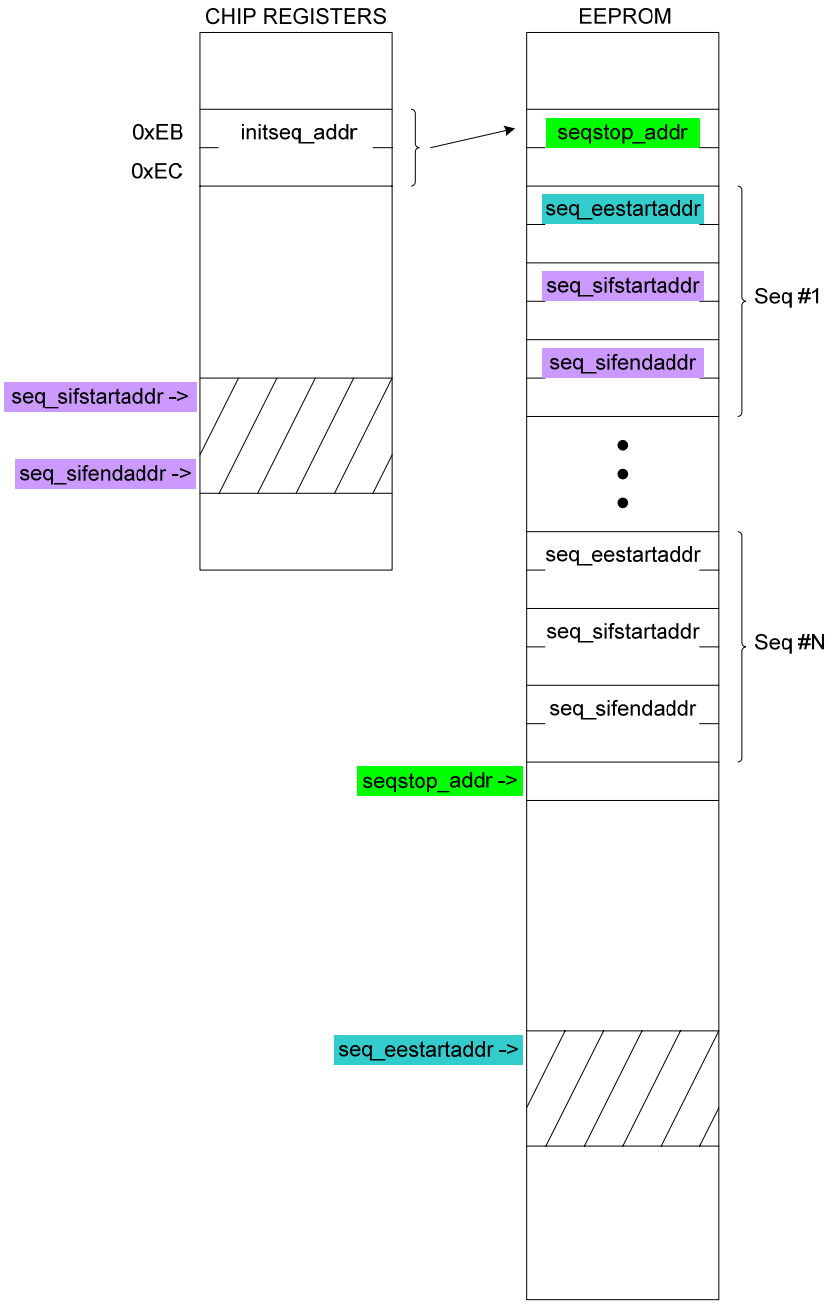


Figure 4. Extended Initialization

Note: The value in the **IGC_SEQADDR** registers can set in two ways. By default, if **auto_config** is not set it will take a value of F00h – corresponding to the start of User Memory. If **auto_config** is set it will be written to the value stored in the corresponding EEPROM address.

The format for the sequences stored in EEPROM is shown in figure 4. The sequences must be in consecutive memory locations and consist of a series of addresses, each having a 16-bit (i.e 2 byte) value.

The first address, **seqstop_addr**, is simply the ending address for the sequence and points to the byte immediately following the final sequence address. This is then followed by a series of sequences, each comprising three addresses. The first address, **seq_eestartaddr**, points to the starting address in EEPROM for the block read. The second address, **seq_sifstartaddr**, points to the destination starting address for where the block data will be written. The third address, **seq_sifendaddr**, is the destination ending address for the data to be written. This will cause the chip to copy a number of bytes, N, starting at address **seq_eestartaddr** to a block of registers starting at **seq_sifstart_addr** and ending at **seq_sifendaddr**, where **seq_sifendaddr = seq_sifstartaddr** + N – 1.

Once this transfer is complete the chip will move to the next sequence and perform a similar operation for its specified addresses, until it reaches **seqstop_addr**. At this point the chip will return to the corresponding point in the Power Up / Reset flow as shown in figure 3.

5.3 Calibration

One possible use for an Extended Initialization sequence is to transfer calibration values stored in EEPROM to the corresponding gain and offset calibration registers for each channel. For more information see Section 7.7.

6. ANALOG FRONT END (AFE)

6.1 Configurable parameters

The following items are configurable for the AFE:

1. Chopper on or off
2. PGA Gain
3. AAF Cutoff Frequency
4. Channel on or off

These settings can all be configured via the Quickfilter Pro software.

6.2 Chopper-stabilized Amplifier

Low frequency flicker noise, which is inherent to CMOS devices, limits maximum dynamic range that can be attained solely by oversampling and averaging data from the analog front end (AFE). This flicker noise has a 1/f^n characteristic, which dominates other noise sources at low frequencies of interest. This is in contrast to white noise, with a flat frequency spectrum, which proportionally decreases with oversampling and averaging.

Chopper stabilization is a technique that applies modulation to transpose the signal of interest to a higher frequency where there is no flicker noise, and then demodulate it back to the baseband after amplification. Details can be found in the following paper: 'Circuit Techniques for Reducing the Effects of Op-Amp Imperfections: Autozeroing, Correlated Double Sampling, and Chopper Stabilisation' By Enz and Temes, Proceedings of the IEEE, November 1996.

In the QF4A512, the circuit is chopped at the input (prior to the PGA) and is remodulated back to the baseband after the analog to digital conversion has occurred. Harmonic components of the chopper frequency are subsequently filtered out in the CIC and CIH blocks. The chopper circuit improves the SNR for configurations with data rates 200 kHz and below. Two important settings in the QF4A512 are the chopper frequency and the phase offset between the modulator and demodulator.

The chopper frequency is set with a divider whose setting is closely related to the CIC R decimation value. The chopper frequency is derived from the ADC clock and the divider value is stored in the **CHPC_DIV*n*** register for each channel. The best setting for the chopper divider is 2 x R x (# of active channels) in most cases. This setting puts the chopper 2nd harmonic frequency in the first null of the CIC filter to most effectively remove it from the final digital signal. While the chopper circuit is effective at signal data rates of 200 kHz and below (down to Hz), the chopper signal itself is most effective at 10 kHz and above, which means the chopper divider should track the CIC R value down only to the point where the chopper frequency would be 10 kHz. For example, for a 4 channel configuration, with the ADC clock running at 50 MHz, and output data rates of 10 kHz and below, the chopper divider should be set no higher than 4E2h (decimal 1250) to ensure the chopper frequency is 10 kHz or above.

The chopper phase accounts for the group delay of the AAF and the pipeline delay of the ADC to ensure the modulated signal is demodulated in the correct phase. The value, which ranges from 680-810 ns, is factory calibrated.

6.3 Programmable Gain Amplifier (PGA)

The PGA buffers and amplifies analog input signals prior to conversion and filtering. The input impedance of the PGA is around 10K on both the positive and negative inputs. The PGA incorporates a chopper stabilized amplifier design to minimize dc offset and noise.

The PGA can be configured as either single-ended or differential and can receive input signals of up to 2.0V p-p directly. With the addition of a single scaling resistor in each channel, two if configured differentially, the PGA can receive signals of up to +/- 10Vp-p or higher. (see Section 14, Applications Circuits)

The PGA gain for each channel can be set to a value of 1, 2, 4 or 8, allowing for the optimum signal level to be passed on for further processing. Usually this will be configured automatically by the Quickfilter Pro software, the resultant value can be verified in the **CH*n*_PGA** register (***n*** = channel number). The gain should be set as high as possible for best SNR, but not too high to cause clipping of the input signal.

6.4 Input Voltage Levels

Ideally the maximum input voltage to the QF4A512 should correspond to a full-scale reading from the ADC. If the input signal level is too low to achieve this, then PGA gain can be introduced to provide a larger signal to the ADC. If the input signal is too high then it should be attenuated to prevent clipping (see section 13 for suggested input circuit configurations). Positive full-scale output from the ADC (7FFFh) will occur when the positive input, A_{IN+}, is 1V more positive than the negative input, A_{IN-}. Negative full scale output (8000h) will occur when A_{IN+} is 1V more negative than A_{IN-}.

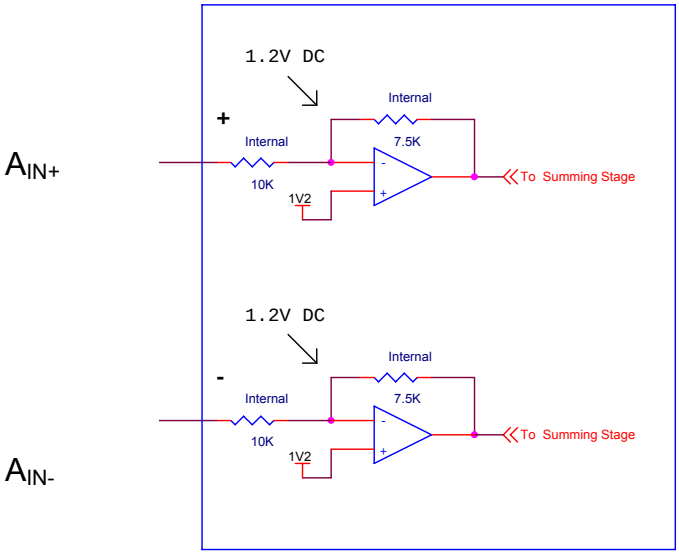


Figure 5. QF4A412 Input schematic

Internally, each input is biased to 1.2V, with a recommended input voltage range from 0.5V to 2.5V. This limits the negative swing on the input to -0.7V so to achieve full scale output from the ADC the input swing would be limited to +/-0.5V (with respect to the 1.2V bias) and a PGA gain of x2 would be selected.

This subject is covered in more detail in Application Note QFAN004, Interfacing Analog Signals to the QF4A512 programmable Signal Converter.

6.5 Anti-Aliasing Filter (AAF)

The Anti-Aliasing Filter is designed to reject frequencies that are higher than the band of interest. If those frequencies are sent to the ADC, they can alias back into the band of interest and can cause erroneous readings to result. The AAF is a 3rd order Bessel function (linear phase) and is set to the appropriate cut-off frequency based on the filter design that is implemented. The AAF has two available cut off frequencies, 500kHz and 3MHz.

The anti-aliasing filter has two frequency cutoff settings which are also configured by the Quickfilter Pro software. If desired the value can be verified in register **CH*n*_CFG** (where *n* is the channel of interest). Either 0.5MHz or 3MHz can be selected according to the frequency of interest for each particular channel.

6.6 Enabling Channels

For a given channel to be active and produce digital output data the following conditions must be met:

a) ADC and system clock enabled (Register **ENABLE_0**, control bits **pcg_ch_enb**).

b) AAF enabled (Register **ENABLE_1**, control bits **afe_opmfec**).

c) Sampling of the designated channel enabled and demuxing to the selected output data stream (Register **ENABLE_2**, control bits **arec_ch_enab**).

d) Channel designated to be present in the output data stream (Register **ENABLE_2**, control bits **sif_ch_enab**)

e) Channel enabled in the global channel control register (Register **GLBL_CH_CTRL**, control bit **ch*n*_pwrd**, where ***n*** is the channel number)

To disable a channel it is only necessary to set the corresponding disable bit in the **GLBL_CH_CTRL** register, this setting will override the ENABLE register bit settings described above.

7. ANALOG TO DIGITAL CONVERTER

7.1 Overview

The ADC has a pipeline architecture that is 12 bits in hardware and runs at up to 100Msps. Resolutions of up to 16 bits are achieved by oversampling the input and averaging the resultant conversions. With INL and DNL of +/- 1LSB, 16 bit linearity is achieved. During Chip Configuration and Filter Design, the exact sampling speed of the ADC is determined (based on the highest sampling rate required for any one of the four channels).

Not shown in the block diagram are the following sub-blocks which handle decimation/down-conversion of the oversampled data:

CIC (Cascaded Integrator Comb Filters)
The purpose of the CIC stage is gain and offset correction. The digitized signal is then processed in the CIH (Cascaded Integrator Halfband Filters)

CIH (Cascaded Integrator Halfband Filters)
The purpose of the CIH stage (not shown in block diagram) is the integration of 16 bits, and adjustment of the proper sample rate through decimation. Gain correction and droop recovery is performed as well. After moving through the CIH, the signals are sent into the FIR (Finite Impulse Response Filter) for user filtering.

7.2 Sampling Rates / ENOB

The QF4A512 features a very flexible architecture allowing tradeoffs between resolution, sampling rate and accuracy. The combination of the ADC sampling rate, subsequent down-conversion in the CIC/CIH blocks and number of active input channels will determine the ***effective sampling rate,*** (f_S), or each input channel. The effective sampling rate is the parameter which limits the overall input bandwidth, according to Nyquist. The table illustrates several different configurations and performance levels for various ADC clock rates.

Table 1. Example sampling rates and ADC clock frequency

ADC clock (f_{ADC}, MHz)	Oversampling Rate	Effective Sampling Rate (f_S)	Aggregate. BW *	Data Output (bits)
12.5	6248	2 kHz	909 Hz	16
12.5	624	20 kHz	9.09 kHz	16
25	128	201.6 kHz	91.6 kHz	16
50	24	2.08 MHz	945 kHz	16
100	48	2.08 MHz	945 kHz	16

* The aggregate bandwidth is equal to the effective sampling rate divided by 2.2.

Although the ADC is 12-bits in hardware, the effective resolution can be increased by oversampling. Theoretically, a 4x increase in the oversampling rate increases the effective resolution by 1 bit. Decimation within the converter always results in 16-bit output data words, regardless of oversampling rate. Beyond a certain limit, determined by the noise and distortion performance of the device, the effective number of bits (ENOB) does not increase any further. For the QF4A512, oversampling rates above 100 have been coded into the Quickfilter Pro Software ("Optimize Precision") to provide optimum performance.

Depending on the application and frequencies of interest it may be more meaningful to refer to the SNR, SFDR or THD in Electrical Characteristics, for a more accurate reflection of overall system performance.

The ADC clock rate (Register **ADC_CLK_RATE**) is always the same for all four channels. However, the oversampling rate can be varied on a per-channel basis. Oversampling by a factor of 4 always occurs in the CIH block, additional oversampling occurs according to the value of "R" in the CIC block. The effective sampling rate (f_S) for each channel is given by the following formula:

$$f_S = f_{ADC} / (4 \times R \times N)$$

R = CIC "R" value (register **CIC_*n*_R** , ***n*** = channel number)
N = Number of active channels

There are many more combinations of ADC clock rate and CIC R values than shown in the table. The Quickfilter Pro software will chose optimum values for each depending on the filter characteristics specified for each of the configured channels. The resulting parameters can be reviewed in the software, and also reviewed by examining the QF4A512's register contents.

7.3 Aggregate Bandwidth

The aggregate bandwidth is the total bandwidth available to all active channels. If only one channel is active then it can use the entire bandwidth, but as further channels are activated the bandwidth available to each will be reduced. Since the oversampling rate can be adjusted for each channel the bandwidth for that channel should be calculated based on its own effective sampling rate. Although Nyquist suggests the sampling rate should be twice the highest frequency of interest it is recommended that a factor of 2.2 be used for optimum performance.

7.4 Serial Interface

For higher frequencies of interest the data rate across the SPI bus must also be considered. The maximum clock rate for the bus is 40MHz which results in a maximum 1.66MHz word rate for 24-bit transfers (multi-channel mode), or 2.5MHz word rate for 16-bit transfers (single channel mode). Allowing for further bandwidth reductions when multiple channels are active, and by applying the 2.2 oversampling factor the maximum analog bandwidth can be determined as shown in the table.

Table 2. Maximum Analog Input Frequency @40MHz SPI bus clock

	Single Channel Mode	Multi-channel Mode			
		1 channel	2 channels	3 channels	4 channels
Maximum analog input frequency	1.136MHz	757kHz	378.8kHz	252kHz	189kHz
Maximum sampling rate	2.5Msps	1.6Msps	800ksps	533ksps	400ksps

7.5 Data Format

The filtered ADC output words are always 16 bits in length. (The 24-bit words output in multi-channel mode comprise a 16-bit data word plus channel ID and status info, see section 10, Serial Interface). The output format is 2's complement so the msb can be regarded as a sign bit. The maximum positive value is 7FFFh, corresponding to an input differential voltage of +1V. The most negative value is 8000h, corresponding to an input differential voltage of -1V (assuming 1x gain).

Each lsb will correspond to 30.5µV at the input with a PGA gain of 1, 15.25µV with a gain of 2, 7.63µV with a gain of 4 and 3.81µV with a gain of 8.

7.6 Analog Mux

The ADC samples each input channel in turn at the output of the analog multiplexer. It takes 9 clock cycles to complete each sample so there is a latency of 9N clock cycles before a complete sample is passed on to the next stage (where N is the number of active channels). Thereafter the pipeline architecture of the ADC will output data on every cycle for subsequent samples. The data samples from the ADC are accumulated and decimated in the CIC/CIH blocks for each respective channel.

Minimum crosstalk is achieved at ADC clock rates of 50MHz or less. Operation at rates up 100MHz is possible for single-channel operation or when some degradation in crosstalk is permissible.

7.7 Gain and Offset Calibration

Provision is provided on chip to calibrate both gain and offset to compensate for deviations from nominal performance in the Analog Front End and ADC. The calibration registers can also be user configured to compensate for variations in external components in the user's application circuit.

Offset calibration, on a per channel basis, is achieved by use of the **CAL_*n*_OFF** register (addresses 56h, 57h for channel 1). This 16-bit value has a default setting of 0h. By appropriately setting this register, offset error can be reduced to less than 1 lsb, well below the noise floor of the device. Typically this register is set to produce a zero output with the input shorted to ground.

Note: If the chopper circuit is used the offset error is effectively removed with no need for calibration.

Gain calibration can be used to fine tune the gain of the chip over a 2:1 range. Register **CAL_*n*_GAIN** (addresses 58h, 59h for channel 1) is used to set the gain on a per channel basis. The nominal / default value for this 16-bit value is 8000h, increasing or decreasing the value will adjust the gain in either direction. User gain calibration can be performed by applying a specific voltage to the analog input and adjusting the value of the **CAL_*n*_GAIN** registers until the appropriate output value is achieved. When used in conjunction with the PGA gain setting it is equivalent to having the ability to scale the input voltage over approximately a 0.5x to 16x range in fine increments.

7.8 Factory Calibration

Device level calibration can be performed during product test. However such calibration will not be as useful as system-level calibration performed by the user. Therefore, by default, factory calibration is NOT performed. Please contact Quickfilter to discuss any requirements you have for factory calibration.

7.9 User (System-level) Calibration

Overall system level performance can be improved if a system level calibration is performed. Using this technique gain and offset errors introduced by variation in external components as well components internal to the QF4A512 itself can be minimized. To achieve this improvement, provision must be made in the user's application circuit to short the input to the channel of interest (for offset calibration) and to apply a known fixed voltage (for gain calibration). The calculated gain and offset calibration values are written to the appropriate **CAL_*n*_GAIN** and **CAL_*n*_OFF** registers.

To perform a user calibration the **CAL_CTRL** (EDh) and **CAL_DTGT** (EEh) registers are used:

1. The **cal_chan_set** bits are written to select the channel, *n*, to be calibrated. (00 = channel 1, 01 = channel 2 …11= channel 4)
2. The **cal_gain_mode** bit selects whether offset (0) or gain (1) calibration is being performed.
3. The **CAL_DTGT** register holds the desired target value (ADC output value) for the voltage applied to the input. It should be set to zero for offset calibration.
4. The **cal_enab** bit is then written to start the calibration measurement.
5. The resultant calibration value is written to the **CAL_*n*_GAIN** (if doing a gain calibration) or **CAL_*n*_OFF** (if doing offset calibration) register.
6. Completion of the test is indicated by **DRDY** going high (and the **cal_enab** bit will auto clear).

Typically this sequence would be performed first for the offset calibration and then repeated (after adjusting **cal_gain_mode** and **CAL_DTGT** accordingly) for gain calibration.

7. To make this calibration data non-volatile the **CAL_*n*_GAIN** and **CAL_*n*_OFF** register values should be copied to EEPROM ((see Section 11.2)) after the calibration measurement is complete.

For gain calibration the target value (**CAL_DTGT**) will depend on the input voltage applied and the PGA gain setting for the channel. For example, a full scale (positive) reading of the ADC would be 7FFFh for a 1V input (to the ADC). If the PGA gain is set to x2 this would correspond to a +0.5V differential voltage at the device input pins. In practice a fixed input voltage in the range of 75-80% of full scale and the corresponding ADC output value would typically be used – allowing for some headroom for offset calibration and to prevent "clipping" of the ADC output for slightly over-range input voltages.

Note: The method described above is ideal if the QF4A512 configuration is static in the user's application. If the application calls for dynamically altering the configuration (for example PGA gain), or if a single design is used for multiple applications with differing configurations, it may be beneficial to take multiple calibration readings, one for each configuration. In this case the multiple calibration values could be stored in User EEPROM and transferred to the calibration registers at power up (or reset) by means of an extended initialization sequence tailored for the desired configuration. This is the same technique that is used to transfer the factory calibration data to the appropriate calibration registers. Indeed, if user calibration is performed it may be convenient to replace the default factory calibration values with the user measured values.

8. FIR FILTERS

8.1 FIR Overview

Each channel features a 512-tap FIR which is used to define the precise filtering characteristics desired. The filtering characteristics of each channel may be set independently may include any combination of the following types: lowpass, notched lowpass, highpass, bandpass, dual bandpass, bandstop, and dual bandstop. Currently available filter algorithms include Parks-McClellan and Windowed Sinc.

The Quickfilter Pro software allows the user to enter the filter characteristics required and see the predicted performance in terms of frequency and impulse response. Once the desired performance has been attained, the configuration can be downloaded to the QF4A512, and the actual hardware performance verified, by using the development kit. The device can be fed with a white noise source (or other source as desired by the user) and the software can display an FFT of the QF4A512's filter response.

The FIR coefficients are downloaded from EEPROM into RAM at power up (depending on the contents of the STARTUP register). The output data from the FIRs is stored in data RAM, this data in turn is output from the SPI port when the device is run mode (see Section 9).

8.2 FIR Memory Locations

The memory locations for the control registers, coefficient and data RAM's for each channel are shown in the following tables:

Table 3. Channel 1 - FIR Filter Address Information

Address	Register Name	Description
0030h	**CH1_PGA**	Control Register. Enable FIR operation, set PGA gain.
0100h – 017Fh	**FIR_0_0_COEF_RAM**	G & H coefficients
0300h – 05FFh	**FIR_0_1_COEF_RAM**	FIR Coefficients
1000h – 10FFh	**FIR_0_0_DATA_RAM**	G & H Data memory
1400h – 17FFh	**FIR_0_1_DATA_RAM**	FIR filter Data Memory

Table 4. Channel 2 - FIR Filter Address Information

Address	Register Name	Description
0060h	**CH2_PGA**	Control Register. Enable FIR operation, set PGA gain.
0180h – 01FFh	**FIR_1_0_COEF_RAM**	G & H coefficients
0600h – 08FFh	**FIR_1_1_COEF_RAM**	FIR Coefficients
1100h – 11FFh	**FIR_1_0_DATA_RAM**	G & H Data memory
1800h – 1BFFh	**FIR_1_1_DATA_RAM**	FIR filter Data Memory

Table 5. Channel 3 - FIR Filter Address Information

Address	Register Name	Description
0090h	**CH3_PGA**	Control Register. Enable FIR operation, set PGA gain.
0200h – 027Fh	**FIR_2_0_COEF_RAM**	G & H coefficients
0900h – 0BFFh	**FIR_2_1_COEF_RAM**	FIR Coefficients
1200h – 12FFh	**FIR_2_0_DATA_RAM**	G & H Data memory
1C00h – 1FFFh	**FIR_2_1_DATA_RAM**	FIR filter Data Memory

Table 6. Channel 4 - FIR Filter Address Information

Address	Register Name	Description
00C0h	**CH4_PGA**	Control Register. Enable FIR operation, set PGA gain.
0280h – 02FFh	**FIR_3_0_COEF_RAM**	G & H coefficients
0C00h – 0EFFh	**FIR_3_1_COEF_RAM**	FIR Coefficients
1300h – 13FFh	**FIR_3_0_DATA_RAM**	G & H Data memory
2000h – 23FFh	**FIR_3_1_DATA_RAM**	FIR filter Data Memory

Note: Address space from 0F00h - 0FFFh and 2400h – 3FFFh is not used. If these locations are read they will return zeroes.

8.3 FIR Latency

There will be a delay introduced to the signal as it passes through the QF4A512. There are several components to this latency:

1. PGA and AAF
2. ADC
3. CIC and CIH filters (Filter 0)
4. FIR filters (Filter 1), up to 512 taps – delay determined by user–specified filter response.
5. Number of active channels (N).

The dominant influence on the overall latency will be the fourth item. The delay introduced by the FIRs is given by:

FIR Delay = (# taps – 1)/2 * $1/f_s$

The PGA + AAF latency = 0.7us (approx) if f_s <800kHz, or 0.12us (approx) if f_s >800kHz.

The ADC latency is equal to 9 ADC clock cycles = 9*N/(ADC clock rate)

The CIC/CIH latency = $28.5 / f_s$

For an ADC clock rate of 75MHz, a single channel sampling at 10kHz would result in latencies of:

512 tap (maximum) filter: Latency = 28.4ms (=0.7us + 9/75MHz + 28.5/10kHz + 255.5/10kHz)

100 tap filter: Latency = 7.8ms (=0.7us + 9/75MHz + 28.5/10kHz + 49.5/10kHz)

Note: The latency for a specific configuration is calculated and displayed on the Config panel within the Quickfilter Pro software.

8.4 Maximum number of taps

There may be situations where it is not possible to implement a filter using all 512 taps. At high sampling rates it may not be possible to implement all 512 taps within the maximum available sys_clk rate. The equation which determines this is as follows:

Max Taps = 2 * Sys_clk/f_s

Example: sys_clk = 200MHz (max allowed value), fs = 2MHz → Maximum number of taps = 200.

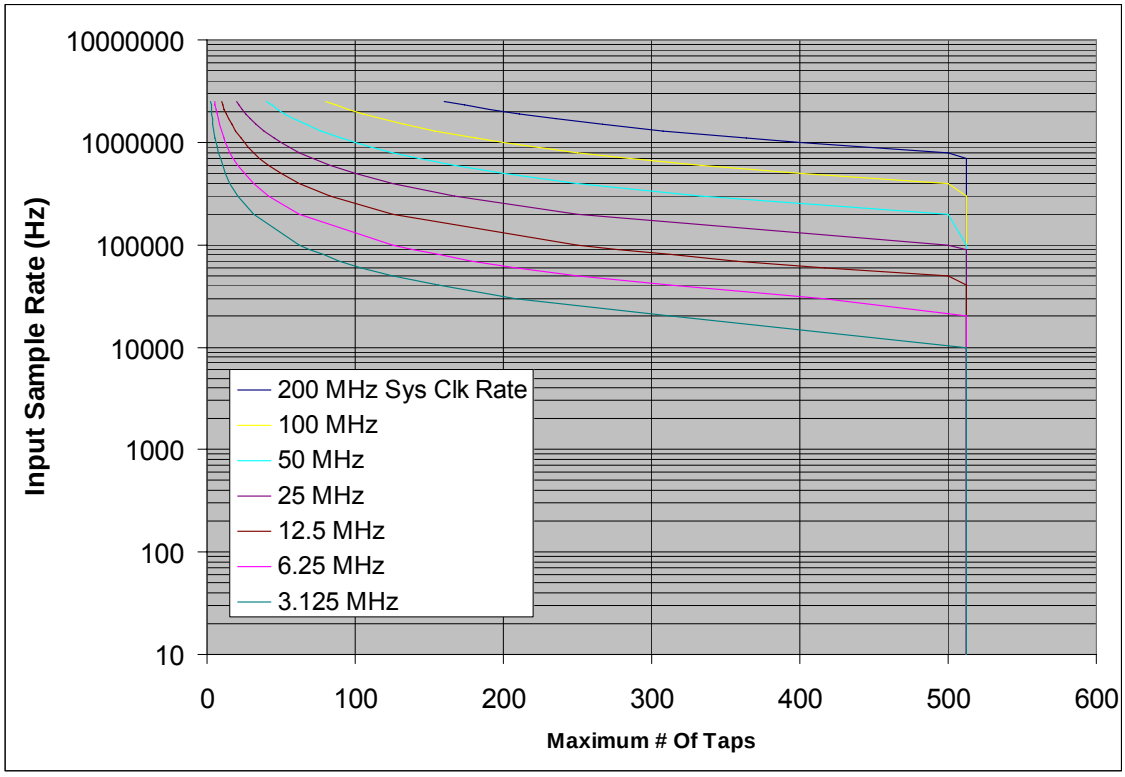


Figure 6. Maximum Taps vs. Sample Rate vs. Sys Clk

9. SYSTEM CLOCKS

The master clock for the QF4A512 is produced by a crystal oscillator with a nominal frequency of 20MHz. Alternatively the device can be fed with an external clock signal derived elsewhere. The master clock is used as a reference for a phase-locked loop (PLL), from which clocks are derived to drive the FIR filters, the ADC and the analog front end. The master clock is also divided down to provide a clock to be used for transfers to the on-chip EEPROM.

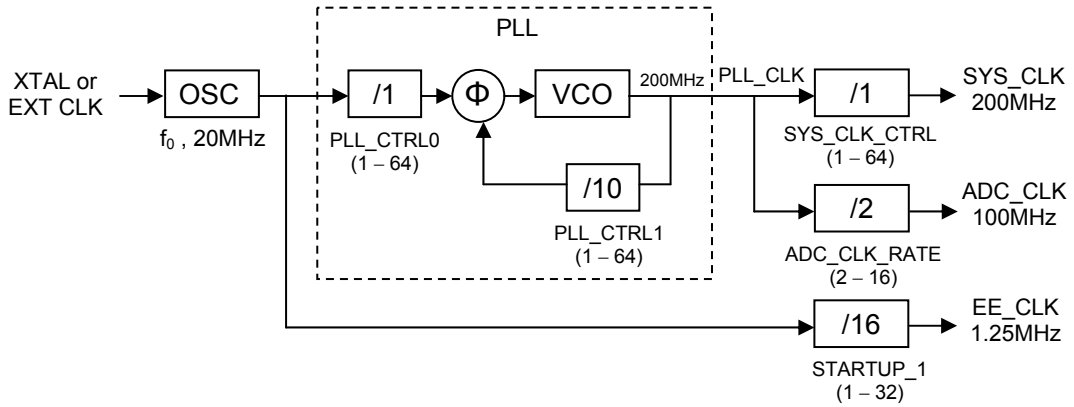


Figure 7. System Clocks Block Diagram
(Default settings shown)

9.1 PLL Clock

The PLL clock frequency is determined by the input clock frequency, f_0, the pre-divider value (M) and the divider value (N):

$$PLL\_CLK = f_0 * N / M$$

The default frequency for PLL_CLOCK is 200MHz. (f_0 = 20MHz, M = 1, N= 10)

Operation of the PLL is possible in two frequency ranges: 20-100MHz and 100-300MHz.

Control registers: PLL_CTRL0 and PLL_CTRL1

9.2 System Clock

The System Clock (SYS CLK) is divided down from PLL CLK by a number in the range 1 – 64, default = 1. SYS CLK is used as the reference for the FIRs.

The default frequency for SYS CLK is 200MHz.

Control register: SYS_CLK_CTRL

9.3 ADC Clock

The ADC Clock (ADC CLK) is also divided down from PLL CLK. The range of divisor values is 2 -16, default = 2. ADC CLK is used to drive the ADC (including CIC and CIH blocks) and other analog front end blocks.

The default frequency for ADC_CLK is 100MHz.

Control register: ADC_CLK_RATE

9.4 EE Clock

The EE Clock (EE CLK) is used for transfers to/from EEPROM. This clock is divided down directly from the master clock with divisors in the range 1 – 32, default value = 16.

The default frequency for EE_CLK is 1.25MHz.

Control register: STARTUP

10. SERIAL INTERFACE

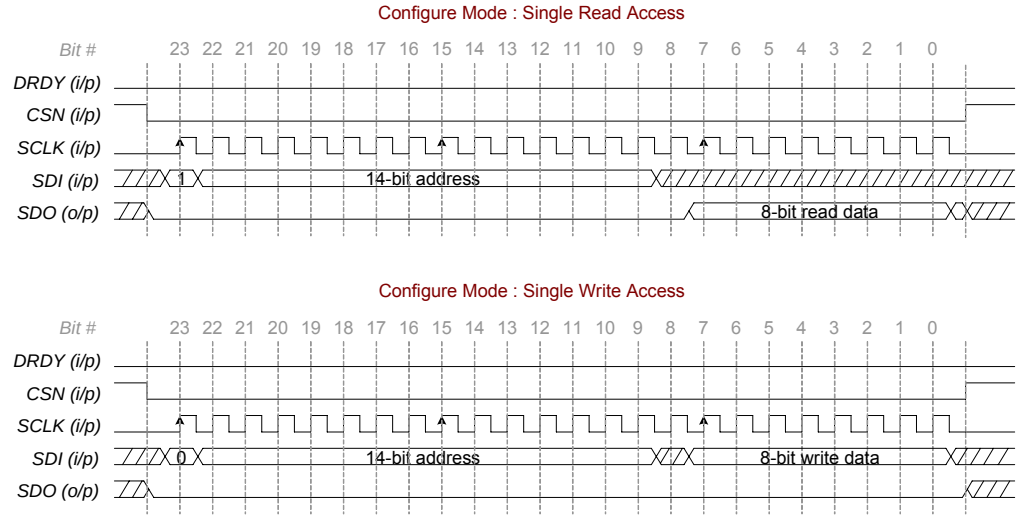
10.1 Modes of Operation

The QF4A512 is designed to interface directly with the serial peripheral interface (SPI) of microcontrollers and Digital Signal Processors. The QF4A512 always operates in SPI slave mode where SDI is the input serial data, and SDO is the output serial data. SCLK is the input serial clock maximum 40 MHz.

In order to address and write to the QF4A512, /CS is asserted lo

(Data7 - Data0) = Unique data per command.

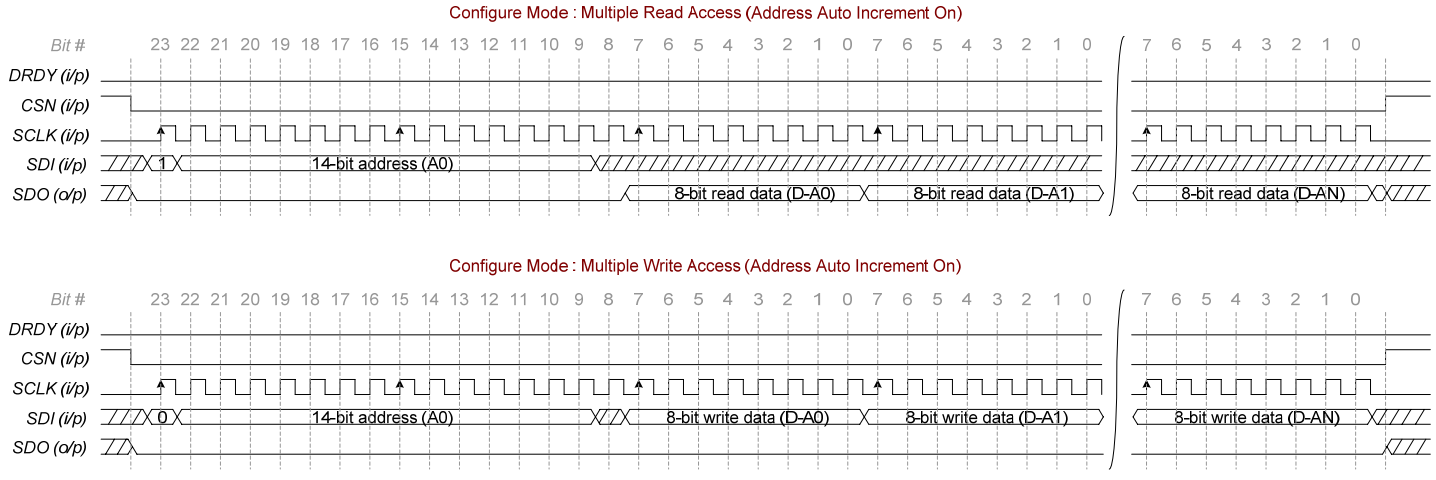
Note, this data applies to SO and SI depending whether it is being read or written.



Notes:
> SDI is captured on the rising edge of SCLK
> SDO transitions after the falling edge of SCLK
> SDO is tri-stated when CSN is high

〈//〉 denotes a "don't care"

Figure 9. Configure Mode Timing, Read and Write



Notes:
> With AAI enabled (reg 0x0015, bit 3 = 1), holding CSN low continues data byte read/write accesses
> AAI works in Configure-mode only (not Run-mode)
> AAI writes can not cross register–coefficient memory boundary. Write as 2 blocks (0x0000 –> 0x00ff, 0x0100 –> 0x2400)
> AAI reads have no boundary restrictions

Figure 10. Configure Mode Timing – Multiple Read / Write

Note that Configure mode registers wider than 8 bits must be written completely starting at the low address.

10.3 Run Mode

By setting the **run_mode** bit to 1 the QF4A512 is in Run mode, and will output converted and filtered data.. A 24-bit format is used including information and data (New Data Flag + Channel ID + 16 bits of data). The Serial Interface (SIF) will arbitrate between the incoming channels from the FIRs by monitoring each channels internal data ready signal. If new data for a given channel is ready in time, it will be inserted on the serial output stream at the appropriate spot for that channel and the new data flag will be set in the header. Otherwise the old data will be output and the new data flag will not be set. The highest channel's sample rate will be used as the data rate output for the DRDY signal, which can be used for handshaking to maximize bus throughput.. Over and under range of the ADC per channel can be monitored. See Section 10.4 for available commands in Run Mode.

The parity bit can be activated to verify proper data transfer. When turned on the parity bit will either add a 0 or 1 to force the remaining 23 bits to equal an odd number of 1's.

Note: For single-channel applications it is possible to use a "high-speed" 16-bit format, without the channel IDs and New Data Flag. This would be used if bus throughput was the limiting item on overall performance. Use of this format is detailed in Application Note QFAN002, "High-Speed Single Channel Operation".

Note: If the device is configured such that a low system clock is used in conjunction with the maximum SPI clock it may be possible for /CS to return to a high level before DRDY has been cleared. To prevent this from occurring be sure to conform to the timing requirements in Electrical Characteristics.

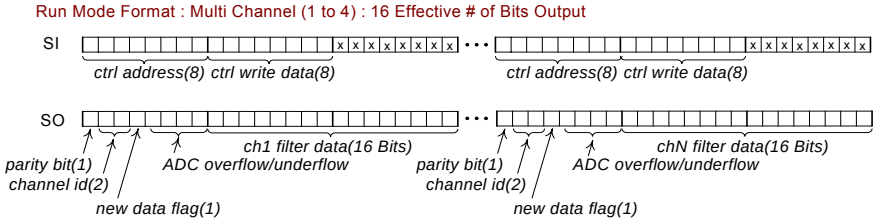


Figure 11. Run Mode Format

Table 9. Run Mode, Control Address for Command Writes, SDI (00h-FFh)

A7	A6	A5	A4	A3	A2	A1	A0
Addr7	Addr6	Addr5	Addr4	Addr3	Addr2	Addr1	Addr0

Addr7-Addr0 = Command Address

Description: See Section 10.4.

Table 10. Run Mode, Control Register Data Format (00h-FFh)

D7	D6	D5	D4	D3	D2	D1	D0
Data7	Data6	Data5	Data4	Data3	Data2	Data1	Data0

(Data7 - Data0) = Unique data per command.

Description: See Section 10.4.

Table 11. Run Mode, Output Data Structure, LSB, SD0 (0000h-FFFFh)

D7	D6	D5	D4	D3	D2	D1	D0
Data7	Data6	Data5	Data4	Data3	Data2	Data1	Data0

Data7- Data0 = Least Significant Byte (LSB)

Description: This is the Least Significant Byte of the 16-Bit filtered data output.

Table 12. Output Data, Second LSB, SD0 (0000h-FFFFh)

D15	D14	D13	D12	D11	D10	D9	D8
Data15	Data14	Data13	Data12	Data11	Data10	Data9	Data8

Data15- Data8 = Most Significant Byte (MSB)

Description: This is the Most Significant Byte of the 16-Bit filtered data output.

Table 13. Output Data, MSB, SD0 (00h-FFh)

D23	D22	D21	D20	D19	D18	D17	D16
PARITY	CH_ID	CH_ID	NEW	adc_ov_L	adc_ov	adc_un_L	adc_un

Data23- Data16 = MSB of the 24 bit serial data.

Description: This is the information byte showing which channel the data corresponds to, along with the new data flag and parity bit for valid data check.

Bits D16-D19 – ADC Overflow/Underflow

Description: These bits, if enabled by the **adc_stat** bit in the **SPI_CTRL** register (15h), indicate over- or under-range conditions in the ADC output. The unlatched bits reflect the contents of the **ADC_STATUS_1** register (11h), the latched bits reflect the contents of the **CHn_STAT** registers (31h, 61h, 91h, C1h). The latched bits will retain their state until reset by writing a zero to the appropriate **CHn_STAT** register.

adc_ov_L 1 = ADC Over-range, latched output

adc_ov 1 = ADC Over-range, not latched

adc_un_L 1 = ADC Under-range, latched output

adc_un 1 = ADC Under-range, not latched

Note: If these bits are enabled the parity option should not also be enabled.

NEW (Sets new data flag)

* 0 = No new data has been put on the SIF serial bus for that specific channel

1 = The data has been updated on the SIF bus

CH_ID (Identifies which channel the data corresponds to)

* 00 = Channel 1

01 = Channel 2

10 = Channel 3

11 = Channel 4

PARITY (Parity bit)

If Parity is enabled this bit will assume a state such that the total number of ones in the data word is odd.

*Note: Parity should not be enabled if ADC out-of-range status reporting is turned on (bit 6 of register 15h – **SPI_CTRL**). If both features are enabled the state of the parity bit will not be reliable.*

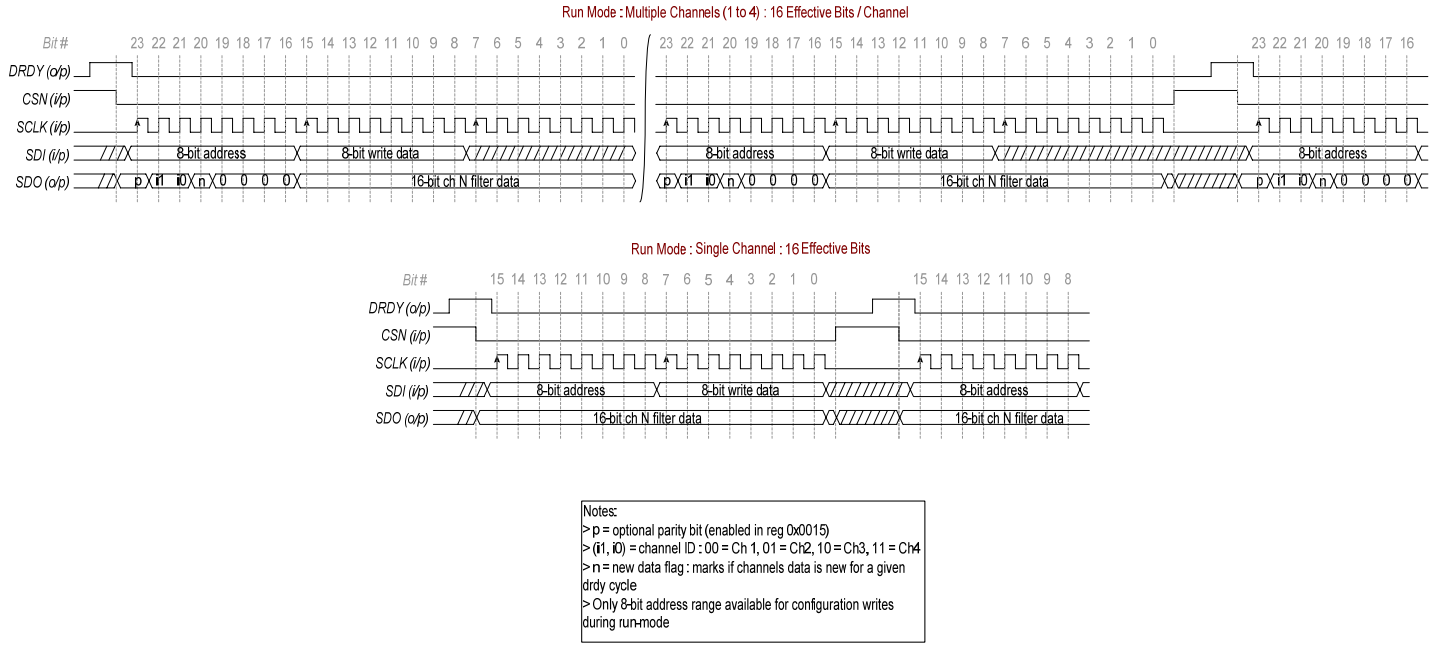


Figure 12. Run Mode Timing, Read and Write

Note: Once set by the chip DRDY will remain high until /CS is pulled low.

10.4 Sending Commands in Run Mode

Although Run mode exists primarily to output filtered data from the ADC it is also possible to issue commands to the QF4A512 in this mode. Of fundamental importance is the ability to write the command to exit run mode and return to Configure mode!

In fact, it is possible to write to any register (that allows writes) within the first 8 bits of address space (Registers 00h – FFh). The format and timing can be seen in Figures 10 and 11. In the register descriptions (Chapter 12) all registers are writeable (R/W) except those specifically designated as Read Only or Auto Set. Obviously since the output data is dedicated to filtered conversion results from the ADC it is not possible to read any of the control registers while in Run mode (except of course for data which is included in the header of the MSB, for example, the new data flags).

The most likely registers to be used for dynamic adjustment during Run mode are as follows:

GLBL_SW (00h)
Actually being used as a dummy register, it is useful to set the control address to 00h when no commands are being issued to prevent inadvertent writes to other command registers.

RUN_MODE (04h)
Writing a 0 to bit 0 will take the QF4A512 out of Run mode and back to Configure mode.

ENABLE_2 (0Bh)
The 4 lsb's can be used to turn on/off data in the output data stream (**arec_ch_en** bits). This can be useful to regulate SPI bandwidth when using multiple channels with varying sample rates.

CHn_PGA (30h, 60h, 90h, C0h)
The **pga_gain** bits can be used to vary the PGA gain on a per channel basis.

CAL_*n*_OFF (56h,57h, 86h, 87h, B6h, B7h, E6h, E7h)
Offset calibration value for channel ***n***.

CAL_*n*_GAIN (58h,59h, 88h, 89h, B8h, B9h, E8h, E9h)
Gain calibration value for channel ***n***.

Note: There are differences in the way the address and data is formatted between Run Mode and Configure mode.

In Configure mode 14-bit address words are used. In Run mode 8-bit addressing is used. These differences are shown graphically in the following diagram. Consequently the host controller must use the appropriate timing depending on which mode of operation is active. (At power up the mode of operation is determined by the value of the **auto_start** bit (register **STARTUP_1**).

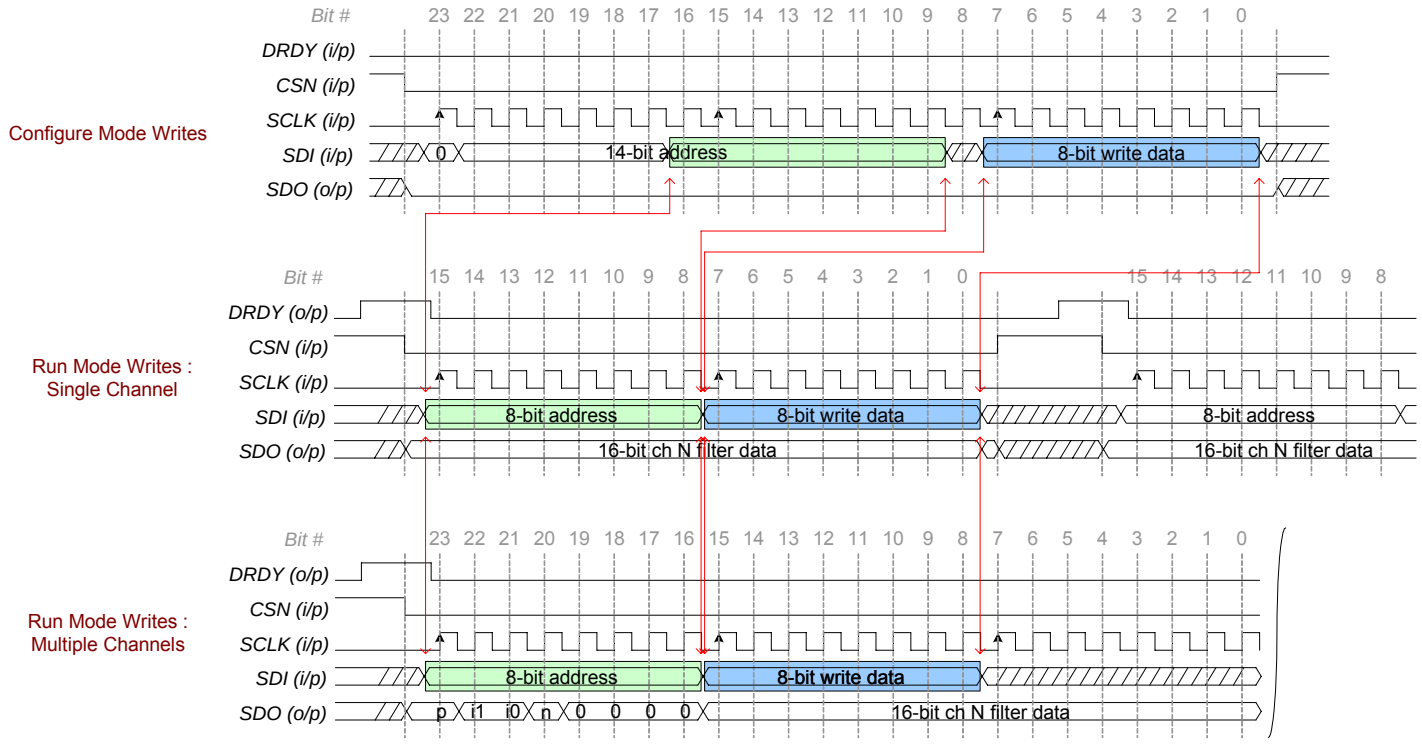


Figure 13. Comparison of Configure and Run Mode Timing

If it is unknown which mode is active there are several ways to determine this. If in Run mode there should be a continuous stream of conversions occurring which should be reflected by changes in level of the DRDY pin, furthermore if SCLK is active and CSN is held low there should be transitions occurring on the SDO pin. These pins can me monitored for activity within a pre-determined timeout interval. These methods are summarized below.

1. If the QF4A512 is in Run mode, DRDY will be driven high when the fastest sample is available. If in Configure mode, DRDY is an input (internal pull-down in the chip). So, by monitoring DRDY you can determine the mode of operation.
2. Holding SDI low (to prevent inadvertently writing any bad info to the chip), toggle SCLK and look for data on SDO. If in Configure mode, SDO will be low the whole time. If in Run mode, SDO will eventually toggle.

11. EEPROM

11.1 Overview

Table 14. EEPROM Memory Map

0F80	User Data (128 bytes)
0F00	Chip Calibration (128 Bytes)
0100	Filter Coefficient Data
0007	Control and status data
0000	Not used

The internal EEPROM is used to store the QF4A512's FIR coefficients, general parameters and startup mode as well as have user space for application specific use, for example Transducer Electronic Data Sheets (TEDS).

Address space 0007 through 0EFF can be automatically transferred at startup to the corresponding Register and RAM addresses. Full transfers can also be initiated, in either direction, by writing to the **EETRANS** (EEPROM Transfer) register. Manual single-byte and block transfers can be performed as described below.

11.2 EEPROM Transfer Procedures

Usually the SPI port connects directly to the chip's internal serial interface (SIF) control block. The SIF allows the user to read or write to on-chip control registers and RAMs. In turn the SIF controls data transfers internally between the registers/RAM and EEPROM.

The following describes procedures to transfer data to/from the EEPROM.

Manual Single Byte and Multi-Byte Transfers

Manual transfers between the register map & coefficient RAM, and the EEPROM occur as follows:

Set the clock rate divider for the transfer based on the crystal frequency as the source: **eeclk_rate** = 000 to 101 (Register **STARTUP_1**, 07h). 000 = XTAL rate, 001 = divby2 … 101 = divby32.

Set the source address:
For reads from EEPROM: **EE_STADDR (17h)**.
For writes to EEPROM: **CHIP_STADDR (18h)**.

Set the destination starting address (can be different from source address):
For reads from EEPROM: **CHIP_STADDR (18h)**.
For writes to EEPROM: **EE_STADDR (17h)**.

For single byte transfers:

Set the destination ending address to the same value as the destination starting address: **END_ADDR** (1Bh).

For multi-byte transfers:

Set the destination address to the desired ending address of the *destination* block. See the following paragraph for applicable restrictions.

Start the transfer:

For EEPROM reads: Set the **rd_start** bit in the **EE_TRANS** register **(05h)**.

For EEPROM writes: Set the **wr_start** bit in the **EE_TRANS** register **(05h)**.

Wait for the transfer to complete. One way to accomplish this is to continually try reading the **GLBL_ID** register (01h) until you get the correct ID value.

Multi-Byte Transfer Restrictions

Reading from EEPROM

A contiguous transfer will not proceed across the register map – coefficient memory boundary. In other words, you can't cross 00FFh – 0100h within the block you are transferring. An easy solution is to break up the block into 2 block transfers, one up to 00FFh and the other starting with 0100h.

Writing to EEPROM

Starting with address 0000h, all block transfers must be on 32-byte boundaries (EEPROM limitation). As an example, if you want to transfer into EEPROM addresses 0000h to 0030h (48 dec), you would break this into 2 blocks, one from 0000 to 001Fh (31 dec), and one from 0020h to 0030h.

EEPROM Status

By setting the **rd_status** bit (**EE_TRANS** register) the chip will read the status register of the EEPROM and put its contents into the **EE_VAL** register. Again, to check if the transfer is done, you can continually access the **GLBL_ID** register (01h) until you get the correct ID value.

Full Transfers

Full EEPROM transfers cover the address range **0006h – 0EFFh**. A one-to-one image is copied for this entire range. Addresses that are undefined in the memory map will fill the EEPROM with a default value. Addresses prior to this range (< 0006h) do not contain information which needs to stored in non-volatile memory and also control the manual transfers described above. Thus we don't want these to go into the EEPROM or they may cause unusual behavior when the chip powers-up (resets). Full transfers are performed as follows:

As above in Manual Transfers, **eeclk_rate** (07h) should be set appropriately.

Start the transfer:

For reading from the EEPROM: Set the **rd_full** bit in the **EE_COPY** register (06h).

For writing to the EEPROM: Set the **wr_full** bit in the **EE_COPY** register (06h).

Wait for the transfer to complete. One way to accomplish this is to continually try reading the ID register (0001h) until the correct ID value is returned.

11.3 Calibration Data

128 bytes of memory are nominally reserved for calibration data. This data can be transferred to the **CAL_OFFSET_*n*** and **CAL_GAIN_*n*** registers (see Section 7.7) at startup by using the Extended Initialization feature of the QF4A512 (see Section 5.2).

By default the QF4A512 is shipped with factory calibration data in this area of memory. At the User's option he may elect to replace this data with his own system-level calibration data, or if no calibration data is required this memory may be used as an additional 128 bytes of User Memory.

Note: Once overwritten the factory calibration data cannot be restored.

11.4 User Memory

128 bytes of EEPROM (starting address 0F80h) have been set aside for user data. This can contain any type of application specific data, for example TEDS data as defined in IEEE P1451.4.

Table 15. T.E.D.S. (Transducer Electronic Data Sheet, Basic Template)

	Bit Length	Allowable Range
Manufacturer ID	14	17 - 16381
Model Number	15	0 – 32767
Version Letter	5	A – Z (data type Chr5)
Version Number	6	0 - 63
Serial Number	24	0 - 16777215

Refer to IEEE-P1451.3 for further information on TEDS.

Alternatively other user-specific information and/or formats can be stored in this area.

The user data is not copied into chip RAM at power up. Since direct reads from EEPROM are not usually possible there are two methods to read/write the user data:

a) Using the **SCRATCH** registers. The 8 registers starting at address 001Dh can be used to transfer data 8 bytes at a time, using the multi-byte transfer method described above.

b) Using the data RAM at startup. If the device is powered up in Configure mode all 128 bytes of user data can be block transferred into the filter data RAM starting at address 1000h. Once the device enters Run mode this data will be overwritten with the data output from the FIRs so this technique can only be used at startup.

12. CONTROL REGISTERS

12.1 Overview

Table 16. Control Register Map

00C0	Channel 4	Maintenance (9)
		Configuration (31)
		Run & Status (2)
0090	Channel 3	Maintenance (9)
		Configuration (31)
		Run & Status (2)
0060	Channel 2	Maintenance (9)
		Configuration (31)
		Run & Status (2)
0051	Channel 1	Maintenance (9)
0032		Configuration (31)
0030		Run & Status (2)
001D	Global Maintenance (19)	
0011	Global Configuration (12)	
0009	Run & Status (8)	
0005	EEPROM Startup (4)	
0000	High Level (5)	

Note: Numbers in parentheses are the number of bytes allocated to each function.

The Control Registers are located in the first 256 bytes of address space as shown in the table. The QF4A512 can be configured to automatically load these registers from EEPROM, with the exception of the first 7 bytes, at power up or after a reset.

It is strongly recommended that the configuration and filter coefficient data is set up using the Quickfilter Pro software. For applications requiring reconfiguration on the fly it is suggested that complete configuration files, generated by the software, are stored in external memory and loaded in full to the device. However, it may often be necessary to write individual commands to the device, for example to switch between run and configure mode, or to turn on/off specific channels. To accomplish this, more detailed descriptions of register functions can be found in the following paragraphs.

Several registers are designated as "Reserved". The user may write to these registers without any effect on chip operation, i.e. it is possible to write to the entire register map as a single contiguous block. However, when they are read these registers will not necessarily reflecting the value written to them during the write operation.

The corresponding EEPROM locations can also be written, and these values can also be read back. Since these locations may be used for future functionality they should not be used for user data (the user area is available for this purpose).

Other registers are denoted for Factory Use Only. These registers should be written with the default values shown to ensure correct device operation.

Table 17. Control Register listing (High-Level, EEPROM Startup, Run & Status)

Hex*	Register Name	Description
0000h	**GLBL_SW**	Software Register, Test Reads and Writes
0001h	**GLBL_ID**	Chip ID Including Revision Number.
0002h	**FULL_SRST**	Activates all soft resets
0003h	**GLBL_CH_CTRL**	Reset, Enable or Power Down each channel
0004h	**RUN_MODE**	Set chip in Run or Configure Mode
0005h	**EE_TRANS**	Control data transfers to/from EEPROM
0006h	**EE_COPY**	Control full transfers to/from EEPROM
0007h	**STARTUP_1**	Set startup configuration, rate for EEPROM clock
0008h	**STARTUP_2**	Initialization delay counter
0009h	**ENABLE_0**	Enable ADC and system clock per channel
000Ah	**ENABLE_1**	Enable AAF per channel, ADC operation mode
000Bh	**ENABLE_2**	Designate active channels
000Ch	**PLL_SIF_STAT**	PLL lock, SIF address out of range
000Dh	**EE_VAL**	EEPROM status register value
000Eh	**EE_STATUS**	EEPROM transfer status flags
000Fh	**ADC_STATUS_0**	ADC out of range, per channel
0010h	**ADC_STATUS_1**	ADC out of range, high or low, per channel

12.2 High-level Registers

Note: * denotes default values

00h GLBL_SW (User Register)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Address 00h	D7	D6	D5	D4	D3	D2	D1	D0

Description: Global Software is provided as a blank user byte for the programmer to read and write to as a test. This byte defaults to 0 at power up and is not loaded from EEPROM.

01h GLBL_ID (Chip ID) - READ ONLY

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Address 01h	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0

[ID7:ID0] = Identification number of the QF4A512, default = A0h (was B1h on pre-production devices).

Description: This read-only byte contains a number describing the identification of the QF4A512 device. This data is hard-wired and is not transferred from EEPROM. It can be read at any time.

*Note: Revision information can be found in the **DIE_REV** register (EAh)*

02h FULL_SRST (Global Soft Reset)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Address 02h	X	X	X	X	X	X	X	glbl_srst

glbl_srst

* 0 = Does nothing.

1 = Reset

Description: Activates all soft resets. The reset value of this register is zero, regardless of the data in the corresponding EEPROM address.

03h GLBL_CH_CTRL (Global Channel Control)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Address 03h	ch4_pwrd	ch3_pwrd	ch2_pwrd	ch1_pwrd	ch4_srst	ch3_srst	ch2_srst	ch1_srst

ch*N*_srst

* 0 = Does nothing.

1 = Reset

Description: Activates all soft resets on a per channel basis.

ch*N*_pwrd

* 0 = Does nothing.

1 = Disable/power down

Description: Turns on or off each channel.

Note: The reset value of this register is zero, regardless of the data in the corresponding EEPROM address.

04h RUN_MODE (Serial Interface Run mode)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Address 04h	X	X	X	X	X	X	X	run_mode

run_mode

* 0 = Configure mode.

1 = Run mode.

Description: Sets the serial interface (SPI) to either configure or run mode. The reset value of this register is zero, regardless of the data in the corresponding EEPROM address. However, if **auto_run** and **auto_config** bits are set the chip will write this register to 1 after a reset (see **STARTUP_1** Register, 07h).

12.3 EEPROM Startup Registers

05h EE_TRANS (EEPROM Transfer) – AUTO CLEAR

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Address 05h	X	X	X	X	X	rd_status	wr_strt	rd_strt

rd_strt

* 0 = default

1 = start transfer

Description: Command to start transfer from EEPROM to registers/RAM.

wr_strt

* 0 = default

1 = start transfer

Description: Command to start transfer from registers/RAM to EEPROM.

rd_status

* 0 = default

1 = start read of status register

Description: Command to start read of EEPROM status register.

Note: These command bits are automatically cleared by the chip after use. The reset value of this register is zero, regardless of the data in the corresponding EEPROM address.

06h EE_COPY (Full EEPROM Transfer) – AUTO CLEAR

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Address 06h	X	X	X	X	X	X	wr_full	rd_full

rd_full

* 0 = default

1 = start transfer

Description: Command to start full transfer from EEPROM to registers/RAM.

wr_full

* 0 = default

1 = start transfer

Description: Command to start full transfer from registers/RAM to EEPROM.

Note: These command bits are automatically cleared by the chip after use. The reset value of this register is zero, regardless of the data in the corresponding EEPROM address.

*For all the following registers the default values (shown with an *) will be overwritten with the values in the corresponding EEPROM address if the **auto_config** bit in the STARTUP register is set in EEPROM memory.*

07h STARTUP_1 (SPI Setup)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Address 07h	alt_startup2	eeclk_rate2	eeclk_rate1	eeclk_rate0	0	0	auto_start	auto_config

auto_config

* 0 = Does nothing.

1 = Data copied from EEPROM

Description: Automatically loads chip configuration registers and FIR coefficients into RAM.

auto_start

* 0 = Configure mode.

1 = Run mode

Description: In Run mode automatically starts filtering and sending out filtered data on the SIF interface.

Note: Bits 2 and 3 must be left at their default value of 0.

eeclk_rate

000 (110, 111) = XTAL frequency

001 = XTAL frequency/2

010 = XTAL frequency/4

011 = XTAL frequency/8

*100 = XTAL frequency/16

101 = XTAL frequency/32

Description: Clock Rate for EEPROM data transfer. Frequency is divided down as shown above. Maximum value is 5, higher values if written will default back to 000.

alt_startup2

Description: Selects alternate values for STARTUP_2 register. Default value is 0.

08h STARTUP_ 2 (Initialization delay counter)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Address 08h	init_dly7	init_dly6	init_dly5	init_dly4	init_dly3	init_dly2/ xtnd_init	init_dly1 / P1	init_dly0 / P0

init_dly

* 10h = Delay count

Description: Delay counter for the initialization and general control

xtnd_init

Description: If **alt_startup2** AND **xtnd_init** bits are set, calls for extended initialization (e.g. load calibration settings)

P0, P1

Description: Reserved for future use.

12.4 Run and Status Registers

09h ENABLE_0 (ADC Enable)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Address 09h	pcg_ch4_en	pcg_ch3_en	pcg_ch2_en	pcg_ch1_en	X	X	pll_pdn	osc_enable

osc_enable

0 = Powered Down

*1 = Oscillator enabled

Description: Enables the crystal oscillator (or external clock if configured).

PLL_enable

0 = Powered Down

*1 = PLL enabled

Description: Enables the phase locked loop.

pcg_ch*N*_en

*0 = Disabled

1 = Enabled

Description: Enables the ADC clock and system clock for channel *N*.

0Ah ENABLE_1 (AAF Enable, ADC Mode)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Address 0Ah	X	X	afe_opmadc1	afe_opmadc0	afe_opmfec4	afe_opmfec3	afe_opmfec2	afe_opmfec1

afe_opmfec*N*

* 0 = Powered Down

1 = Enabled

Description: Enables the anti-aliasing filter for channel *N*. Must be enabled for the channel to be used, this bit is for power savings on disabled channels.

afe_opmadc

* 00 = Powered Down (10uW, 5us)

01 = Sleep (2mW, 0.5us)

10 = Standby (22mW, 12 clock cycles)

11 = Active (80mW)

Description: Sets the operating mode of the ADC. These bits can be used to conserve power in duty cycle applications. The mode can be chosen to trade off power savings versus time to return to an active state (approximate values as shown).

0Bh ENABLE_2 (Sampling Enable, Serial output enable)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Address 0Bh	sif_ch_en4	sif_ch_en3	sif_ch_en2	sif_ch_en1	arec_ch_en4	arec_ch_en3	arec_ch_en2	arec_ch_en1

arec_ch_en*N*

0 = Disabled

*1 = Enabled

Description: Controls the input mux and enables sampling for channel *N.* This bit should be disabled only for power savings on unused channels. Disabling a channel will alter the effective sampling rate for the remaining active channels.

Sif_ch_en*N*

*0 = Disabled

1 = Enabled

Description: Controls the output mux. In multi-channel mode enables channel *N* in the serial output data stream. In single-channel mode identifies which channel is enabled in the serial output data stream. If two or more bits are set the lowest channel set will be output.

0Ch PLL_SIF_STAT (PLL status, serial interface status)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Address 0Ch	X	X	X	X	X	X	ism_pll_lock	pll_lock

pll_lock – READ ONLY

* 0 = Not locked.

1 = Locked.

Description: Indicates PLL lock status.

ism_pll_lock – AUTO SET, may be reset by user

* 0 = Not locked.

1 = Locked.

Description: Indicates initialization lock status.

0Dh EE_VAL (EEPROM Status Register Value) – READ ONLY

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Address 0Dh	D7	D6	D5	D4	D3	D2	D1	D0

Description: Value of the EEPROM Status register. Default value = 0 at powerup.

0Eh EE_STATUS (EEPROM Status Flags) – *Bits are autoset by the chip, can only be reset by the user*

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Address 0Eh	igc_done_xtdinit	igc_done_ism	wr_full_done	rd_full_done	spim_eebusy	spim_eestat	spim_wr_done	spim_rd_done

Default value= 00h.

These flags can only be set by the chip. They can only be cleared by writing a zero to the desired location.

spim_rd_done = Read from EEPROM complete.

spim_wr_done = Write to EEPROM complete.

spim_eestat = EEPROM status read complete.

spim_eebusy = EEPROM busy caused abort of attempted read/write.

rd_full_done = Full read from EEPROM complete.

wr_full_done = Full write to EEPROM complete.

igc_done_ism = Initialization sequence complete.

igc_done_xtdinit = Extended initialization sequence complete.

Description: Status flags for data transfers to/from EEPROM.

0Fh ADC_STATUS0 (ADC out of range, high or low) – READ ONLY

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Address 0Fh	X	X	X	X	adc_oo4	adc_oo3	adc_oo2	adc_oo1

adc_00*N*

* 0 = Within range.

1 = Out of range, high or low.

Description: Indicates an out of range condition for the ADC on channel *N*.

10h ADC_STATUS1 (ADC out of range, specific) – READ ONLY

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Address 10h	adc_un4	adc_un3	adc_un2	adc_un1	adc_ov4	adc_ov3	adc_ov2	adc_ov1

adc_ov*N*

* 0 = No overflow.

1 = ADC overflow, out of range, high.

Description: Indicates an overflow condition for the ADC on channel *N*.

adc_un*N*

* 0 = No underflow.

1 = ADC underflow, out of range, low.

Description: Indicates an underflow condition for the ADC on channel *N*.

12.5 Global Configuration Registers

Table 17. Control Register listing (Global Configuration)

Hex*	Register Name	Description
0011h	**PLL_CTRL_0**	PLL Pre-divider, frequency range.
0012h	**PLL_CTRL_1**	PLL loop divider.
0013h	**ADC_CLK_RATE**	Clock rate for ADC, CRC and AREC.
0014h	**SYS_CLK_CTRL**	System Clock control.
0015h	**SPI_CTRL**	Set single-, multi-channel mode
0016h	**SPI_MON**	Monitor internal data transfers
0017h	**EE_STADDR**	EE start address for block transfers (byte0)
0018h	**EE_STADDR**	EE start address for block transfers (byte1)
0019h	**CHIP_STADDR**	Chip start address for block transfers (byte0)
001Ah	**CHIP_STADDR**	Chip start address for block transfers (byte1)
001Bh	**END_ADDR**	Ending address for block transfers (byte0)
001Ch	**END_ADDR**	Ending address for block transfers (byte1)

11h PLL_CTRL_0 (PLL pre-divider and range)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Address 11h	X	pll_range	pll_m5	pll_m4	pll_m3	pll_m2	pll_m1	pll_m0

pll_m

Description: A 6-bit number designating the value of the PLL pre-divider (M). Default value is 1.

pll_range

0 = 20 – 100 MHz

*1 = 100 – 200 MHz

Description: Set the range of the PLL clock which supplies the ADC and system clocks.

12h PLL_CTRL_1 (PLL loop divider)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Address 12h	X	X	pll_n5	pll_n4	pll_n3	pll_n2	pll_n1	pll_n0

Pll_n

Description: A 6-bit number designating the value of the PLL loop divider (N). Default value is 10.

13h ADC_CLK_RATE (ADC Clock Rate)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Address 13h	X	X	X	X	X	afe_clk_inv	adcclk_rate1	adcclk_rate0

adcclk_rate

*00 = PLL clock/2

01 = PLLCLK/4

10 = PLLCLK/8

11 = PLLCLK/16

Description: Clock for the analog front end and ADC blocks.

Afe_clk_inv

*0 = No inversion

1 = Inverted

Description: Inverts the clock input to the ADC. This setting should not be altered.

14h SYS_CLK_CTRL (System Clock Control)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Address 14h	X	X	X	csifee_en	X	sysclk_rate2	sysclk_rate1	sysclk_rate0

sysclk_rate

*000 = PLL clock rate

Description: System clock. Frequency is PLLCLK/2^N, where N is the 3-bit value. Maximum value for N is 6 (divide by 64).

csifee_en

0 = Disabled

*1 = Inverted

Description: Enables clk_sifee, the clock for EEPROM transfers.

15h SPI_CTRL (Serial Interface Control)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Address 15h	X	reserved	fast_ch1	fast_ch0	sif_autoinc	sif_par	sif_singlech	ram_run_mode

ram_run_mode

*0 = Disabled

1 = Enabled

Description: Keeps RAM contents updated. Disable only during access to internal RAM from the SPI bus in configure mode. Usually will be enabled with run mode once the coefficient RAMs have been configured.

sif_singlech

*0 = multi-channel mode

1 = Single channel mode

Description: Sets configuration of output data in run mode.

sif_par

*0 = No parity

1 = Parity enabled

Description: If set and in multi-channel mode, each channel's MSB will toggle so the total number of "ones" is always odd.

sif_autoinc

*0 = Disable

1 = Enable

Description: Enable address autoincrement. If set, on the next read/write cycle the address data can be followed by multiple data bytes.

fast_ch

*00 = Channel 1

01 = Channel 2

10 = Channel 3

11 = Channel 4

Description: Identifies the channel with the fastest sample rate. This channel is used to provide the DRDY signal. The user must ensure this channel is correctly identified and that the corresponding channel is enabled, otherwise missed data samples will result. The value will be correctly set by the Quickfilter Pro Software, but if the chip configuration is dynamically altered the user must ensure this value is correctly maintained.

16h SPI_MON (SPI Monitor) - *For factory use only*

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Address 16h	X	X	X	X	X	X	mon_ee_sifn	en_sifee_mon

en_sifee_mon

*0 = Disable

1 = Enable

Description: Allows monitoring of internal bus during transfers.

Mon_ee_sifn

*0 = Monitor SIF

1 = Monitor EEPROM

Description: Selects which bus is monitored.

17h EE_STADDR (EEPROM Starting address - LSB)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Address 17h	addr7	addr6	addr5	addr4	addr3	addr2	addr1	addr0

18h EE_STADDR (EEPROM Starting address - MSB)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Address 18h	X	X	X	X	addr11	addr10	addr9	addr8

Description: Starting address in EEPROM for block transfers.

19h CHIP_STADDR (Chip Starting address - LSB)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Address 19h	addr7	addr6	addr5	addr4	addr3	addr2	addr1	addr0

1Ah CHIP_STADDR (Chip starting address - MSB)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Address 1Ah	X	X	addr13	addr12	addr11	addr10	addr9	addr8

Description: Chip starting address for block transfers.

1Bh END_ADDR (Destination ending address - LSB)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Address 1Bh	addr7	addr6	addr5	addr4	addr3	addr2	addr1	addr0

1Ch END_ADDR (Destination ending address - MSB)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Address 1Ch	X	X	addr13	addr12	addr11	addr10	addr9	addr8

Description: Destination ending address for block transfers.

12.6 Global Maintenance 1 Registers

Table 18. Control Register listing (Global Maintenance 1)

Hex*	Register Name	Description
001D – 0024h	**SCRATCH**	User scratch pad.
0025h	**SU_UNLOCK**	Lock bit for test/maintenance (factory use only)
0026h	**GLBL_SRST**	Global soft resets
0027h	**ADC_CTRL**	ADC control.
0028h	**AREC_CTRL**	AREC control.
0029h	**PMUX**	Test mux (factory use only)
002Ah	**DEBUG**	Debug (factory use only)
002Bh	**PCG_MNTNC**	Clock test (factory use only)
002Ch	**CAL_AFE**	Calibration (reserved for future use)
002Dh	**BIST_CTRL**	BIST control register (factory use only)
002Eh	**BIST_STATUS_0**	BIST status register (factory use only)
002Fh	**BIST_STATUS_1**	BIST Status register (factory use only)

1D - 24h SCRATCH (User scratchpad)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Addresses 1D -24h	D7	D6	D5	D4	D3	D2	D1	D0

Description: 8 bytes of space reserved for user functions. Since the 128 bytes of user data in EEPROM are not copied over to RAM/registers these 8 bytes can be used to access the data (or any other data as required). See Chapter 11 for further information.

25h SU_UNLOCK (Test/Maintenance unlock) - *Factory use only*

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Address 25h	X	X	X	X	X	X	X	su_unlock

su_unlock

*0 = Locked

1 = Unlocked

Description: This bit can be read. Writing to this bit will lock the device. Locks the registers designated as “Locked”.

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26h GLBL_SRST (Global soft resets) - *Factory use only*

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Address 26h	X	X	X	pmux_srst	arec_srst	spim_rst	ilgc_srst	pcg_srst

*0 = Default

1 = Reset

Description: Soft reset of internal blocks. User resets can be performed in register FULL_SRST (02h).

27h ADC_CTRL (ADC control) - LOCKED

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Address 27h	X	X	X	X	afe_dcr_en	afe_adc_shin	afe_sub_samp1	afe_sub_samp0

28h AREC_CTRL (ADC Pipeline latency) - LOCKED

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Address 28h	X	X	X	X	D3	D2	D1	D0

Description: Programmable ADC pipeline latency. Default value is 9, allowable range is 6 – 10.

29h PMUX (Test Mux) – *Factory use only* (Default value = 0)

2Ah DEBUG (Debug mode) – *Factory use only* (Default value = 0)

2Bh PCG_MNTNC (PCG maintenance) – *Factory use only* (Default value = 0)

2Ch CAL_AFE (AFE Calibration) – *Factory use only* (Default value = 1)

2Dh BIST_CTRL (BIST control) – *Factory use only* (Default value = 0)

2Eh BIST_STATUS_0 (BIST status) – *Factory use only* (Default value = 0)

2Fh BIST_STATUS_1 (BIST status) – *Factory use only* (Default value = 0)

12.7 Channel-specific Registers

Table 19. Channel-specific Register Map

Channel 1	Channel 2	Channel 3	Channel 4	Function
0030h - 0031h	0060h - 0061h	0090h - 0091h	00C0h – 00C1h	Run & Status
0032h – 0050h	0062h – 0080h	0092h – 00B0h	00C2h – 00E0h	Configuration
0051h – 0059h	0081h – 0089h	00B1h – 00B9h	00E1h – 00E9h	Maintenance
005Ah – 005Fh	008Ah – 008Fh	00Bah – 00BFh	00EAh – 00EFh	*Reserved*

The following descriptions show the address for Channel 1. The maps for the other three channels are identical with address offsets of 30h for Channel 2, 60h for Channel 3 and 90h for Channel 4, as shown in the table above.

Run and Status Registers

30h CH1_PGA (Programmable Gain Amplifier Setting, FIR bypass)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Address 30h	X	X	X	fir_0_1_bypass	X	X	pga_gain1	pga_gain0

pga_gain
* 00 = 1
01 = 2
10 = 4
11 = 8
Description: Sets the individual gain of the programmable gain amplifiers. The four settings are 1x 2x 4x or 8x the incoming signal.

fir_0_1_bypass
0 = In-circuit
*1 = Bypassed
Description: Bypasses the main FIR filter (filter 1).

31h CH1_STAT (Channel status) - AUTOSET

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Address 31h	fir_outsat1	fir_outsat0	fir_inbuf_over1	fir_inbuf_over0	X	adc_un	adc_ov	adc_oo

Once set these bits retain their value until reset by the user.
adc_oo
*0 = In range
1 = Out of range
Description: ADC out of range, high or low.

adc_ov
*0 = No overflow
1 = Overflow
Description: ADC out of range, high.

adc_un
*0 = No underflow
1 = Underflow
Description: ADC out of range, low.

fir_inbuf_over0
*0 = No overflow
1 = Overflow
Description: FIR, filter 0, input buffer overflow flag.

fir_inbuf_over1
*0 = No overflow
1 = Overflow
Description: FIR, filter 1, input buffer overflow flag.

fir_outsat0

*0 = Not saturated

1 = Saturated

Description: FIR output saturation flag, filter 0.

fir_outsat1

*0 = Not saturated

1 = Saturated

Description: FIR output saturation flag, filter 1.

Configuration Registers

32h CH1_CFG (Channel configuration)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Address 32h	fir_0_0_bypass	fir_0_1_enable	fir_0_0_enable	cic_0_bypass	X	chpc_calph0	chpc_inv0	aaf_freq0

aaf_freq

*0 = 0.5MHz

1 = 3MHz

Description: Anti-aliasing filter cutoff frequency select.

chpc_inv0

*0 = No invert

1 = Invert

Description: Inverts the input signal using the chopper circuit. Do not alter. – *for factory use only*

chpc_calph0

*0 = Default

1 = Use calibrated chopper phase

Description: Use calibrated chopper phase. Do not alter. – *for factory use only*

cic_0_bypass

0 = No bypass

*1 = Bypass

Description: Bypasses the CIC module. Do not alter. – *for factory use only*

fir_0_0_enable

0 = Disable

*1 = Enable

Description: Enable FIR operation, filter 0.

fir_0_1_enable

0 = Disable

*1 = Enable

Description: Enable FIR operation, filter 1.

fir_0_0_bypass

0 = In-circuit

*1 = Bypassed

Description: Bypasses the FIR filter (filter 0).

33h AREC_1_GAIN (AREC gain control)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Address 33h	D7	D6	D5	D4	D3	D2	D1	D0

34h AREC_1_GAIN (AREC gain control)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Address 34h	D15	D14	D13	D12	D11	D10	D9	D8

Description: AREC gain control, default value = 4000. This is a function of the CIC “R” value and along with CIC_SHIFT (3Ah) is calculated automatically by the Quickfilter Pro software.

35h CHPC_1_DIV (Chopper divider setting)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Address 35h	D7	D6	D5	D4	D3	D2	D1	D0

36h CHPC_1_DIV (Chopper divider setting)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Address 36h	D15	D14	D13	D12	D11	D10	D9	D8

Description: Sets the frequency for the chopper circuit. Default value = 0, which turns off the chopper circuit. When a value is written here the chopper frequency is equal to the ADC_CLK divided by this value.

37h CIC_1_R (CIC decimation, R value)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Address 37h	D7	D6	D5	D4	D3	D2	D1	D0

38h CIC_1_R (CIC decimation, R value)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Address 38h	D15	D14	D13	D12	D11	D10	D9	D8

39h CIC_1_R (CIC decimation, R value)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Address 39h	X	X	X	X	X	X	X	D16

Description: CIC decimation rate factor minus 1 (R-1), default value = 8. Effective sampling rate for the channel is the ADC_CLK divided by (Number of channels * 4). See Section 7.2)

3Ah CIC_1_SHIFT (CIC shift)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Address 3Ah	X	D6	D5	D4	D3	D2	D1	D0

Description: CIC shift value, default; value = 0. This is a function of the CIC “R” value and along with AREC_GAIN (33h, 34h) is calculated automatically by the Quickfilter Pro software.

Note: The following registers (3Bh – 50h) have values generated by the Quickfilter Pro Design Software. Manual alteration of these registers is not recommended, the descriptions are for reference only.

3Bh FIR_0_0_CTRL (FIR Control, filter 0)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Address 3Bh	fir_0_0_decimf2	fir_0_0_decimf2	fir_0_0_decimf1	fir_0_0_decimf1	X	fir_0_0_oddf2	fir_0_0_oddf1	fir_0_0_f2_enable

fir_0_0_f2_enable
*0 = Disable
1 = Enable
Description: Enable the second filter block, f2.

fir_0_0_oddf1
*0 = Disable
1 = Enable
Description: Set an odd number of taps for f1.

fir_0_0_oddf2
*0 = Disable
1 = Enable
Description: Set an odd number of taps for f2.

fir_0_0_decimf1
Description: Decimation value for f1. Default value = 0, values in range 0 – 3.

fir_0_0_decimf2
Description: Decimation value for f2. Default value = 0, values in range 0 – 3.

3Ch FIR_0_0_NMIN_F1 (Minimum storage address for f1)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Address 3Ch	X	addr6	addr5	addr4	addr3	addr2	addr1	addr0

Default value = 0

3Dh FIR_0_0_NMAX_F1 (Maximum storage address for f1)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Address 3Dh	X	addr6	addr5	addr4	addr3	addr2	addr1	addr0

Default value = 7F
Description: Minimum and maximum data storage (tap) address values for f1.

3Eh FIR_0_0_CMIN_F1 (Minimum coefficient storage address for f1)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Address 3Eh	X	X	addr5	addr4	addr3	addr2	addr1	addr0

Default value = 0

3Fh FIR_0_0_CMAX_F1 (Maximum coefficient storage address for f1)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Address 3Fh	X	X	addr5	addr4	addr3	addr2	addr1	addr0

Default value = 3F

Description: Minimum and maximum coefficient storage address values for f1.

40h FIR_0_0_NMIN_F2 (Minimum storage address for f2)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Address 40h	X	addr6	addr5	addr4	addr3	addr2	addr1	addr0

Default value = 0

41h FIR_0_0_NMAX_F2 (Maximum storage address for f2)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Address 41h	X	addr6	addr5	addr4	addr3	addr2	addr1	addr0

Default value = 7F

Description: Minimum and maximum data storage (tap) address values for f2.

42h FIR_0_0_CMIN_F2 (Minimum coefficient storage address for f2)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Address 42h	X	X	addr5	addr4	addr3	addr2	addr1	addr0

Default value = 0

43h FIR_0_0_CMAX_F2 (Maximum coefficient storage address for f2)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Address 43h	X	X	addr5	addr4	addr3	addr2	addr1	addr0

Default value = 3F

Description: Minimum and maximum coefficient storage address values for f2.

44h FIR_0_1_CTRL (FIR Control, filter 1)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Address 44h	fir_0_1_decimf2	fir_0_1_decimf2	fir_0_1_decimf1	fir_0_1_decimf1	X	fir_0_1_oddf2	fir_0_1_oddf1	fir_0_1_f2_enable

fir_0_1_f2_enable
*0 = Disable
1 = Enable
Description: Enable the second filter block, f2.

fir_0_1_oddf1
*0 = Disable
1 = Enable
Description: Set an odd number of taps for f1.

fir_0_1_oddf2
*0 = Disable
1 = Enable
Description: Set an odd number of taps for f2.

fir_0_1_decimf1
Description: Decimation value for f1. Default value = 0, values in range 0 – 3.

fir_0_1_decimf2

Description: Decimation value for f2. Default value = 0, values in range 0 – 3.

45h FIR_0_1_NMIN_F1 (Minimum storage address for f1)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Address 45h	addr7	addr6	addr5	addr4	addr3	addr2	addr1	addr0

46h FIR_0_1_NMIN_F1 (Minimum storage address for f1)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Address 46h	X	X	X	X	X	X	X	Addr8

Default value = 0

47h FIR_0_1_NMAX_F1 (Maximum storage address for f1)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Address 47h	addr7	addr6	addr5	addr4	addr3	addr2	addr1	addr0

48h FIR_0_1_ NMAX_F1 (Maximum storage address for f1)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Address 46h	X	X	X	X	X	X	X	Addr8

Default value =1FF

Description: Minimum and maximum data storage (tap) address values for f1.

49h FIR_0_1_CMIN_F1 (Minimum coefficient storage address for f1)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Address 49h	addr7	addr6	addr5	addr4	addr3	addr2	addr1	addr0

Default value = 0

4Ah FIR_0_1_CMAX_F1 (Maximum coefficient storage address for f1)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Address 4Ah	addr7	addr6	addr5	addr4	addr3	addr2	addr1	addr0

Default value =FF

Description: Minimum and maximum coefficient storage address values for f1.

4Bh FIR_0_1_NMIN_F2 (Minimum storage address for f2)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Address 4Bh	addr7	addr6	addr5	addr4	addr3	addr2	addr1	addr0

4Ch FIR_0_1_NMIN_F2 (Minimum storage address for f2)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Address 4Ch	X	X	X	X	X	X	X	addr8

Default value = 0

Description: Minimum data storage (tap) address value for f2.

4Dh FIR_0_1_NMAX_F2 (Maximum storage address for f2)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Address 4Dh	addr7	addr6	addr5	addr4	addr3	addr2	addr1	addr0

4Eh FIR_0_1_ NMAX_F2 (Maximum storage address for f2)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Address 4Eh	X	X	X	X	X	X	X	addr8

Default value =1FF

Description: Maximum data storage (tap) address value for f2.

4Fh FIR_0_1_CMIN_F2 (Minimum coefficient storage address for f2)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Address 4Fh	addr7	addr6	addr5	addr4	addr3	addr2	addr1	addr0

Default value = 0

Description: Minimum coefficient storage address value for f2.

50h FIR_0_1_CMAX_F2 (Maximum coefficient storage address for f2)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Address 50h	addr7	addr6	addr5	addr4	addr3	addr2	addr1	addr0

Default value = FF

Description: Maximum coefficient storage address value for f2.

Maintenance Registers

51h CH1_SRST (Channel soft reset) – *For factory use. User should use FULL_SRST (02H) to reset the chip*

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Address 51h	X	X	X	fir_0_1_srst	fir_0_0_srst	txrx_0_srst	cic_0_srst	chpc_0_srst

chpc_0_srst

*0 = No action

1 = Reset

Description: Soft reset the chopper clock generator.

cic_0_srst

*0 = No action

1 = Reset

Description: Soft reset the CIC module. Clears all internal CIC registers.

txrx_0_srst

*0 = No action

1 = Reset

Description: Soft reset the tx/rx.

fir_0_0_srst

*0 = No action

1 = Reset

Description: Soft reset the FIR block, filter 0.

fir_0_1_srst

*0 = No action

1 = Reset

Description: Soft reset the FIR block, filter 1.

52h CHP_OFFSET_1 (Chopper clock phase offset) – *Factory use only*

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Address 52h	D7	D6	D5	D4	D3	D2	D1	D0

53h CHP_OFFSET_1 (Chopper clock phase offset) – *Factory use only*

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Address 53h	X	X	X	X	D11	D10	D9	D8

Default value = 95

Description: Chopper clock phase offset value.

54h AREC_OFFSET_1 (Digital offset) – *Factory use only*

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Address 37h	D7	D6	D5	D4	D3	D2	D1	D0

55h AREC_OFFSET_1 (Digital offset) – *Factory use only*

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Address 55h	D15	D14	D13	D12	D11	D10	D9	D8

Default value = C000

Description: Digital offset for the channel.

56h CAL_1_OFF (Calibration offset)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Address 56h	D7	D6	D5	D4	D3	D2	D1	D0

57h CAL_1_OFF (Calibration offset)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Address 57h	D15	D14	D13	D12	D11	D10	D9	D8

Default value = 0

Description: Offset calibration value is written here.

58h CAL_1_GAIN (Calibration gain)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Address 58h	D7	D6	D5	D4	D3	D2	D1	D0

59h CAL_1_GAIN (Calibration gain)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Address 59h	D15	D14	D13	D12	D11	D10	D9	D8

Default value = 8000

Description: Gain calibration value is written here.

5Ah – 5Fh – *Reserved*

The following registers implement similar functionality for the three remaining channels. Please refer to the descriptions above.

60h – 8Fh Channel 2 Registers *(see 30h – 5Fh for functionality)*

90h – BFh Channel 3 Registers *(see 30h – 5Fh for functionality)*

C0h – E9h Channel 4 Registers *(see 30h – 5Fh for functionality)*

12.8 Global Maintenance 2 Registers

Table 21. Control Register listing (Global Maintenance 2)

Hex*	Register Name	Description
EAh	**DIE_REV**	Metal Revision ID
EBh, ECh	**IGC_SEQADDR**	Extended Initialization Sequence Start Address
EDh	**CAL_CTRL**	Calibration Control
EEh, EFh	**CAL_DTGT**	Target Calibration Value
F0h	**DBG_TEST**	Factory Use Only
F1h - FFh		Reserved

EAh DIE_REV – Read Only

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Address EAh	D7	D6	D5	D4	D3	D2	D1	D0

Default value = C2

Description: Die revision.

Note current version of the QF4A512 is Rev A (QF4A512A) which has a die revision of C2. The previous die revision was C1.

EBh IGC_SEQADDR (Extended Initialization Sequence Start Address)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Address EBh	D7	D6	D5	D4	D3	D2	D1	D0

ECh IGC_SEQADDR (Extended Initialization Sequence Start Address)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Address ECh	X	X	X	X	D11	D10	D9	D8

Default value = F00h

Description: Starting address for an Extended Initialization Sequence (See Section 5.2).

EDh CAL_CTRL (Calibration Control)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Address EDh	X	X	X	cal_srst	cal_enab	cal_gain_mode	cal_chan_sel	cal_chan_sel

cal_chan_sel

Description: Selects the channel to be calibrated.

cal_gain_mode

*0 = Offset calibration

1 = Gain calibration

Description: Select whether to perform gain or offset calibration.

cal_enab

*0

1 = Start

Description: Write to 1 to begin calibration.

cal_srst

*0

1 = Reset

Description: Soft reset the calibration block.

EEh CAL_DTGT (Target Calibration Value)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Address EEh	D7	D6	D5	D4	D3	D2	D1	D0

EFh CAL_DTGT (Target Calibration Value)

	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Address EFh	D15	D14	D13	D12	D11	D10	D9	D8

Default value = 0

Description: Target calibration value for applied input voltage (gain calibration). Write to 0 for offset calibration.

F0h DBG_TEST – *Reserved (Factory use only) (Default = 0)*

F1h – FFh – *Reserved*

12.9 Register Listing

13. APPLICATION CIRCUITS

For more information please see Application note QFAN004 at http://www.quickfiltertech.com/html/app_notes.php

13.1 AC Coupled, Single-ended

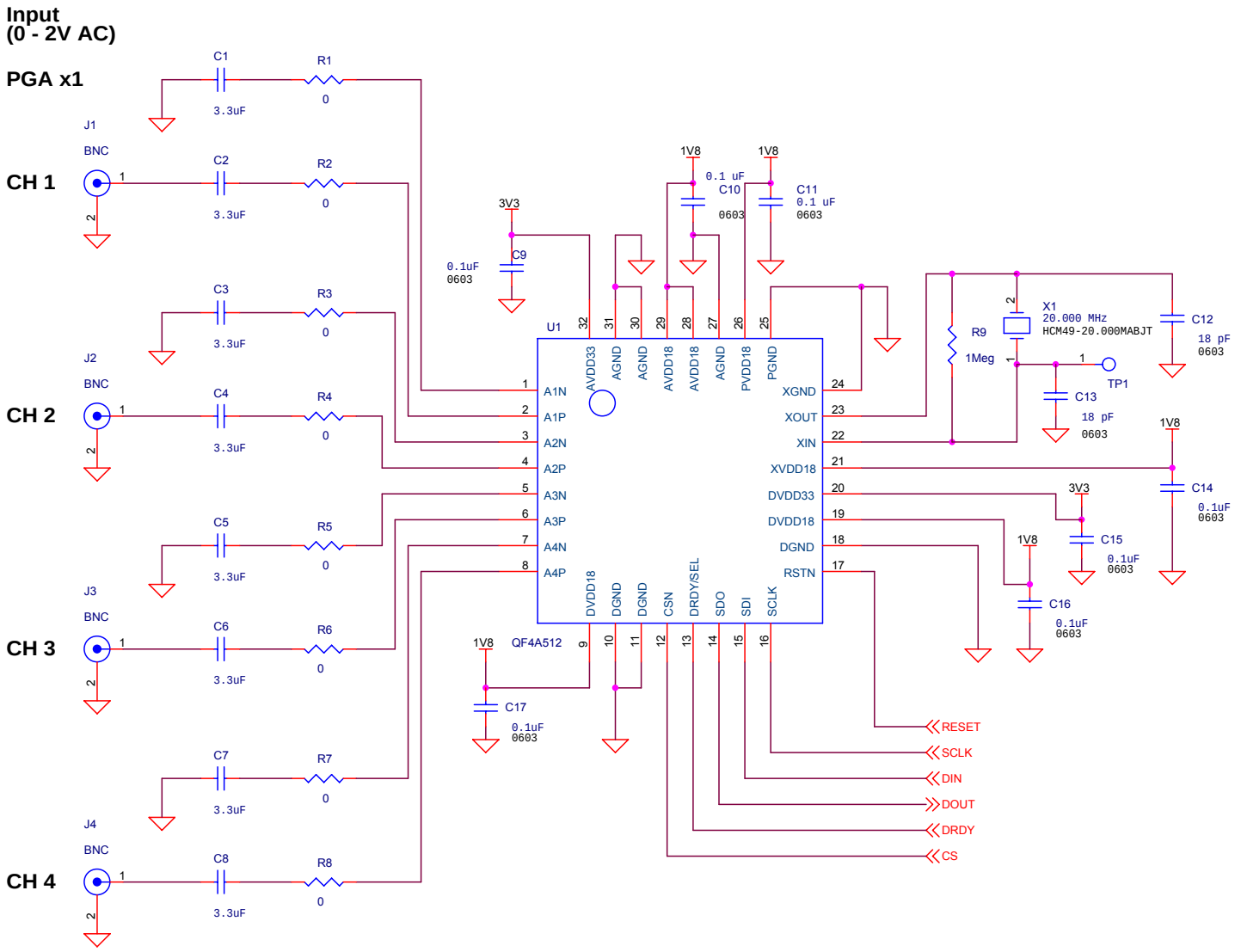


Figure 14. Application Circuit – Single-ended, ac coupled

Table 20. Example resistor values for ac-coupled, single-ended

AC-coupled, singled-ended		
Input level	R1 - R8 value	PGA setting
1V ptp	0k	x2
3.3V ptp	6.5k	x1
5V ptp	15k	x1
10V ptp	40k	x1

13.2 DC coupled, Single-ended

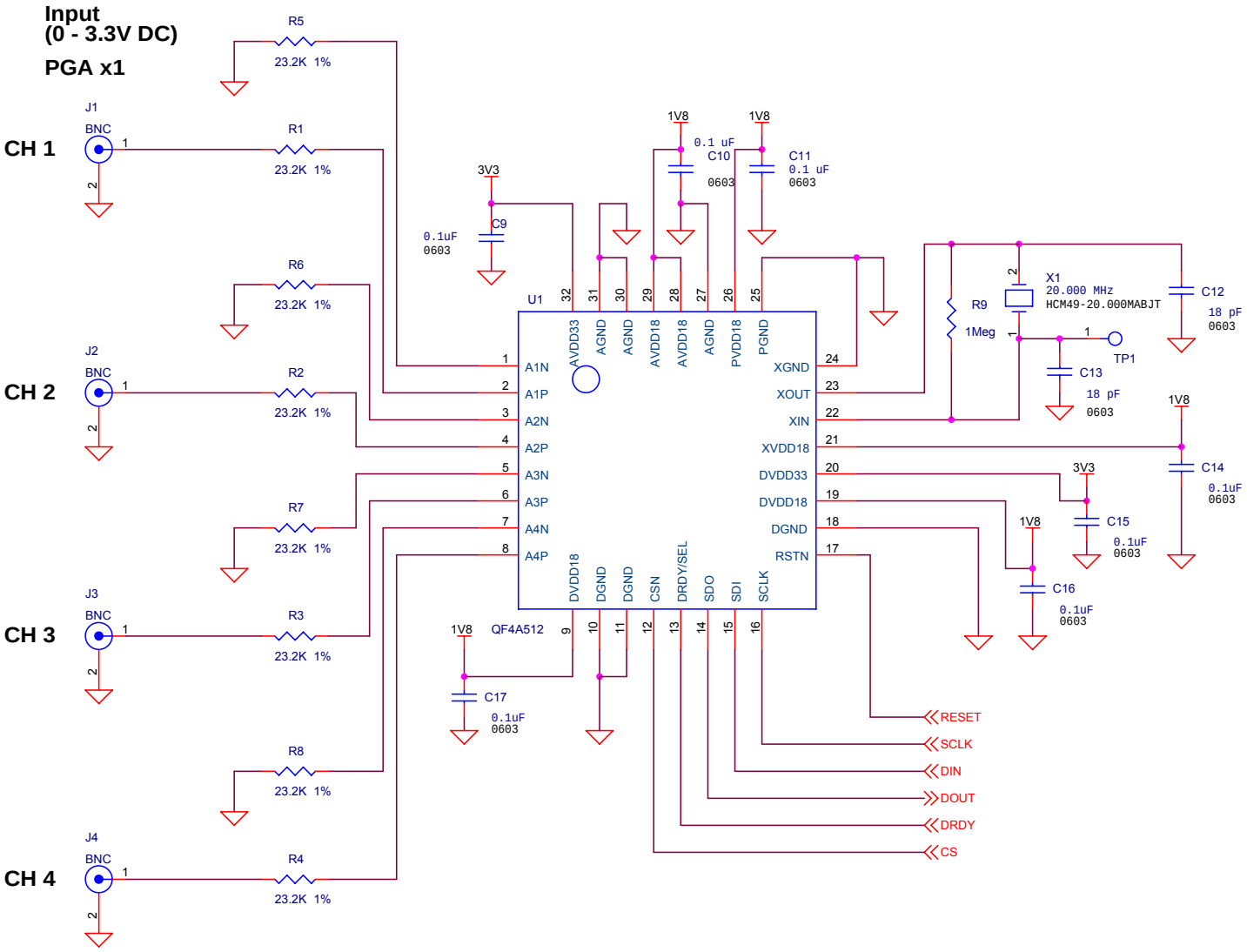


Figure 15. Application Circuit – Single-ended, dc coupled

Table 21. Example resistor values for dc-coupled, single-ended

DC-coupled, singled-ended		
Input level	R1-R8 value	PGA setting
0 – 1V	18k	x2
0 - 3.3V	23k	x1
0 – 5V	40k	x1
0 – 10V	90k	x1

13.3 AC coupled, Differential

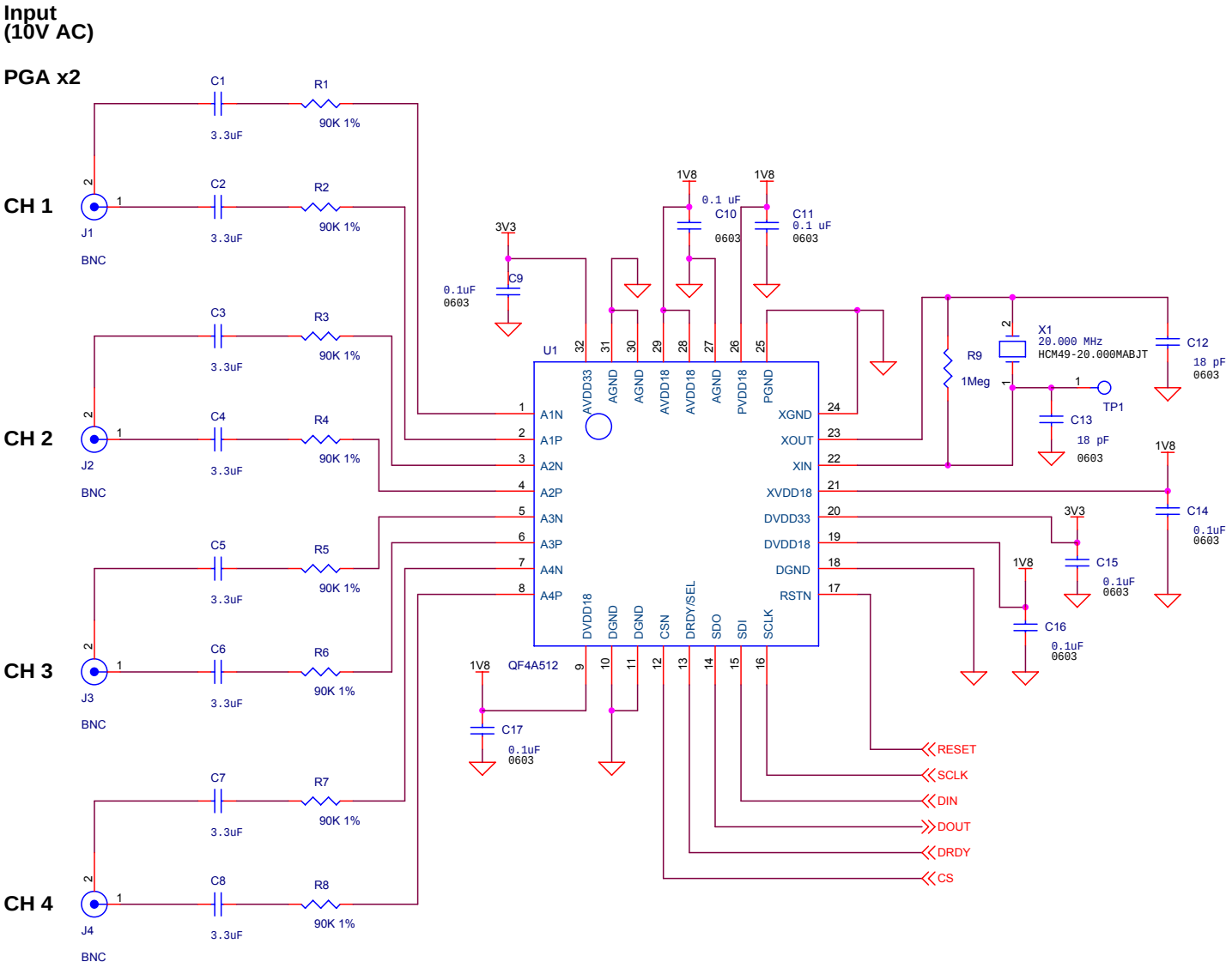


Figure 16. Application Circuit – Differential, ac coupled

Table 22. Example resistor values for ac-coupled, differential

AC-coupled, differential		
Input level	R1-R8 value	PGA setting
1V ptp	0k	x2
3.3V ptp	23k	x2
5V ptp	40k	x2
10V ptp	90k	x2

13.4 DC coupled, Differential

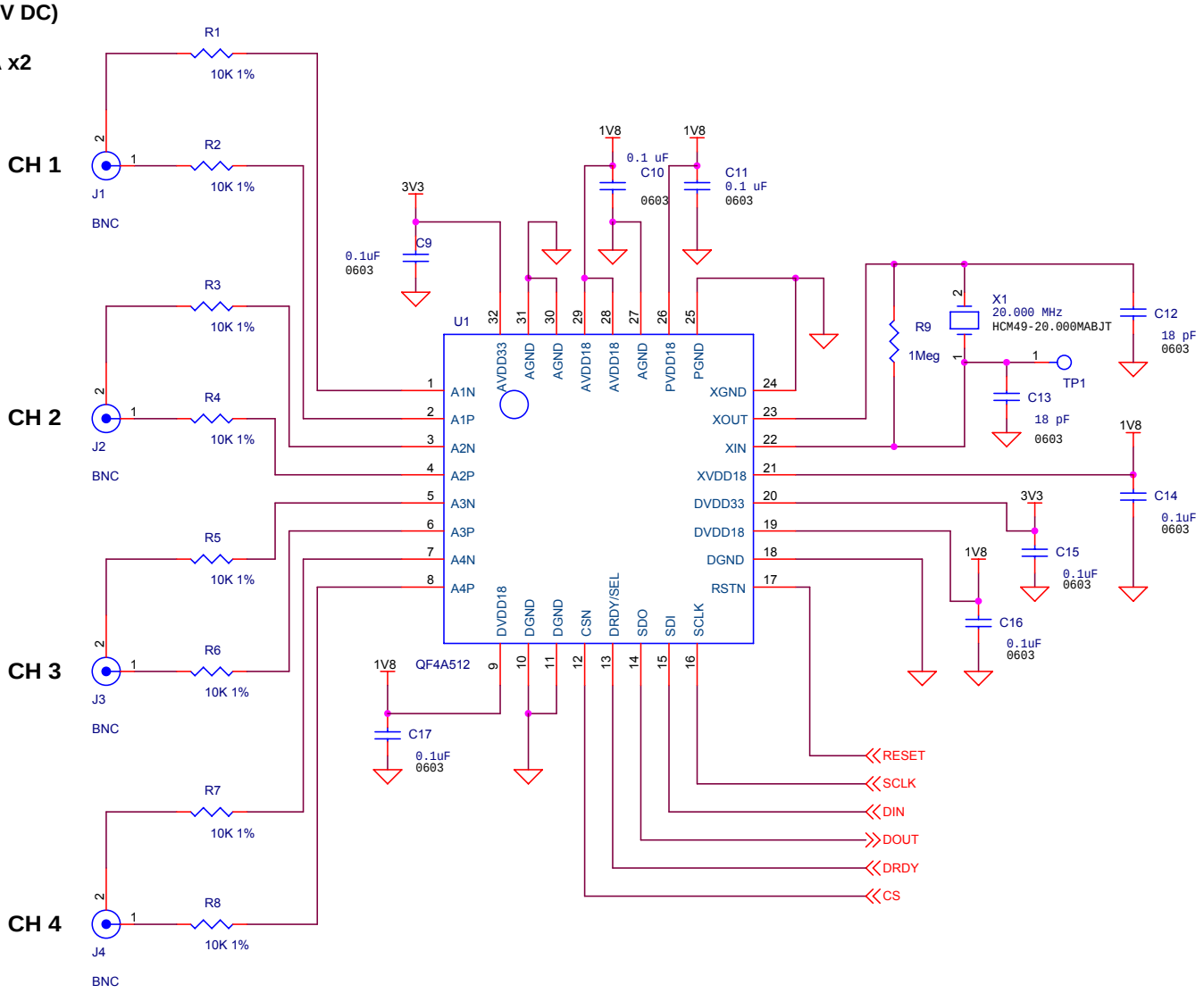


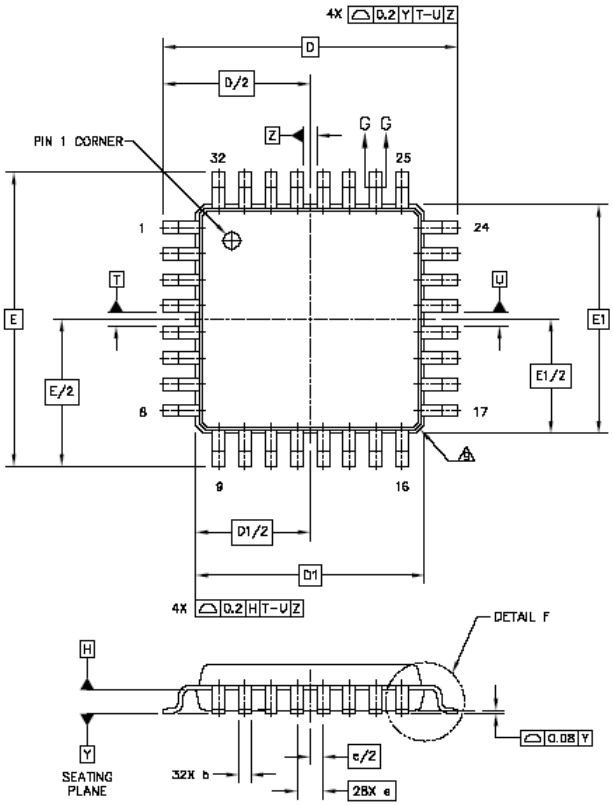
Figure 17. Application Circuit – Differential, dc coupled

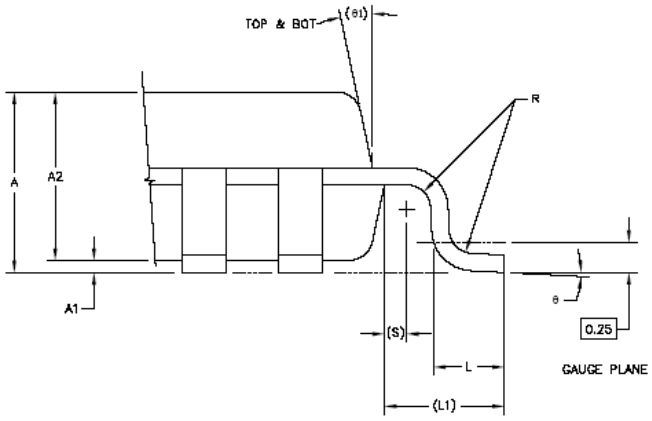
Table 23. Example resistor values for dc-coupled, differential

DC-coupled, differential		
Input Level	R1-R8 Value	PGA setting
-0.25V +0.25V	10K	x8
-0.5 to +0.5V	10K	x4
-1V to 1V	10K	x2
-2V to 2V	10K	x1
-3V to 3V	20K	x1
-3.3V to 3.3V	23K	x1
-5V to 5V	40K	x1
-10V to 10V	90K	x1
-12V to 12V	110K	x1
-15V to 15V	140K	x1
-20V to 20V	190K	x1
-24V to 24V	230K	x1
-28V to 28V	270K	x1

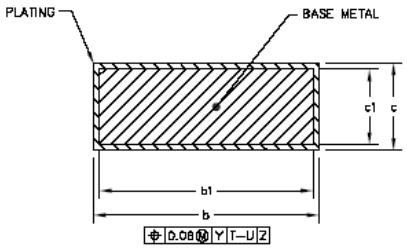
14. PACKAGING INFORMATION

7x7x1.4mm, LQFP 32, 0.8 mm Pitch POD (JEDEC)





DETAIL F



SECTION G–G

Dimension	Minimum (mm)	mm	Maximum (mm)
A	1.4		1.6
A1	0.05		0.15
A2	1.35		1.45
b	0.3		0.45
b1	0.3		0.4
c	0.09		0.2
c1	0.09		0.178
D		9 BSC	
D1		7 BSC	
e		0.8 BSC	
E		9 BSC	
E1		7BSC	
L	0.5		0.7
L1		1 REF	
R	0.15		0.25
S		0.2 REF	
θ	1°		5°
θ1		12° REF	

Notes:

1. Dimensions are in millimeters.
2. Interpret dimensions and tolerance per ASME Y14.5M-1994
3. Datum Plane H is located at bottom of lead and is coincident with the lead where the lead exits the plastic body at the bottom of the parting line.
4. Datum T, U, and Z to be determined at Datum Plane H.
5. Dimensions D and E to be determined at seating Plane Y.
6. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25 mm per side. Dimensions D1 and E1 do include mold mismatch and are determined at datum plane H.
7. Dimension b does not include Dam Bar protrusion. Dam Bar protrusion shall not cause the b dimension to exceed 0.533 mm.
8. Minimum solder plate thickness shall be 0.0076 mm.
9. Exact shape of each corner may vary from depiction.

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http://www.quickfiltertech.com