DEEPAK KUMAR GUPTA

Address (current): WD-45,Zanskar Hostel
IIT Delhi, Hauz Khas
New Delhi
Delhi.
India-110016

Email: deepakgupta.india@yahoo.com ,
Contact no (cell): +919999395257 (M)
+917882225022 (Res.)
Web: **www.cse.iitd.ac.in/~jvl072176** (office)
www.geocities.com/deepakgupta.india (personal)

RESUME

OBJECTIVE

I want to stretch myself beyond all my limits and I want to take active participation in contribution to my country in the field of science and technology.

Research area of interest:

- Analog / Mixed signal system /RF VLSI Design
- Radiation Hardened electronics design.

ACADEMIC PROFILE:

Degree / Certificate	School / College	Board/ University	Year of Passing	Rank in Group	Percentage Scored (%) / CGPA
M. TECH. , VLSI Design Tools & Technology (VDTT)	IIT, DELHI	Indian Institute of Technology (IIT) , DELHI	Completed 1st year	6th	**8.0 (SEM-I)**
				5th	**8.67 (SEM-II)**
B.E. (Electronic & Tele Communication Engineering)	Bhilai Institute of Technology (BIT)	Pt. Ravi Shankar Shukla University (PRSUV)	2004	1st	**82.24%**
Std. XII	BSP Higher Secondary School No.1, Sector-6	Madhya Pradesh Board	2000	1st	**84.22%**
Std. X	BSP Higher Secondary School No.1, Sector-6	Madhya Pradesh Board	1998	1st	**78.8%**

TRAINING UNDERGONE

- One year OCEs (Orientation Course for Engineers) training on Nuclear power plant operation and maintenance under Department of atomic Energy (DAE)
- Training on "Deep Submicron CMOS IC design "Dr. Harry Veendrick (NXP,Phillips Research)
- 15 days Course and Lab work on " IC Processing " (CEERI Pilani)

INDUSTRIAL VISITS

- Bhilai Steel Plant (SAIL's unit)
- Hydral Power Plant at Gandhi sagar Dam –Rajasthan
- Nuclear Power Plants-Kakrapara Atomic Power Station (KAPS) Rajasthan Atomic power station (RAPS),Kaiga Generating Station-1 to4 (KGS)
- Electronic Corporation of India Limited (ECIL), Hyderabad.

TECHNICAL SKILLS-SET

- Programming Language : VHDL,C, C++
- Tools (cadence) : 1.Custom Design Schematic Editor :ICFB
  2. Layout Editor : Assura Virtuso
  2.Formal Verification : Conformal
  (Synopsis) : 3-D Semiconductor Device simulator : davinci
- FPGA Prototyping : xilinx ISE 8.2.1
- HDL simulator : GHDL
- Process controllers : Programming of ASCON process controllers
- Commissioning of Feedback control system sensors and transducer
- Simulator testing and Negative logic checks**.**

INDUSTRIAL PROJECT /PRESENTATION

- **NTC(Nuclear Training Center)** : Project on Modification in Storm Drainage System in KAPS as per G.P.C.B. Norms under guidance of Mr. P. Shrikant (STE(C))

UNDERGRADUATE PROJECT/PRESENTATION

- Data Encryption System, under the guidance of Dr.M.K.Kowar (HOD, ELEX &TC, BIT, Durg)

POST GRADUATION THESIS

- Design of high speed (2Gbps) transmitter and buffer design for LVDS(Low Voltage Differential Signaling)IEEE standard.
  (under the guidance of Prof Shouri Chatterjee (IIT Delhi) and Mr. Sunil Chandra (NXP Semiconductor)

SEMINAR/PRESENTATION DURING POST GRADUATION

- Nuclear and Space Radiation :Effects on ICs and Solutions" in Departmental periodical seminar session at Indian Institute of Technology Delhi.
- * High Reliable design issue for Space, Nuclear and Military Application Departmental seminar , Journal club , IIT Delhi

  * To be presented, Date of seminar is only appointed now.

Deepak Kumar Gupta, E-mail: deepakgupta.india@yahoo.com
4-A/37/Sector-6, Bhilai, Durg, (C.G.), 490006, India, contact no +919999395257 / +917882225022

POST GRADUATE COURSE PROJECTS

1. Digital Design Laboratory : LZ77 and run length data compression implementation on FPGA under the guidance of Prof. Preeti Rnajan Panda.
Tools used : Xilinx ISE .

2. Synthesis of Digital system : generate the VHDL/Verilog code with the information available from the CDFG and the state-table under the guidance of Prof. Preeti Rnajan Panda.
Tools used : gcc (GNU compiler Collection)
3.Physical design lab : Formal veification among RTL and gate level net list *under the guidance of* ***Dr.G.S.Visweswaran***
Tools used : conformal (cadence)

4. Analog Design " High Gain Operational Transconductance Amplifier Design under the guidance of Dr.G.S.Visweswaran(Professor EE Dept.,IITD)
Tools used : cadence virtuso Analog design environment
Special Features :
Umc 90nm CMOS technology,2.5Volts,total quiescent current drawn (469µA)Topology (Folded cascode) High gain (123dB) UGB (64MHZ)Phase Margin(66º) CMRR(152.9 dB) , PSRR(138dB for positive and 179dB for Negative power supply) all testing is done with capacitive load of 0.5pF.

5. CAD of VLSI : Presentation on " CAD for Leakage Current optimisation for Thin Film Transitor " under the guidance of **Dr.Jayadeva**
Tool used : GOSAM Optimizer, Da vinci device simulator (Synopsis)

6. Memory Design and Testing : " Cache Memory Design and Architecture " *under the guidance of* ***Dr.G.S.Visweswaran***
Features: *Technology (umc 90nm,1Volt),size(65536 bits, cache size,128bits line size,,4-way set associative ,32bit data bus.32bit main memory, access time (5nsec)*

MAJOR COURSES TAKEN IN MASTER OF TECHNOLGY

Analog VLSI, MOS VLSI, CAD of VLSI, Synthesis of digital system, Memory design and testing, Mixed signal system*, CAD of RF and Microwave Devices* , Computer Architecture * , IC processing ,Microelectronics.

* course undergone in this semester.

TEACHING EXPERIENCES

- Teaching Assistantship for undergraduate's Analog electronics lab under Prof. Vinod Chandra in Indian Institute of Technology
- Teaching Assistantship for undergraduate's Digital electronics lab under Prof. Shouri Chatterjee and Prof M. Jagadesh Kumar in Indian Institute of Technology

WORK EXPERIENCE (Previous Company)

Organization	: Nuclear Power Corporation of India Limited (NPCIL) under Department of Atomic Energy
Designation	: Scientific Officer-C
Experience	: 2 years 10 months
Roll in Project/organization	: Fuel Handling System (FHS) Control maintenance Engineer

RESPONSIBILITIES (Previous Company)

- Fuel handling system control system commissioning of Kaiga Nuclear Power Project-3
- PM(Preventive Maintenance checks of process instruments) .
- Procurement of spares of process instruments for inventory management
- Automating the testing/maintenance procedures (write & run script, analysis the Results) wherever applicable.
- Prepare daily/weekly testing status report for testing.
- Knowledge transition to new team members
- Co-ordination, peer review among team members.

PERSONAL PROFILE:

DATE OF BIRTH

25th June 1983

ACHIEVEMENTS

- Secured 1st rank in Bachelor of Engg(B.E.) in college Bhilai Institute of Technology
- Occupied 1st rank in the university in 3rd SEM of B.E.
- Occupied **All India Rank-77** with **99.79 Percentile** in Graduate Aptitude Test of Engineering **(GATE)-2004** and **All India Rank 129 with 99.56 Percentile in GATE-2007**
- Selection in Prime Minister Trophy Scholarship award by BSP for excellence In academic achievement.
- Occupied first position in district level Quiz competition –BRAMHAND PRASHNOTARY
- Selected in state level Environment awareness exam conducted by ECSDS
- Felicitations in Science Project exhibitions.
- Various academic awards in school level.

HOBBIES AND INTERESTS

- Reading ,Swimming, Gardening, Painting

Deepak Kumar Gupta, E-mail: deepakgupta.india@yahoo.com
4-A/37/Sector-6, Bhilai, Durg, (C.G.), 490006, India, contact no +919999395257 / +917882225022

LANGUAGES KNOWN

- Hindi and English

CONTACT ADDRESSES

Current address	WD-45,Zanskar Hostel,IIT Delhi Hauz Khas, New Delhi-110016 Contact no- +919999395257
Permanent Address	Block no-4/A street-37, sector-6, Bhilai Nagar Dist-Durg (Chattisgarh)-490006 Contact no- (0788) 2225022/+919406253137

DECLERATION

I hereby declare that the information given above is true to best of my knowledge and belief.

Date: **Deepak Kumar Gupta**

15th August 2008