A Multi-Standard Video Compact Disk Encoder With Built-In On Screen Display

Sam-Yong Bahng, Bong-Soon Kang, Jeong-Cheol Kim
Samsung Electronics, Micro Device Business, Micro Division
Buchun, Kyunggi-Do, Korea, 421-130

David Tanwei Chung, James Y. Pi,
Samsung Electronics, Los Angeles Design Center,
10805 Holder Street, Suite 170. Cypress, California, 90630, U. S.A.

Thomas C. Tang, Tak Wong
Independent Consultant

Abstract
This paper describes a multi-standard Video Encoder chip for video compact disk (VCD) and digital video disk (DVD) applications. The chip converts 8-bit CCIR656 [1] or CCIR601 [2] inputs from digital video source into NTSC or PAL baseband TV signals in both S-video and CVBS composite video. A vertical filter is implemented on the chip which smooths the single field MPEG1 video to enhance the picture quality. This chip also contains on-screen display (OSD) circuitry that can display 10 rows by 25 columns of characters at the video output. The font can be changed through one layer metal mask change. This chip can be directly interface with most MPEG decoders and is therefore ideal for VCD applications. The chip was fabricated using 0.8-micron, double matal CMOS process and was functioning in the first silicon.

Functional Description
A functional block diagram of this multi-standard Video Encoder chip is illustrated in Figure (1). The video data input port accepts 8-bit CCIR656 or 16-bit CCIR601 digital data. These luminance (Y) and chrominance (C) data are demultiplexed after passing through the vertical filter. The luminance processing path includes crisping, gain conversion, interpolation and band-limiting functions. The sync and OSD are inserted before interpolation filtering. The luminance data is gain and offset adjusted so its output will be at the correct NTSC or PAL level. The chrominance processing path performs gain conversion, band limiting, interpolation and modulation. The color burst gate is inserted and the 13.5 Mhz Cb and Cr data are up sampled to 27 Mhz through an interpolation filter. These two color difference components are then quadrature modulated by the subcarrier which is generated from a 32-bit digital subcarrier synthesizer. Finally, chrominance and luminance data are added to generate the CVBS composite. Three 10-bit DACs are used to convert the digital Y, C and CVBS data to analog form at 27 Mhz.

This chip also consists of a 10-row by 25-column character On-Screen-Display RAM circuit to address a 250 character font ROM OSD Generator. The ROM contains English (upper case and lower case), Korean characters, Japanese alphabets, numbers and symbols.
Slave and master timing generation are supported by this chip. In the slave mode operation, the video timing is synchronized to the EAV[3] data (CCIR 656), or the sync signal on the bi-directional horizontal ($\overline{\text{HSYN}}$) and vertical sync ($\overline{\text{VSYN}}$) pins. The field flag (ODD) is the odd or even field indicator. In the master mode operation, this chip generates these three reference sync signals.

An 8-bit microprocessor interface is provided to program control functions, such as master or slave mode selection, filter bandwidth selection, luminance data coring and crisping functions, OSD background character color selection, etc. The OSD characters are also programmed via this microprocessor interface.

A 27 Mhz TTL clock (CKI27), a 13.5 Mhz CMOS clock or a 13.5 Mhz crystal (XTLI) can be used to supply the internal clock The chip provides an output clock (CKO) which can be used as a pixel clock. An internal clock doubler and divide-by-2 divider generates the output clock which can be either 27 Mhz or 13.5 Mhz. The selection of the output clock frequency is also user-programmable.

Vertical Filter
The vertical filter is a field interpolation filter which is very useful for single field input sources, such as MPEG1. For single field video sources, this chip uses the input for odd field without change. The even field is interpolated from the input. The vertical interpolation filter creates the even field with smooth edge along diagonal and vertical directions. It generates the current video line output using the current and previous line inputs. For interlaced video, both odd and even fields are interpolated from the input.

The Luma Path Crisping Circuit
After vertical filtering, the crisping circuit in the luma path further improves video quality. The crisping circuit is designed to reduce mosquito effect in MPEG1 video. A functional block diagram of the crisping circuit is shown in Figure

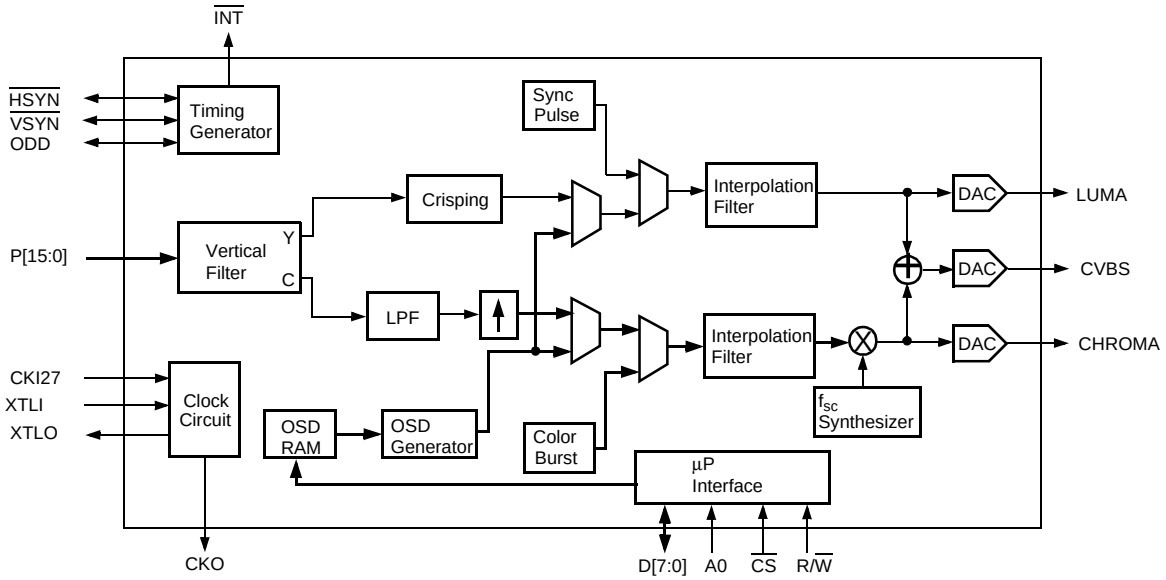


Figure (1). Functional Block Diagram

(2). It consists of a band separation circuit, a coring circuit, and a gamma correction ROM. The luminance data is first separated into high and low frequency components. The low amplitude signals embedded in the high frequency component can optionally be suppressed by the coring circuit. This boosts the low amplitude detail signals and gives a better and crisper image. Furthermore, an additional gamma ROM can apply gamma correction to the high frequency component after the coring function. Two selections are provided for gamma correction. One has large peaking, the other has small peaking. Also, gamma correction can be disabled by programming a control bit. Finally, the high and low frequency components are recombined.

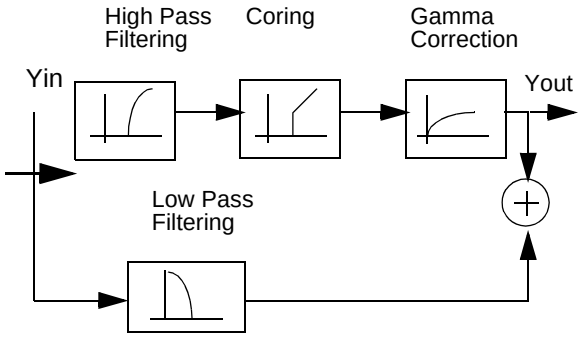


Figure (2) Crisping Circuit Block Diagram

Luminance Interpolation Filter

After the crisping circuit, the luminance data is gain and offset adjusted to give the correct NTSC or PAL signal level at the DAC output. The luminance multiplexers not only passes the luminance data, but also performs wave shaping for sync pulse and passing of OSD data. Before going to the DAC, the luminance data is interpolated to 27 Mhz. This up sampling will simplify the external analog reconstruction filter. The overall luminance frequency response is given in Figure (3).

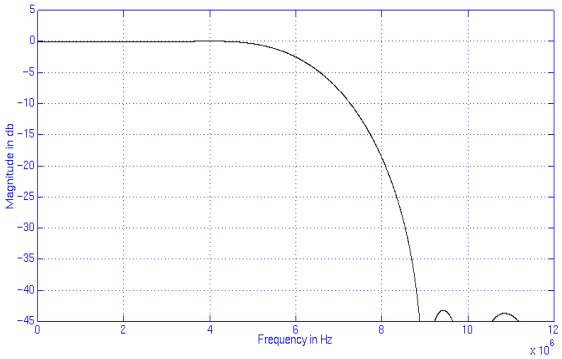


Figure (3) Luminance Frequency Response

Chrominance Path Filters

The Chrominance data passes through a low pass filter (LPF) whose bandwidth can be selected via the microprocessor interface. The bandwidth can be 1.1 Mhz, 1.45 Mhz or 1.75 Mhz. The chroma Cb/Cr data is interpolated from 6.75 Mhz to 13.5 Mhz, and then gain adjusted. The Cb/Cr data is then demultiplexed to Cb and Cr paths. OSD character and background colors are inserted into the Cb and Cr data paths. The color burst gate is also inserted and the 13.5 Mhz Cb and Cr data are then up sampled to 27 Mhz The overall frequency response of the chrominance path filters is shown in Figure (4).

On Screen Display (OSD)

The On Screen Display (OSD) allows the user to overlay characters over the video. The desired characters and their positions are programmed on the display screen via the 8-bit microprocessor interface. Figure (5) shows a block diagram of the OSD. This

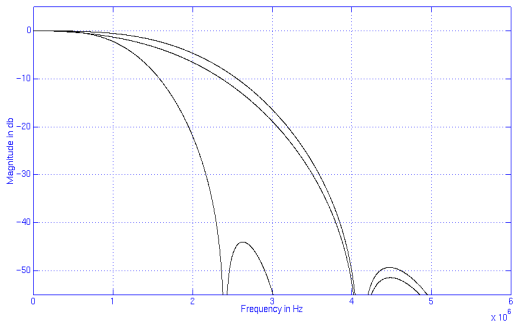


Figure (4) Chrominance Filter Frequency Response

block consists of a character display buffer RAM, a character generation font ROM, character location generator, character boundary location generation and the OSD shaping circuits. The on chip Timing Generator Pixel Counter and Line Counter generate controls to define the OSD display area. The RAM address defines where the character will be displayed. The RAM data output acts as the pointer to select a particular character from the Character Font ROM. The character location generator converts the 12-bit character font ROM outputs to serial character streams, while the boundary location generator creates a boundary to surround the character. Finally, the OSD shaping circuits performs character color selection and background color selection. The OSD Y, Cb and Cr outputs are properly shaped by band-limited filters to reduce the ringing caused by the abrupt amplitude changes. The OSD supports four different colors for the character display, i.e., white, cyan, green and magenta. It also supports two different background colors, blue and black.

On Screen Display Area

The OSD area is confined to a rectangle as shown in Figure (6) Within the rectangle, the area is further divided evenly into 10 rows and 25 columns. The font selection RAM can be viewed as a two dimensional array that maps to the 10x25 character cells. Each RAM address contains the font code corresponding to the character to be displayed at the particular cell. The size of each font is 12 x14 pixels. A boundary is added to each character to make the total character size 14 x 16 pixels.

Design Methodology

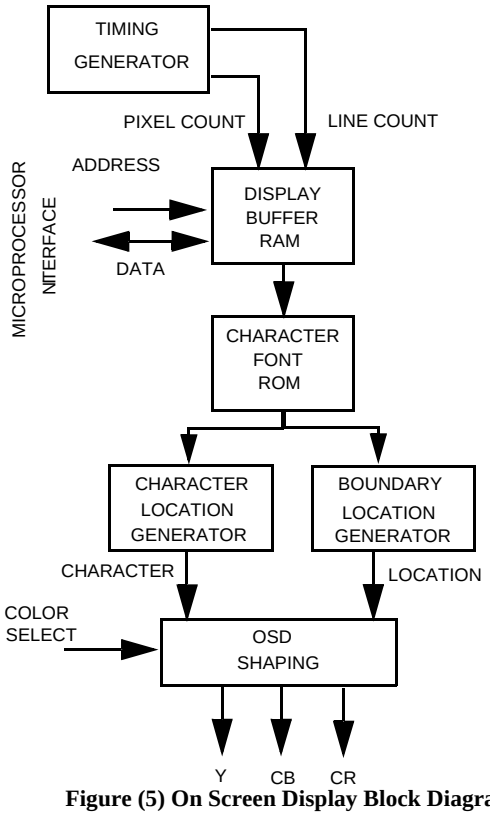
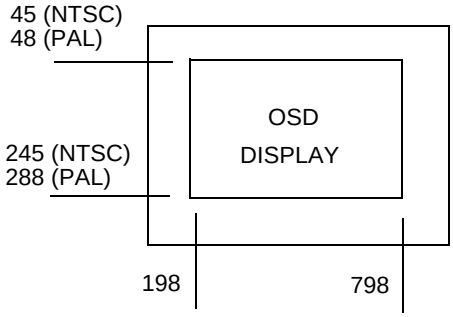


Figure (5) On Screen Display Block Diagram



Note: Line numbers are for odd field
Pixel numbers are referenced to the midpoint of the leading edge of the horizontal sync.

Figure (6) OSD Display Area

The Verilog HDL language was used to create behavioral models for the entire chip. Then the Synopsys Design Compiler was used to synthesize most of the digital portion of the chip, some digital blocks, such as all the digital filters, the 32-bit sub-carrier synthesizer, and the microprocessor interface was designed using the in-house schematic capture system (Basecamp) to achieve better timing and to optimize gate count. All analog circuits were also captured by the in-house schematic capture tool. EDIF output files were generated for the Synopsys synthesized circuits and were “edifread” into the in-house schematic capture data-

base. Then, the Verilog netlist were generated for the digital portion of the entire chip. Verilog simulations were performed again to compare the netlist results with the behavioral code results. For the layout, the Cadence Layout Tool was used. A custom floor plan was first made to divide the chip into several major functional blocks, then the Cadence Cell-Ensemble Tool was

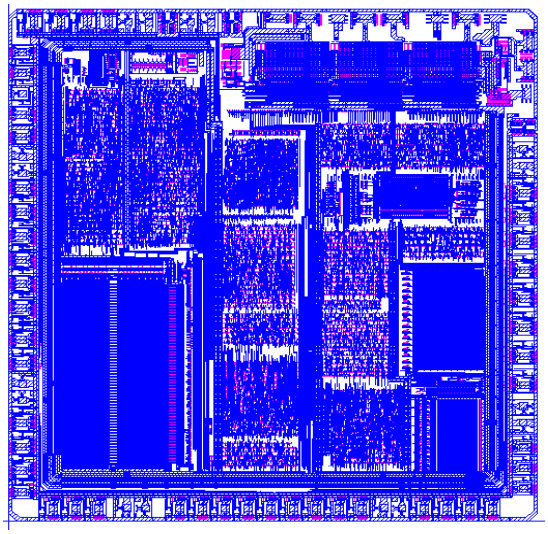


Figure (7) Photo Of The Die

used to auto-route these major functional blocks, all RAMs, ROMs and DACs were laid out manually. Fiinally, parasitic information was back-annotated into the verilog netlist files for post layout simulation. The layout of the this chip is given in Figure (7). The die size is 7150 mm x 7650 mm.

Test Results

9 sets of test vectors were generated by Verilog simulation. After fabrication, the packaged component passed all 9 sets of test vectors. Extensive functional tests were performed after putting the chip on a demonstration circuit board. The Tektronix TSG 1001 and TSG 130 were used as signal sources for various kinds of input patterns such as color bar, line 17, and ramp. Video performance measurement was done using the Tektronix VM700A. Figures (8) and (9) show the Vectorscopte Display results of color burst from the VM700A video measurement set for NTSC and PAL respectively. At 27 Mhz clock input, power consumption of the chip is 1.0 Watt.

Conclusion

A Multi-standard Video Compact Disk Encoder was designed. This chip utilized 0.8-micron, double matal CMOS process. The chip has a built-in On Screen Display which can display 10 rows by 25 columns of characters at the video outputs. A vertical filter is implemented on the chip which smooths the single field MPEG1 video to enhance the picture quality. In terms of programmability, filter selection, coring function, peaking function, four OSD colors, etc. are user-selectable. The chip has a die size of 7150 mm x 7650 mm. It consumes 1 watt of power at a 27 Mhz clock input. After fabrication, the chip is functioning on a demontration circuit board.

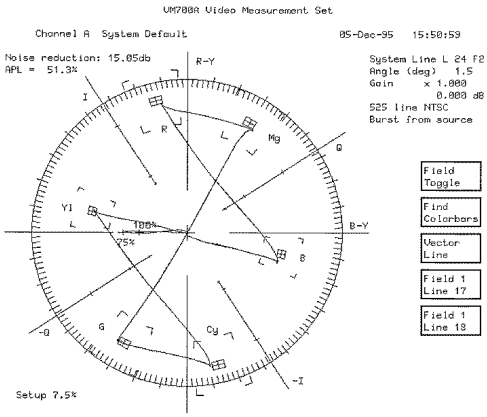


Figure (8) Vectorscope Display Of Color Burst - NTSC

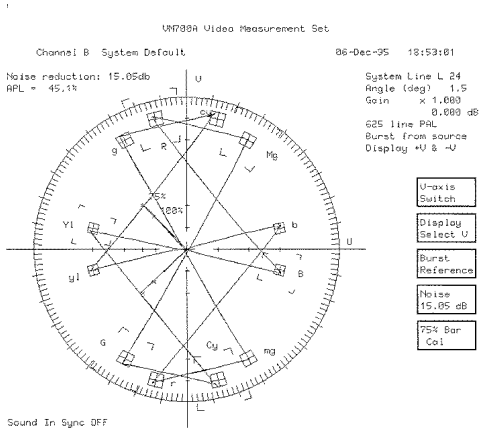


Figure (9) Vectorscope Display Of Color Burst - PAL

Acknowledgements

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References

[1] CCIR Recommendation 656-2 " Interfaces for Digital Component Video Signals in 525-line and 625-line Televison Systems (1994)

[2] CCIR Recommendation 601-1, "Encoding parameters of digital televison for studios, (1994)

[3]

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