PSP-SOI: A Surface Potential Based Compact Model of Partially Depleted SOI MOSFETs

(Invited Paper)

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***Abstract*— This paper reports recent progress on partially depleted (PD) SOI modeling using a surface potential based approach. The new model, called PSP-SOI, is formulated within the framework of the latest industry standard bulk MOSFET model PSP. In addition to its physics-based formulation and scalability inherited from PSP, PSP-SOI captures SOI specific effects by including a floating body simulation capability, a parasitic bipolar model, and self-heating. A nonlinear body resistance is included for modeling body-contacted SOI devices. The PSP-SOI model has been extensively tested on several PD/SOI technologies.**

I. Introduction

In recent years partially depleted SOI technology has become the mainstream technology for low-power, high performance CMOS ULSI applications [1], [2]. Successful use of SOI technologies requires a physics-based SOI MOSFET compact model to serve as the bridge between the manufacturing process and circuit design. Such a model must faithfully reproduce the device characteristics responsible for the advantages provided by SOI technology, such as reduced junction capacitance, elimination of the body effect in stacked devices (e.g., nMOS transistors in NAND gates), dynamic threshold voltage shifts associated with the floating body effect (FBE), and the corresponding increase of the $I_{\rm on}/I_{\rm off}$ ratio which is beneficial for low-power CMOS applications.

These are traditional requirements imposed on SOI compact models. In addition, scaling of the oxide thickness to 2nm and below introduces tunneling current components that contribute to device performance degradation [3]. The importance of tunneling currents is common to both bulk and SOI CMOS. However, the presence of a floating body in SOI device requires modeling of electron tunneling from the valence band (EVB), which is usually not critical for bulk MOSFET models.

For both bulk and SOI CMOS technologies, the reduction of the power supply voltage to about 1V means that the moderate inversion region becomes fractionally larger part of the overall voltage swing and needs to be modeled accurately using either inversion charge based [4], [5] or surface potential based [6]–[9] compact models. The latter are also capable of a physics-based description of accumulation region behavior and overlap capacitances, which is important for accurate modeling of the performance of advanced CMOS circuit. Consequently, one of the advanced surface potential based models (PSP) has been adopted as the new industry standard [15] for bulk MOSFETs. Both threshold voltage based [10] and surface potential based SOI models have been published [11]–[13]. Reflecting the state-of-the-art of bulk CMOS modeling in the previous decade, as summarized in [14]. The PSP-SOI model brings into SOI realm the advantages of the recently completed work on the development [15] and verification [16] of the surface potential based bulk MOSFET models.

In this work we present a partially-depleted SOI MOSFET model based on PSP. With the previously published SP-SOI model [12] it shares the non-iterative algorithm for the surface potential calculation that is used in PSP and is valid for high forward bias of the source and drain junctions that can be encountered in floating body SOI devices. PSP-SOI also shares PSP's physics-based formulation and description of small geometry effects, that came from merging the best features of the SP [6] and MM11 [17] models. In particular, this assures complete Gummel symmetry, including the requirements imposed on compact models in the presence of tunneling and impact ionization currents [18]. This includes the EVB tunneling symmetry recently verified using a simple engineering model [19].

The PSP-SOI model differs from SP-SOI [12] in several critical aspects. In particular, while the mobility description remains the same, the velocity saturation model is changed to that of PSP and allows modeling of higher order derivatives at $V_{\rm DS}=0$ [16]. The EVB tunneling model of PSP-SOI is a further advance, and also simplification, of [19] to provide a better fitting of experimental data. PSP-SOI contains a detailed surface potential based non-linear body resistance model that is presented here for the first time. The new PSP-SOI model has been verified in detail using data from 90nm and 65nm processes from two manufacturers, and implemented using a Verilog-A based approach [20]. Simulation results presented

to illustrate specific features of the model are based on typical parameter sets representing the 90nm and 65nm processes.

This work proceeds as follow. A model description is given in section II, self-heating effect is analyzed in section III and this is followed by a presentation of the new body contact model in section IV. Conclusions are presented in V.

II. Modeling the Floating Body Effect

Fig. 1 shows the equivalent circuit diagram of PSP-SOI. For the floating body configuration there are four external nodes: source (S), drain (D), gate (G) and substrate/back-gate (E). For DC simulations, the body potential $V_{\rm BS}$ is determined by the balance of currents from source and drain junction generation/recombination, impact ionization current and gate-to-body tunneling current (which flows between the gate and the body). For transient and AC simulations, $V_{\rm BS}$ is determined in addition by the capacitive coupling of the body to the drain, source and gate terminals. For the body contact configuration, an external node (BC) connects to the internal node (B) through a resistive path (body resistance $R_{\rm B}$). The balance of currents from this external node, from capacitance coupling, and from above-mentioned DC paths determines the body potential if there is a body contact.

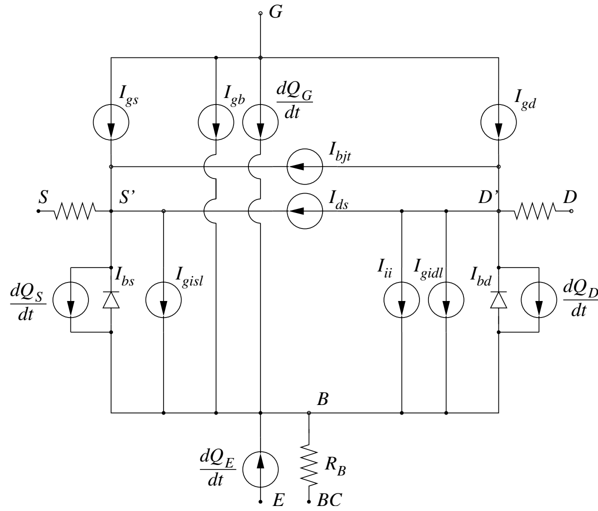


Fig. 1. Circuit representation of PSP-SOI. $I_{\rm ds}$ – intrinsic drain current, $I_{\rm bjt}$ – parasitic bipolar current, $I_{\rm ii}$ – impact ionization current, $I_{\rm gidl}/I_{\rm gisl}$ – gate induced drain (source) leakage. $I_{\rm bs}/I_{\rm bd}$ is source/drain junction current. $I_{\rm gs}/I_{\rm gd}$,$I_{\rm gb}$ is gate to source/drain/body tunneling current. Q_S, Q_D, Q_G, Q_E are source, drain, gate and back-gate charges. For body-contacted SOI, an extra node (BC) is provided to control the internal body node (B) voltage through a body resistance $R_{\rm B}$.

A. Junction Modeling

In PD/SOI technologies, the junction diode characteristics are highly non-ideal, from both the channel engineering (halo doping) and the source engineering (e.g., Ge implantation). Therefore, a physical and accurate junction model is crucial in modeling the floating body effects in SOI, such as the “kink” effect and history dependence of propagation delay [21]. PSP-SOI model uses the most advanced junction model, JUNCAP2 [22], which includes Shockley-Read-Hall recombination/generation, trap-assisted-tunneling, and band-to-band tunneling currents. The temperature dependence of junction leakage is also accurately modeled. For example, when the device local temperature is increased by self-heating, the junction current increases and the body potential decreases, resulting in a less pronounced “kink” effect in floating body SOI output characteristics.

B. Impact Ionization Current

The impact ionization current induced at the drain side flows into the body region and raises the body potential. This gives rise to the “kink’ effect observed in device output characteristics.

PSP-SOI uses the same impact ionization model as PSP. It includes accurate descriptions of the subthreshold region and of the effect of body bias. The temperature dependence of impact ionization rate is also included. As Fig. 2 shows, the model fits the substrate current in short-channel SOI devices at low drain bias.

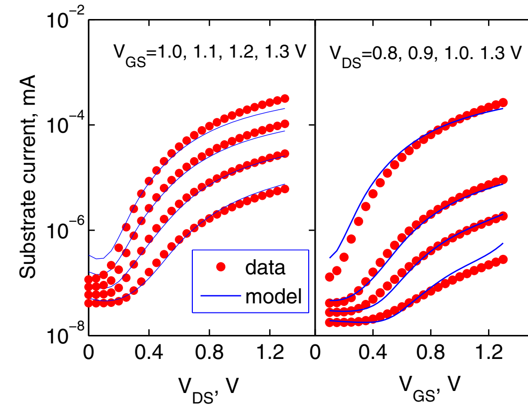


Fig. 2. Simulated and measured substrate current for body-contacted SOI at 25°C. W/L=3μm/0.065μm

C. Gate-to-Body Tunneling Current

As the gate oxide thickness $t_{\rm ox}$ scales to 1.0 nm, the oxide tunneling current increases dramatically. Gate-to-body tunneling includes several components: ECB (electron tunneling from conduction band), HVB (hole tunneling from valence band) and EVB (electron tunneling from valence band) [3]. In bulk MOSFETs EVB tunneling generates the substrate current, which is much less than the gate-to-channel tunneling current (ECB or HVB) and therefore can be neglected. However, in SOI MOSFETs the EVB tunneling current charges and discharges the body, and consequently affects the threshold voltage V_T by altering the body potential. The impact of gate-to-body tunneling current on PD/SOI CMOS circuits is explicitly studied in [23], [24].

In PSP-SOI, the EVB model is developed from a surface potential based approach. In the Tsu-Esaki formulation [25],

the tunneling current density takes the form

$$J_{\text{EVB}} = \frac{4\pi q m^*}{h^3} \int_0^{qV_{ox}-E_{\text{g}}} D(E_x)(qV_{ox}-E_{\text{g}}-E_x)dE_x, \quad (1)$$

where q is the magnitude of electron charge, m^* is the effective electron mass in the valence band of the body, E_g is the energy gap, and V_{ox} is the voltage across the oxide. $D(E_{\text{x}})$ is the tunneling transmission coefficient which comes from WKB approximation

$$D(E_x) = \exp\left(-2\int_0^{t_{\text{ox}}} \sqrt{\frac{2m^*_{\text{ox}}}{\hbar^2}\left[E_C(x)+E_x\right]}\, dx\right), \quad (2)$$

where $E_C(x)$ is the conduction band energy in the oxide and m^*_{ox} is the effective mass of electrons in SiO_2. Assuming that the EVB tunneling current is mainly from electrons having energy $E_x = 0$ in the valence band (mono-energetic approximation) gives [19]

$$J_{\text{EVB}}(y) = J_0 D(y) F_s(y), \quad (3)$$

where

$$J_0 = q^3 m^*/(2\pi\hbar^3), \quad (4)$$

$$F_s(y) = (V_{ox} - E_g/q)^2\, \Theta\left(V_{ox} - E_g/q\right), \quad (5)$$

is the "effective" supply function. The Heaviside step function Θ makes $J_{\text{EVB}}(y) = 0$ for $V_{ox} - E_g/q < 0$, and

$$D(y) = \exp\left[B_0 \cdot \left(-\frac{3}{2} + G_1 z_g + G_2 z_g^2\right)\right], \quad (6)$$

is the transmission coefficient, where

$$B_0 = \frac{4t_{\text{ox}}\sqrt{2m^*_{\text{ox}}(\chi_{\text{B}}+E_{\text{g}})}}{3\hbar} \quad (7)$$

and $z_g = qV_{ox}/(E_{\text{g}}+\chi_{\text{B}})$, V_{ox} is the oxide voltage , χ_{B} is the conduction band offset at the Si/SiO_2 interface. J_0, G_1 and G_2 are introduced as adjustable model parameters to compensate for the inaccuracy of our approximations.

To avoid using the Heaviside step function, (5) is smoothed as follows

$$F_s(y) = \left\{n_{\text{EVB}}\phi_{\text{T}} \ln\left[1+\exp\left(\frac{V_{ox}-\xi E_g/q}{n_{\text{EVB}}\phi_{\text{T}}}\right)\right]\right\}^2. \quad (8)$$

Here n_{EVB} (=1 by default) and ξ (=1 by default) are introduced as tuning model parameters for flexibility and ϕ_{T} is the thermal potential. The total EVB tunneling current is obtained by integrating along the channel

$$I_{\text{EVB}} = W\int_0^L J_{\text{EVB}}(y)\, dy. \quad (9)$$

Using the symmetric linearization method [15] gives

$$I_{\text{EVB}} = \frac{WL}{H\Delta\psi}\int_{-\frac{\Delta\psi}{2}}^{\frac{\Delta\psi}{2}} J_{\text{EVB}}(u)(H-u)\, du. \quad (10)$$

where $\Delta\psi = \psi_{sd} - \psi_{ss}$ and $u = \psi_s - \psi_m$, and ψ_{sd} and ψ_{ss} are the surface potentials (ψ_s) at the drain and source ends. $H = q_{im}/\alpha_m + \phi_{\text{T}}$, q_{im} is the inversion charge at the surface potential midpoint $\psi_m = (\psi_{sd} + \psi_{ss})/2$ and α_m is linearization coefficient. A complete expression for H, including velocity saturation and small geometry effects, can be found in [15].

To obtain an analytical expression of I_{EVB}, the surface potential dependence of transmission coefficient is approximated as [26]

$$D(u) = D_m \exp\left(-\frac{u}{u_{\text{D}}}\right), \quad (11)$$

where

$$u_{\text{D}} = \frac{\chi_{\text{B}} + E_g}{q(G_1 + 2G_2 z_{gm})}, \quad (12)$$

$z_{gm} = qV_{oxm}/(\chi_{\text{B}} + E_g)$ and $V_{oxm} = V_{\text{GB}} - V_{\text{FB}} - \psi_m$ is the oxide voltage at the surface potential midpoint. Here V_{GB} is the gate-to-body voltage and V_{FB} is the flat-band voltage.

The "effective" supply function is approximated by

$$F_s(u) = F_{sm}\exp(-\frac{2u}{u_{\text{F}}}), \quad (13)$$

where

$$F_{sm} = F_{ss}\exp\left(-\frac{\Delta\psi}{u_{\text{F}}}\right), \quad (14)$$

$$F_{ss} = \left[n_{\text{EVB}}\phi_{\text{T}} \ln\left(1+\Delta_{\text{si}}\right)\right]^2, \quad (15)$$

$$\Delta_{\text{si}} = \exp\left(\frac{V_{oxs} - \xi E_g/q}{n_{\text{EVB}}\phi_{\text{T}}}\right), \quad (16)$$

$$u_{\text{F}} = n_{\text{EVB}}\phi_{\text{T}} \ln\left(e + \Delta_{\text{si}}\right) \quad (17)$$

and $V_{oxs} = V_{\text{GB}} - V_{\text{FB}} - \psi_{ss}$ is the oxide voltage at the source end.

The total EVB tunneling current is approximated by

$$I_{\text{EVB}} = \frac{WLJ_0}{H\Delta\psi} D_m F_{sm}\int_{-\frac{\Delta\psi}{2}}^{\frac{\Delta\psi}{2}} \exp\left(\frac{-u}{u_0}\right)(H-u)\, du, \quad (18)$$

where

$$\frac{1}{u_0} = \frac{1}{u_{\text{D}}} + \frac{2}{u_{\text{F}}}. \quad (19)$$

Integrating (18) gives the total EVB tunneling current

$$I_{\text{EVB}} = WLJ_0 D_m F_{sm} h_0, \quad (20)$$

where

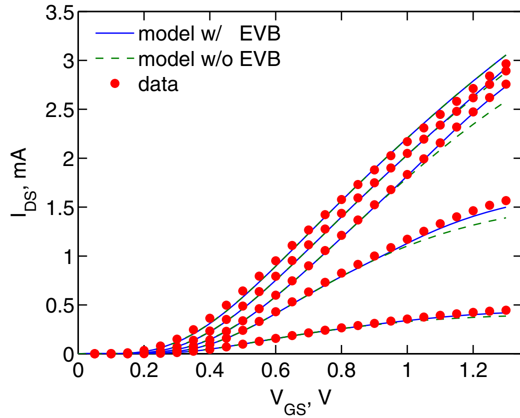
$$h_0 = (1-b)\frac{\sinh(x)}{x} + b\cosh(x), \quad (21)$$

$$x = \frac{\Delta\psi}{2u_0}, \quad (22)$$

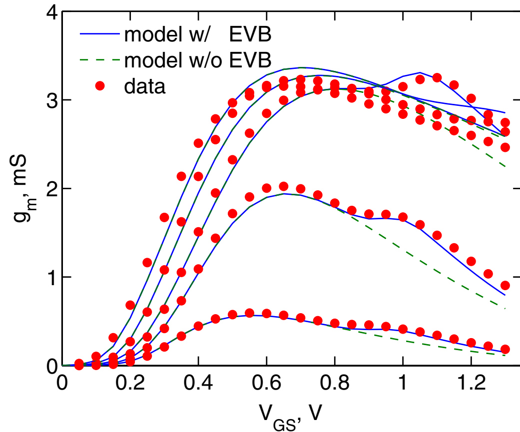
$$b = \frac{u_0}{H}. \quad (23)$$

As Fig. 3 shows, the drain current I_{DS} is increased due to higher body potential induced by the EVB tunneling. This model accurately reproduces the "kink" effect observed in the transconductance g_{m} particularly at low V_{DS}.

Fig. 4 shows a transmission-gate multiplexer implementing the Boolean function $\text{F} = \overline{\text{A}\cdot\text{S} + \text{B}\cdot\bar{\text{S}}}$. If initially the inputs "A", "B" are "High" ($V_{\text{A,B}} = V_{\text{DD}}$) and "S" is "Low", the input of the inverter is settled at "High". Under this scenario



(a) Drain current

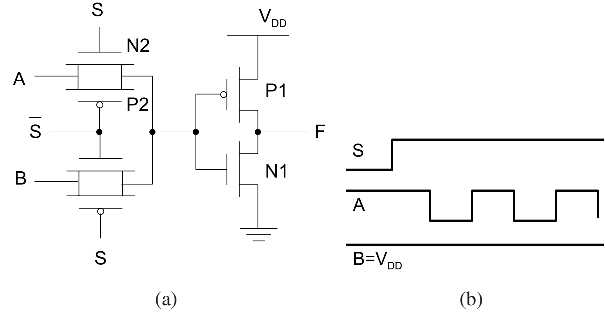


(b) Transconductance

Fig. 3. Impact of gate-to-body tunneling current (EVB) on the DC transfer characteristics of floating body SOI MOSFETs. $V_{\rm DS}$=0.05, 0.2, 0.6, 1.0 1.3V, W/L=3μm/0.13μm.

the pre-switch body potential of nMOS (N1) is determined by the EVB tunneling current and two forward biased junction currents. The body potential of pMOS (P1) is determined by the balance of back-to-back junction leakage currents. The EVB tunneling current has little impact on the body potential of P1. Consequently, the initial input-fall delay $t_{\rm pLH}$ is larger and the input-rise delay $t_{\rm pHL}$ is smaller because N1 is "stronger"(a lower $V_{\rm T}$) in the presence of EVB tunneling current. During the switching cycles, the body potentials are mainly determined by the capacitive coupling and the impact of EVB tunneling current becomes less significantly or vanishes when the circuit reaches steady state. These are illustrate in Fig. 5 and Fig. 6. Also, the nMOS (N2) of the top multiplexer becomes "slightly stronger" during input rise transitions due to the EVB tunneling current. This also makes the input rise delay faster.

As temperature increases, the junction leakage current become larger and the amount of body potential increase caused by the EVB tunneling, which is less temperature sensitive, becomes smaller. The impact of the EVB tunneling current on the circuit delay times becomes less significant. These are also illustrated in Figs. 5, Fig. 6.



(a) (b)

Fig. 4. (a) Circuit diagram of a transmission-gate multiplexer. (b) Input signal waveforms used in simulations. Signal "A" has a period of 2 ns and slew time of 20 ps.

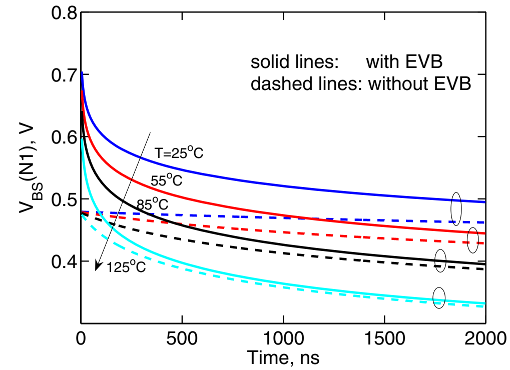


Fig. 5. Body potential of nMOS (N1) before the input falling transition.

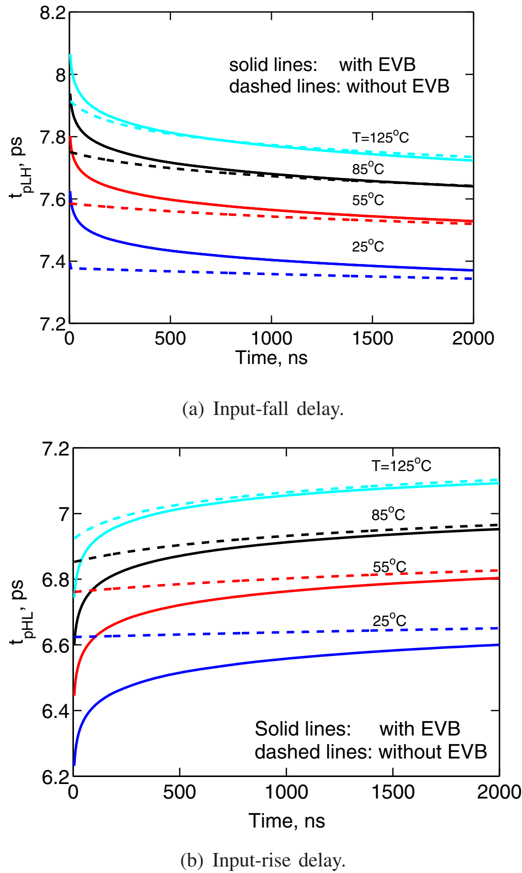
D. Parasitic bipolar current

The parasitic bipolar transistor, which is in parallel with the intrinsic MOS transistor, may be activated during transient switching if there is a large base-emitter voltage ($V_{\rm BS}$) across the source-to-body junction. This bipolar current may cause extra power consumption, degrade noise margin in static CMOS configurations, or lead to logical state errors in some dynamic circuits [27]. In PSP-SOI, this effect is modeled by adding a parasitic BJT current element

$$I_{\rm bjt} = I_{\rm bjt,sat} \cdot \left[\exp\left(\frac{V_{\rm BS}}{\phi_{\rm T}}\right) - \exp\left(\frac{V_{\rm BD}}{\phi_{\rm T}}\right) \right] \cdot \frac{1}{q_{\rm B}} \quad (24)$$

where $I_{\rm bjt,sat}$ is the saturation current, and the normalized base charge q_B includes high-level injection and Early effects.

Fig. 7 shows a Gummel plot measured on a body-contacted SOI nMOSFET, and this characteristic is used to extract the bipolar current model parameters. Fig. 8 shows a simulation of pass-gate logic with the PSP-SOI model. Initially, the control signal "C" and the input signal "IN" are "High" ($V_{\rm DD}$). With both the nMOS and pMOS turned on, the drain node and internal body potentials settle to $V_{\rm DD}$. If the source node (IN) is pulled down after switching the control signal "C" to "Low",



(a) Input-fall delay.

(b) Input-rise delay.

Fig. 6. Impact of EVB tunneling current on the delay times of a transmission-gate multiplexer with initial “High” condition. Simulations are done at several ambient temperatures. The model parameter sets used in simulations are representing typical 65nm PD/SOI technology.

a large body-to-source voltage is created . This turns on the parasitic npn BJT and causes a transient bipolar current $I_{\rm bjt}$ to flow. Once the body is discharged, this current disappears.

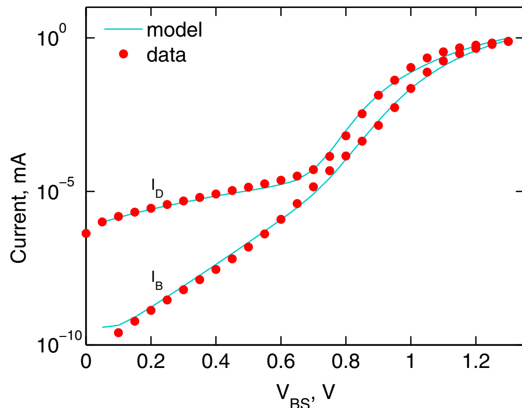
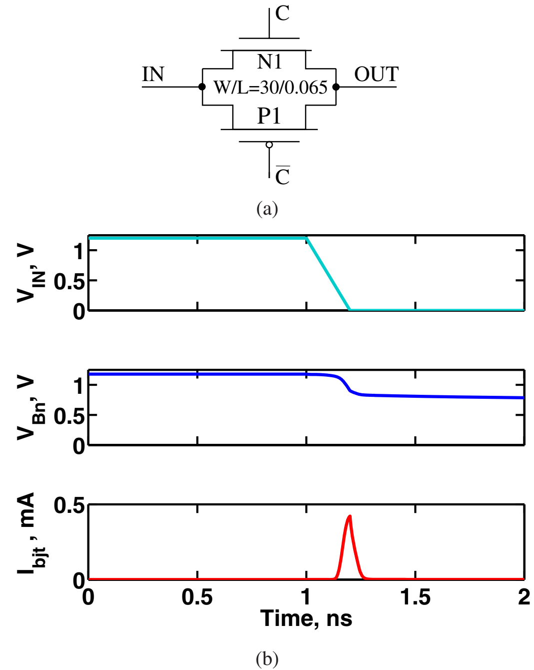


Fig. 7. Gummel plot of parasitic BJT in body-contacted SOI (nMOS). The source is grounded and drain-to-body voltage $V_{\rm DB} = 0$ while sweeping $V_{\rm BS}$.W/L=3μm/55nm



(a)

(b)

Fig. 8. (a) Circuit diagram of a basic pass-gate logic. (b) Waveforms of input signal $V_{\rm IN}$, body potential $V_{\rm Bn}$ and parasitic bipolar current $I_{\rm bjt}$ in nMOS. The model parameters are extracted from typical 65nm PD/SOI technology.

III. Self-Heating Effect

The self-heating effect (SHE) in SOI devices and circuits has been extensively studied [28], [29]. The heat generated in the channel raises the local temperature due to the low thermal conductivity (two orders of magnitude less than silicon) of silicon dioxide. In PSP-SOI, the self-heating effect is modeled by adding standard auxiliary $R_{\rm th}$-$C_{\rm th}$ subcircuit [30], [10], shown in Fig. 9, where $R_{\rm th}$ and $C_{\rm th}$ are thermal resistance and capacitance, respectively.

Fig. 10 shows the measured and simulated static output characteristics of a floating body SOI device. Simulations for high gate and drain bias without self-heating predict a larger drain current $I_{\rm DS}$ than when self-heating is included. The rise in device temperature is about 60–100K.

In most digital logic applications, self-heating is negligible since the power consumption per device under switching condition is low [31]. Further, the thermal time constant (0.1-1 μs) is larger than the switching clock rate and self-heating is therefore effective suppressed. Fig. 11 (a) shows the frequency of a 51 stage ring oscillator simulated at different ambient temperatures with self-heating effect switched on and off. The actual temperature rise, as simulation predicts (Fig. 11 (b)), is small, which suggests that it is safe to turn off the self-heating in most digital circuit simulations. However, self-heating should be taken into account in parameter extraction. The data are usually taken from static measurements where self-heating effect is significant. Recently a new methodology to derive self-heating free data (for both drain and substrate currents) has been proposed to reduce the iteration loops in

parameter extraction process [32] .

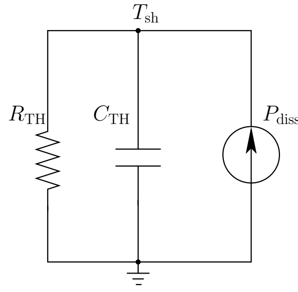


Fig. 9. Auxiliary self-heating network. $P_{\rm diss} = I_{\rm DS} \times V_{\rm DS}$. The thermal node $T_{\rm sh}$ is accessible by the user to monitor the device temperature in Spice simulations.

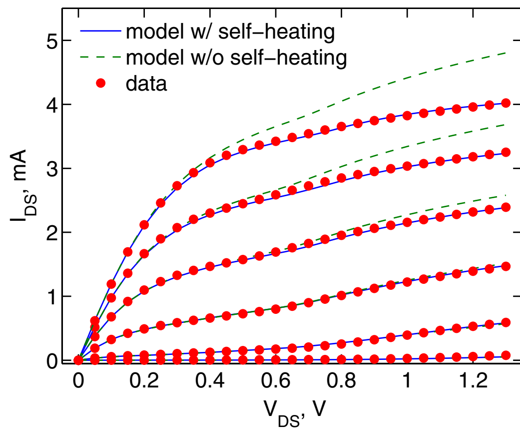


Fig. 10. Measured and modeled output characteristics of floating body SOI nMOSFET. W/L=3μm/65nm.

IV. Body Contact Model

In some critical circuits, like sense amplifiers, where slow variations of threshold voltage are unacceptable, body contacts are used to suppress the floating body effect. A common configuration is the T gate structure shown in Fig. 12.

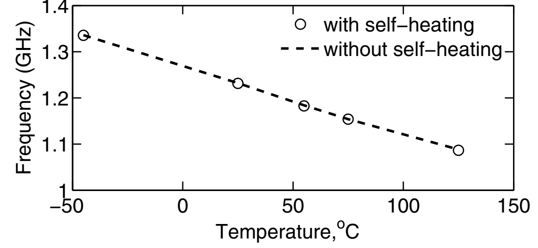
The body resistance depends strongly on the doping profile and film thickness. A simple but inaccurate linear model often used to estimate the body resistance is

$$R_{\rm B} = R_{\rm bsh}\frac{W}{L}, \quad (25)$$

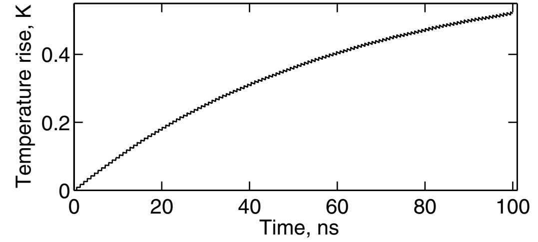
where $R_{\rm bsh}$ is the body sheet resistance and W and L are the width and length of the device. In practical applications the body resistance is highly bias-dependent. In some cases, the thin film can become fully depleted and the resistance of the body region becomes so high that the body terminal is effectively disconnected from the body of the device.

In PSP-SOI, a bias-dependent body resistance sub-model is provided to capture the variation of $R_{\rm B}$ with the terminal voltages:

$$R_{\rm B} = \frac{W^2}{\mu_{\rm B} Q_{\rm nbr}}, \quad (26)$$



(a)



(b)

Fig. 11. (a) Simulated 51 stage ring oscillator oscillation frequency at different ambient temperatures. Model parameters are extracted from 65nm PD/SOI technology data. (b) Simulated device temperature rise in nMOS at 25°C.

where $\mu_{\rm B}$ is the mobility of majority carrier in the body (holes in nMOSFETs), and

$$Q_{\rm nbr} = qN_{\rm EFF}t_{\rm SI}WL - Q_{\rm B} \quad (27)$$

is the total mobile majority charge in the neutral body region. Here $N_{\rm EFF}$ is the effective channel doping including the effect of halo implants, and $t_{\rm SI}$ is the thin film thickness. The total bulk charge $Q_{\rm B}$ includes the (front) gate induced bulk charge Q_B^f, the junction depletion charges $Q_{j,S/D}$ and the back-gate induced bulk charge.

Fig. 13 shows a typical plot of the bias dependence of body resistance. The body resistance varies significantly with the external body bias $V_{\rm BS}$ even when the device is off ($V_{\rm GS} = -0.3$V, $V_{\rm DS} = 0$V). Fig. 14 shows the measured and modeled body resistance under varying DC bias for an H-gate device. Depending on the bias conditions, $R_{\rm B}$ may vary by orders of magnitude. This shows that proper modeling of body resistance is crucial to modeling of the transient behavior of body-contacted SOI devices.

Floating body related effects are usually characterized from measurements on body-contacted devices across a wide range of bias. The bias dependence of $R_{\rm B}$ should be taken into account during the parameter extraction process. For example, at high forward bias ($V_{\rm BS} > 0.6$V), the body resistance becomes lower and enhances the current drive, this is rendered as a lower $V_{\rm T}$. Under reverse bias, the body contact becomes less influential and the body effect is reduced (lower $V_{\rm T}$). Fig. 15 compares our model with experimental data.

The effect of body resistance is distributed in nature [33]. In our simulations, the wide body-contacted SOI device is partitioned into several smaller segments (e.g., 5) along the

width direction and they are cascaded together with proper handling of narrow-width effects.

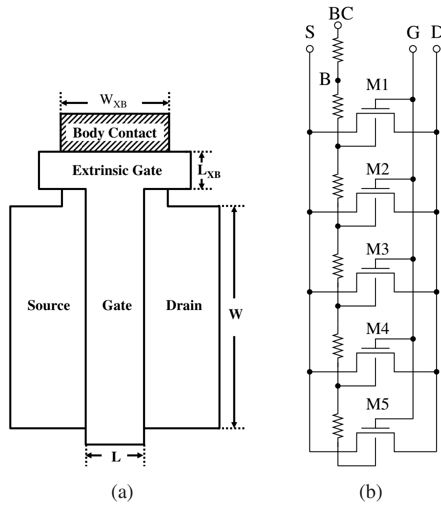


Fig. 12. (a) A typical structure of T-gate SOI device. For H-gate SOI device, another body contact is patterned at the other end of the gate. (b) Schematic representation of the T-gate SOI sub-circuit used in simulations.

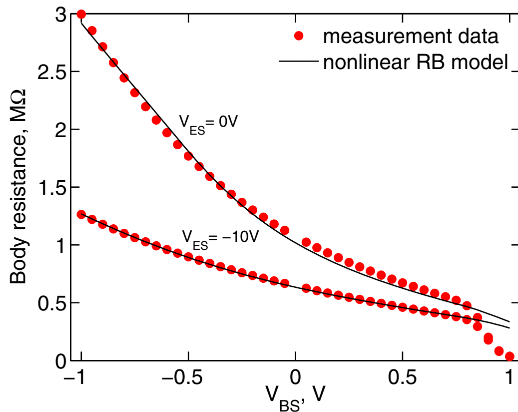


Fig. 13. Measured and modeled body resistance of body-contacted SOI device (H-gate). $V_{\mathrm{GS}} = -0.3$V, $V_{\mathrm{DS}} = 0$V, back-gate bias $V_{\mathrm{ES}} = 0, -10$V. W/L=3μm/65nm. The extracted film thickness $t_{\mathrm{SI}} = 45$nm and buried oxide thickness $t_{\mathrm{BOX}} = 282$nm. The sudden drop of R_{B} near $V_{\mathrm{BS}} = 0.8$V is caused by junction currents.

V. Conclusions

PSP-SOI was implemented in a circuit simulator and used to reproduce characteristic features of SOI CMOS devices/circuits. The new results of this work indicate that the advantages of surface potential based bulk MOSFET models can be extended to the SOI domain.

VI. Acknowledgement

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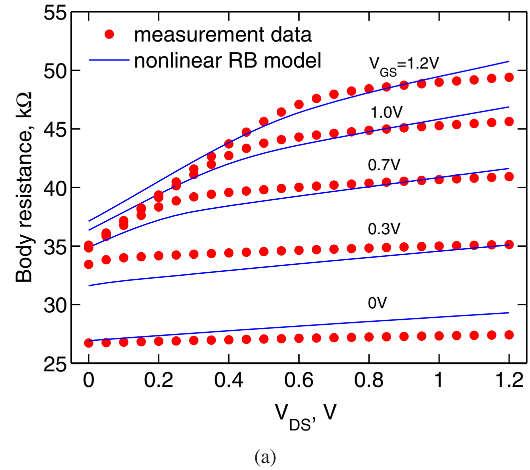
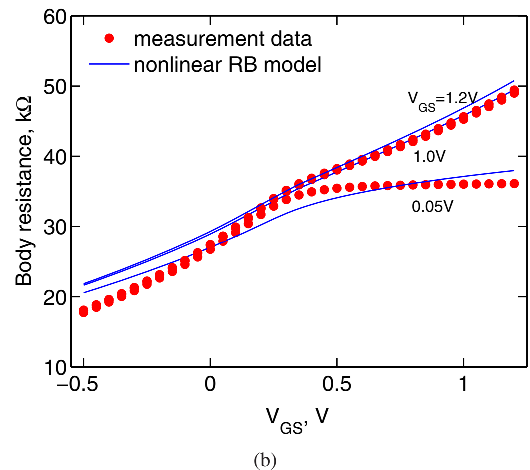


(a)



(b)

Fig. 14. Measured and modeled body resistance of an H-gate SOI structure under varying DC bias condition. W/L=4μm/2μm.

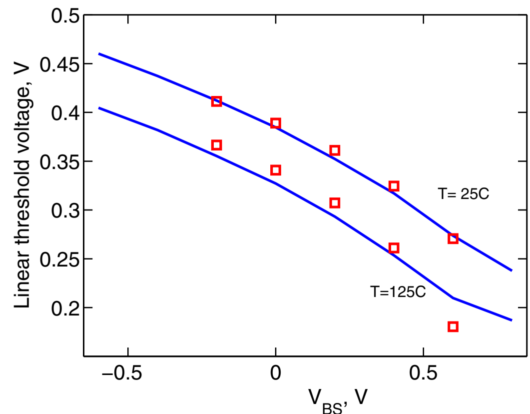


Fig. 15. The effect of body resistance on the threshold voltage. Model parameters are extracted from body-contacted SOI. W/L=3μm/65nm.

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