PSP: An Advanced Surface-Potential-Based MOSFET Model for Circuit Simulation

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Invited Paper

***Abstract*—This paper describes the latest and most advanced surface-potential-based model jointly developed by The Pennsylvania State University and Philips. Specific topics include model structure, mobility and velocity saturation description, further development and verification of symmetric linearization method, recent advances in the computational techniques for the surface potential, modeling of gate tunneling current, inclusion of the retrograde impurity profile, and noise sources. The emphasis of this paper is on incorporating the recent advances in MOS device physics and modeling within the compact modeling context.**

***Index Terms*—Compact model, MOSFET, surface potential, surface-potential-based (PSP) model.**

I. Introduction

COMPACT MOSFET models represent an essential bridge between the fabrication process development and the circuit design. Their primary function is to accurately reproduce minute details of the device characteristics, which are essential to the design of digital, analog, mixed-signal, and RF integrated circuits. This must be accomplished in a manner consistent with high computational efficiency and with a model structure that remains invariant of the fabrication process particulars and the device design. The conflicting requirements of the model accuracy, generality, and computational efficiency make the subject of compact model development particularly challenging since traditional modeling techniques relying on computationally expensive special functions of the mathematical physics cannot be employed. Hence, curve-fitting techniques and careful selection of the model parameters play essential roles in the development of compact MOSFET models. Today, a general-purpose state-of-the-art compact model consists of about 300–400 equations and 150–400 parameters containing physical information about the device (e.g., oxide thickness and doping level) and compensating for the simplified description of the physical effects inevitable in compact models of semiconductor devices (e.g., semi-empirical mobility models) [1]–[8].

Apart from the accuracy and comprehensive nature, a compact model must satisfy several rather restrictive requirements imposed by their use in advanced circuit simulators. From the mathematical point of view, the equations of the models should be of, at least, class C^1 in order to be compatible with Newton–Raphson-based circuit simulators, with class C^2 or better preferred in order to achieve faster convergence, and class C^3 required for distortion modeling in RF circuits. This also applies to the unphysical bias ranges (e.g., $V_{\rm GS} = 2000$ V and $V_{\rm DS} = -1600$ V in a 100-nm device) since such extreme voltages may appear during convergence of the circuit simulations for some "difficult" circuits. One technique to accomplish this is to insist on the "asymptotic correctness" of all model equations, by which it is understood that even semi-empirical equations employed in the model formulation should revert to physically meaningful behavior for extreme values of terminal voltages and model parameters [9].

As the device dimensions approach their fundamental limits, new physical phenomena become essential for the accurate reproduction of the device characteristics. Quantum-mechanical corrections and description of polysilicon depletion (and sometimes accumulation effects [10]) in the MOSFET's gates become indispensable in advanced device models. More recently, deviations from the "universal" dependence of the effective channel mobility on the effective vertical field [11], [12] were introduced to account for the effects of Coulomb scattering on the low gate voltage characteristics and the temperature effects in MOSFETs [7], [8], [13], [14]. The reduction of the gate oxide thickness below 2 nm necessitated the accurate modeling of the gate tunneling current including scaling effects and partition between different device terminals [7], [8], [15], [16]. Since the channel contribution to the terminal charges scales down faster than that of the overlap regions and other parasitics, accurate and physical description of the latter became an indispensable part of advanced MOSFET models. Continued scaling down

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of the junction depth brought out the necessity to accurately model trap-assisted tunneling and other second-order effects [17]–[19]. Another phenomenon that has only recently found its way in the compact model formulation is the enhanced channel length modulation effect and corresponding degradation of the output resistance in long-channel MOS transistors fabricated with HALO doping.

Significant advances in RF CMOS applications imposed further requirements on the compact CMOS models. In addition to the traditional figures of merit such as accurate and physically meaningful description of g_m/I_D ratio (g_m denotes the device transconductance) [20], the details of the output characteristics near $V_{\rm DS} = 0$ turned out to be critical for the modeling of some circuits (e.g., passive mixers), essential in mobile communication designs [21]. Furthermore, modeling of the accumulation region becomes important for varactor-based circuits such as voltage-controlled oscillators [7], [10]. Of particular importance for RF CMOS design is the complete and accurate description of the noise sources including the channel-induced gate noise and its correlation with the channel thermal noise. Only in the last few years has this subject been brought in a definitive form, both from the point of view of model accuracy [22], [23] and implementation techniques [24]. Rapid progress has also been made in the development of nonquasi-static MOSFET models essential for some RF applications [25]–[29].

Gradual accumulation of the requirements imposed on the compact models and simultaneous realization of the limitations associated with the traditional modeling techniques [3] resulted in the intensive investigation of several alternative approaches [30]. Development and reduction to practice one of them selected as present as a new industry standard is the main purpose of the present paper. The new surface-potential-based (PSP) model is obtained by merging and developing the best features of the two advanced surface-potential-based (ψ_s-based) models, namely: 1) SP (developed at The Pennsylvania State University) [7] and 2) MM11 (developed at Philips) [5].

The rest of this paper is presented as follows: In Section II, we discuss the structure of the model followed by the discussion of the intrinsic model in Section III. Formulation of the extrinsic model is the subject of Section IV, while Section V deals with the verification of the above models against experimental data. The noise model used in PSP is discussed in Section VI followed by the conclusions presented in Section VII.

II. Model Structure

Leaving aside the lookup tables, there are essentially three approaches to the compact modeling of MOS transistors. By far, the most widely used is the threshold voltage-based ($V_{\rm th}$-based) method that has been highly developed in models like MOS Model 9 [31], BSIM3 [4], and BSIM4 [32]. The models of this type are formulated directly in terms familiar to circuit designers (e.g., threshold voltage, subthreshold slope, etc.) and have been in use since the development of MOSFET transistor in the 1960s. At present, however, there is a wide consensus that the $V_{\rm th}$-based approach is inconsistent with the development of sub-100-nm MOSFETs, reduction of the power supply voltage, and requirements of RF CMOS design, and needs to be replaced. The arguments leading to this conclusion are presented in [3], [7], [21], and [30].

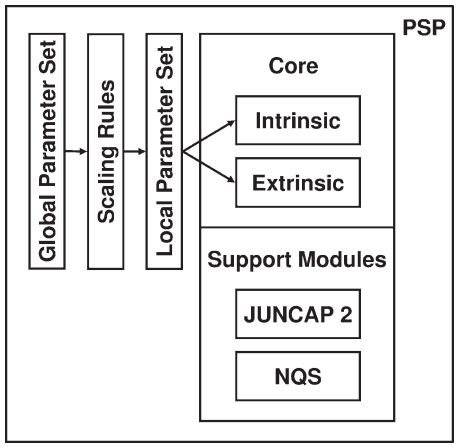


Fig. 1. Structure of the PSP model.

A powerful alternative technique is what is now called inversion-charge-based (q_i-based) approach that was originally introduced in [33] and [34] and further developed in [35] and [36]. Since the inversion charge is directly related to the intrinsic drain current, this formulation has certain elegance and, unlike $V_{\rm th}$-based models, directly and mostly physically describes device characteristics in the weak inversion (subthreshold) region. Nevertheless, the flexibility of the q_i-based formulation is limited by the fact that q_i is not available for the model formulation in the accumulation region (essential for RF applications) and in the source-drain overlap regions. Furthermore, the inversion charge density is not a natural variable for the formulation of the noise model, gate current partition in the channel region, and makes it more difficult to formulate the large-signal NQS version of the model.

This leaves the ψ_s-based formulation [5]–[8], [30], [37]–[42] as the only viable foundation for the next generation of compact MOSFET models. In fact, as shown in [7], ψ_s-based formulation includes both $V_{\rm th}$-based and q_i-based methods as special cases that follow from the general approach under additional assumptions. To serve as a gateway to advanced MOS IC design for new generations of CMOS technology, PSP contains an accurate description of the major physical effects responsible for the characteristics of scaled MOSFETs. These include Coulomb scattering and nonuniversality of the mobility model, HALO doping, vertical profile nonuniformity (e.g., retrograde channel profiles), quantum-mechanical effects, polysilicon depletion region, a nonsingular velocity saturation model, gate tunneling current and gate-induced drain and source leakage (GIDL and GISL) currents, all MOSFET noise sources, an advanced junction model, and an STI-induced stress model [32]. The PSP model formulation enables these features to be implemented without a prohibitive increase in model complexity.

The structure of the PSP model is shown in Fig. 1. The core model includes computation of the surface potentials $\psi_{\rm ss}$ and $\psi_{\rm sd}$ at the source and drain ends of the channel, respectively, the intrinsic drain current, and the terminal charges. The

extrinsic model includes computation of the overlap charges, gate tunneling current, substrate impact ionization current, and spectral densities for the electrical fluctuations ("noise"). The PSP model also contains two additional modules dealing with the NQS formulation and junctions. These are described in detail in [26], [28], [29], and [17]–[19], respectively.

Both MM11 and SP distinguish between local and global model parameters. This approach is carried over to PSP. Global parameters include geometry dependencies, and before evaluating the MOSFET output characteristics, they are converted into a small number of local parameters actually used in the core model. The use of local parameters facilitates the model parameter extraction as one can extract the local parameters for each device geometry separately and then use scaling equations to obtain the global parameters for the relevant range of geometries. To illustrate the difference between local and global parameters, consider the scaling of series resistance RS as

$$\mathrm{RS} = \mathrm{RSW1} \cdot (W_{\mathrm{EN}}/W_E) \cdot [1 + \mathrm{RSW2} \cdot (W_{\mathrm{EN}}/W_E)] \quad (1)$$

where $W_{\mathrm{EN}} = 1\ \mu$m is the normalization constant. The expression for the drain–current contains only the local parameter RS, whose dependence on the effective channel width W_E is described using the two global parameters RSW1 and RSW2. The first parameter describes an ideal scaling, and the second parameter introduces deviations from the ideal behavior. The parameter extraction procedure can be found in [41].

III. Intrinsic Model

A. Surface Potential

Surface potential is defined as the potential at the Si/SiO_2 interface and is usually evaluated in the gradual channel approximation that consists of neglecting the lateral field gradient term in the Poisson equation. The resulting one-dimensional (1-D) equation can be easily integrated in the case of a MOS capacitor, where the electron's imref is position independent. However, integration of Poisson equation in a MOS transistor cannot be performed exactly since the closed-form expression for the positional dependence of the minority carrier imref is unavailable. Following the development of the first ψ_s-based model in [37], several alternative forms have been developed for the first integral of the Poisson equation, which, in the present context, became known as the surface potential equation (SPE). All different versions of the SPE reported in the literature can be written in the form

$$(V_{\mathrm{GB}} - V_{\mathrm{FB}} - \psi_s)^2 = \gamma^2 \phi_T \{\exp(-u) + u - 1 + (n_b/p_b) \cdot k_n \cdot [\exp(u) - u - 1 - \chi(u)]\} \quad (2)$$

where ψ_s is referenced to bulk, the body factor is expressed as

$$\gamma = \sqrt{2 \cdot q \cdot \epsilon_{\mathrm{Si}} \cdot N_{\mathrm{SUB}}}/C_{\mathrm{ox}} \quad (3)$$

N_{SUB} denotes the substrate concentration, C_{ox} is the oxide capacitance per unit channel area, $\phi_T = k_B T/q$ is the thermal potential, V_{FB} is the flat-band voltage, $u = \psi_s/\phi_T$, n_b and p_b denote the bulk concentrations of electrons and holes, respectively, and $k_n = \exp(-V_n/\phi_T)$, where V_n is the so-called channel voltage formally defined as the imref splitting normalized to q.

In the original formulation [37], we have

$$\chi(u) = u\left(k_n^{-1} - 1\right). \quad (4)$$

The surface potentials at the source side and at the drain side are then given implicitly by setting V_n equal to V_{SB} and V_{DB}, respectively. The resulting SPE is still widely used today but is problematic in the narrow gate bias region close to the flat-band voltage where the right hand side of (2) becomes negative. This subject was investigated in [43]–[45], where the problem was traced to the position dependence of the minority carrier imref not included in the original derivation of the SPE.

Consequently, in [43], an alternative form

$$\chi(u) = 0 \quad (5)$$

free of this complication has been suggested. The corresponding SPE is used in most surface-potential-based models with the exceptions of SP and PSP. Before proceeding further, it is essential to note that this modified SPE is neither more nor less physical than the original formulation and is selected for the sake of mathematical convenience. In this regard, it is useful to note that only for $V_n = 0$, i.e., for $k_n = 1$ (MOS capacitor) (2) becomes exact (with two forms of $\chi(u)$ becoming identical).

An important observation regarding the original SPE and its subsequent modifications is that these modifications do not appreciably affect the output device characteristics, transconductances, and transcapacitances. Indeed, the term $\chi(u)$ affects only the minority carrier contribution to the surface field and (except for the narrow gate bias region near the flat-band voltage) is negligible until the inversion layer begins to form. But once it happens, $\chi(u) \ll \exp(u)$ and is insignificant once again (see [44] for further details). Hence, to some extent, one can select the function $\chi(u)$ in a way most convenient for compact model development. In [7] and [44], this observation is taken advantage of to impose an additional condition $\partial\Delta\psi/\partial V_{\mathrm{GB}} = 0$ for $V_{\mathrm{GB}} = V_{\mathrm{FB}}$, where $\Delta\psi = \psi_{\mathrm{sd}} - \psi_{\mathrm{ss}}$ is the surface potential variation across the channel. This allows one to set $\Delta\psi = 0$ in the accumulation region $V_{\mathrm{GB}} \le V_{\mathrm{FB}}$.

One possible choice of $\chi(u)$ that accomplishes this [46] is adopted in PSP, i.e.,

$$\chi(u) = u^2/(u^2 + 2). \quad (6)$$

To the model user, the change from (5) to (6) is invisible, since both forms produce identical device characteristics and make the right hand side of (2) positive for all values of the gate bias. We note in passing that yet another form of $\chi(u)$ has been introduced in [44], but it is limited to the case of $V_n > -0.5$ V and is not suitable for high forward biases of source–substrate junction and, hence, is not discussed here. In contrast, SPE, with $\chi(u)$ in the form (5) or (6), does not suffer from this limitation.

The surface potentials computed numerically for two choices of $\chi(u)$ are presented in Fig. 2. The results confirm that the choice of $\chi(u)$ has negligible effect on the device characteristics and is a matter of convenience. Only the results

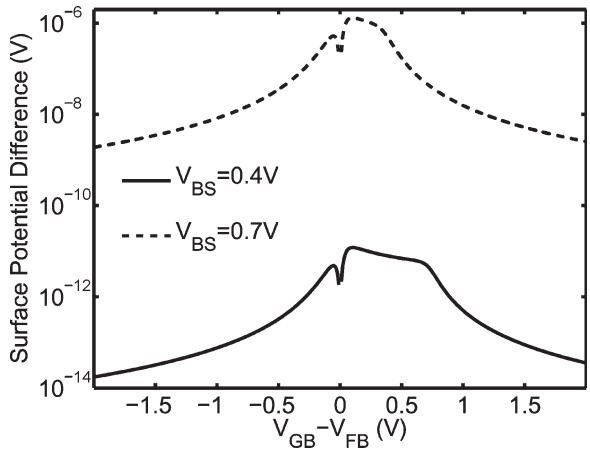


Fig. 2. Difference in surface potentials calculated numerically from (5) and (6) for $V_{\rm BS} = 0.4$ and 0.7 V. $N_{\rm SUB} = 5 \times 10^{17}$ cm^{-3}, and $t_{\rm ox} = 2$ nm.

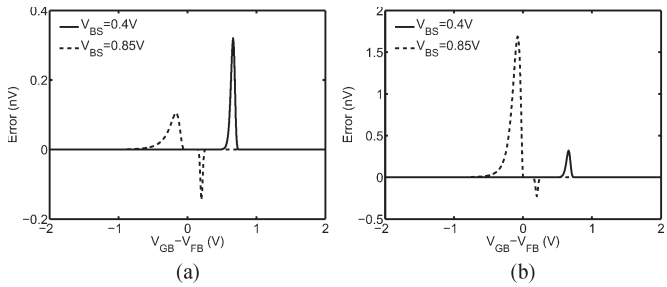


Fig. 3. Accuracy of the analytical approximation of surface potential for $\chi(u)$ given by (a) eqn. (6) and (b) eqn. (5). $N_{\rm SUB} = 5 \times 10^{17}$ cm^{-3}, and $t_{\rm ox} = 2$ nm.

for forward-biased source–substrate junctions are presented since for $V_n \leq 0$ the difference is totally negligible.

As far as the actual computation of the surface potential is concerned, PSP uses an advanced noniterative algorithm [41], [46]. This algorithm replaces that developed for the SP model [7] and has the advantage of remaining valid for high forward biases. Typical results are shown in Fig. 3(a), which indicate an accuracy of better than 1 nV for forward biases up to 0.85 V. Naturally, this accuracy figure applies to the case when both numerical ("exact") solution and analytical approximation of ψ_s use the same form of $\chi(u)$ given by (6). Adaptation of the approximation to SPE with $\chi(u)$ given by (5) yields similar results shown in Fig. 3(b).

An alternative to using analytical approximation for ψ_s is to adopt recently developed efficient numerical methods [5], [47]. Since evaluation of the surface potential takes about 5% of the model execution time, the difference between numerical and analytical evaluation of the ψ_s is usually invisible to the model user. This desirable situation is brought about by the progress in the development of both analytical and numerical techniques for solving SPE. The analytical algorithm is adopted in PSP in order to eliminate the internal iterative loop and corresponding convergence issues.

B. Retrograde Profile

There is presently considerable interest in MOSFETs with the so-called "retrograde" doping profile in the direction normal

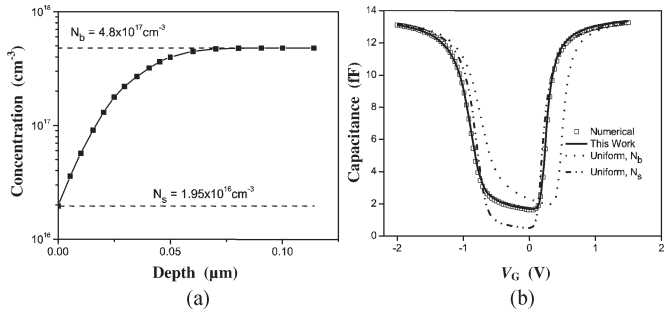


Fig. 4. (a) Retrograde doping profile and (b) $C(V)$ curves for different approximate impurity profiles. $t_{\rm ox} = 2.5$ nm.

to the Si/SiO_2 interface. From a simple point of view, this approach allows one to obtain higher effective channel mobility in the surface region where the impurity concentration is reduced while retaining good short-channel behavior. More sophisticated analysis shows that the ability to use retrograde profiles provides an opportunity to separately optimize the designs of low-power and high-performance CMOS processes [48]. Hence, there is a clear need to include nonuniform doping in the compact transistor models used in modern circuit simulators. Conceptually, the problem is well understood and can be reduced to computing the surface potential as a function of the gate bias in a vertically nonuniformly doped device. However, this approach is not suitable for circuit design applications since numerical solution of Poisson equation is prohibitively slow in circuit simulations.

A simplified method of modeling nonuniformly doped MOS devices using bias-dependent "effective" doping has been considered in [49] and in a more complete form in [50]. It still requires extensive computations that are not conducive to circuit design applications. Furthermore, in [49] and [50], the effect of doping nonuniformity is introduced primarily to model the substrate sensitivity of the threshold voltage. Consequently, it is absent from the device characteristics corresponding to $V_{\rm BS} = 0$.

In a more powerful method [51], the actual profile is approximated by a step function leading to an analytical expression for the effective impurity concentration as a function of surface potential. Further applications of this technique were reported in [9] and [52]. An important advantage of the approach taken in [51] is that unlike the analysis in [50], the problem of modeling the vertical impurity profile nonuniformity is decoupled from other short-channel effects. This method is, however, not directly applicable to ψ_s-based models. Indeed, such models are invariably based on the first integral of the Boltzmann–Poisson equation that is solved under the assumption that the impurity concentration is uniform [37]. This section contains a new version of the method developed in [51] that has the same physical content but is compatible with the ψ_s-based approach.

A typical retrograde impurity profile is shown in Fig. 4(a) [53]. The surface (N_s) and bulk (N_b) concentrations differ by an order of magnitude so that the effect of nonuniform doping on the $C(V)$ characteristics is pronounced and is readily seen in Fig. 4(b). In particular, it is shown in Fig. 4(b) that using a uniform impurity profile with either $N_{\rm SUB} = N_s$ or $N_{\rm SUB} = N_b$ results in $C(V)$ curves that differ significantly from the

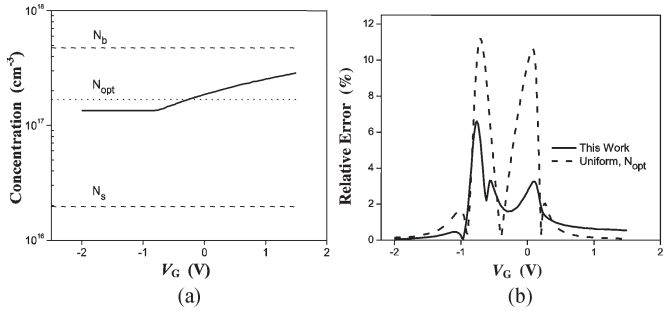


Fig. 5. Gate bias dependence of (a) the effective substrate impurity concentration and (b) the relative error of the new and traditional approaches. $t_{ox} = 2.5$ nm, $N_0 = 1.35 \times 10^{17}$ cm^{-3}, $D_N = 0.5$, $V_N = -0.75$ V, and $\varepsilon = 0.001$.

$C(V)$ curve obtained by numerical solution of Poisson equation with the nonuniform impurity distribution shown in Fig. 4(a). A better result is achieved by still considering a MOS capacitor with uniform doping density but using least square fit to select the optimal value of $N_{\rm SUB}$ denoted as $N_{\rm opt}$. Nevertheless, even in this case, the difference between the actual $C(V)$ curve and that of the uniformly doped capacitor is greater than what is acceptable in modern compact models [cf. Fig. 5(b)]. Hence, it follows the need to incorporate nonuniform doping in the compact model of MOS devices.

The essential physics of the problem is the increase of the width of the surface space-charge region with the gate bias V_G. For the retrograde impurity profile, this implies the increase of the doping concentration at the edge of the space-charge region. Hence, it is plausible that the effect of nonuniformity can be modeled by introducing the fictitious gate bias dependence of the substrate doping. In other words, instead of the actual device with position-dependent doping, we substitute the uniformly doped capacitor, but with the doping level $N_{\rm SUB} = N(V_G)$, which is an increasing function of the gate bias. For such a capacitor, the surface potential is determined from the first integral of the Boltzmann–Poisson equation in the form (2), but with $\gamma = \gamma(V_G)$ obtained by substituting $N(V_G)$ in the standard expression (3).

While computing the surface potential corresponding to a given bias V_G, inclusion of the $\gamma(V_G)$ dependence is inconsequential: $N_{\rm SUB}(V_G)$ and $\gamma(V_G)$ are fixed. This means that the proposed inclusion of doping nonuniformity carries no overhead in terms of the computational complexity and is well suited for compact modeling applications. This analysis also makes it clear why the physical $N_{\rm SUB}(\psi_s)$ dependence [51] is difficult to use directly in ψ_s-based models. Indeed, while the underlying physics is well reproduced by either $N_{\rm SUB}(\psi_s)$ or $N_{\rm SUB}(V_G)$ description, only the latter allows one to retain the well-developed solution methods for the surface potential (2) such as the analytical approximation in [41].

It remains to demonstrate the accuracy of the proposed approach. A particular form of the bias dependence of the effective doping used in this study is given by

$$N_{\rm SUB} = N_0 \left[1 + D_N f_\varepsilon (V_G - V_N)\right] \tag{7}$$

where $f_\varepsilon(v) = (v + \sqrt{v^2 + \varepsilon})/2$.

Equation (7) describes the gradual increase of the effective doping with the applied voltage motivated by physical consideration. Constants N_0, D_N, V_N, and ε are model parameters and, in this paper, are selected by the least square fit to the numerically evaluated capacitance–voltage characteristic. The resulting $N_{\rm SUB}(V_G)$ dependence is shown in Fig. 5(a). As shown in Figs. 4(b) and 5(b), it provides an accurate reproduction of the MOS $C(V)$ curve. This justifies the use of a particular form of the $N_{\rm SUB}(V_G)$ dependence given by (7). In practical applications, four model parameters are extracted from experimental data and do not change during circuit simulations. More complex forms of the $N_{\rm SUB}(V_G)$ dependence may be introduced as well, including the upper limit of the effective doping. We also note that correct reproduction of the MOS $C(V)$ curve using bias-dependent doping automatically guarantees that both the surface potential and the gate charge are identical in the actual nonuniformly doped device and the device with uniform but bias-dependent doping.

C. Mobility

The effective channel mobility in the PSP model is given by

$$\mu_{\rm eff} = \frac{U0 \cdot \mu_x}{1 + (\mathrm{MUE} \cdot E_{\rm eff})^{\rm THEMU} + \mathrm{CS} \cdot q_{\rm bm}^2 / \left(q_{\rm bm} + q_{\rm im}\right)^2 + G_{\rm R}} \tag{8}$$

where $U0$ is the low-field mobility, and the parameters MUE and THEMU account for the mobility degradation caused by the surface roughness and phonon scattering of the effective vertical field $E_{\rm eff} = (q_{\rm bm} + \eta \cdot q_{\rm im})/\epsilon_{\rm Si}$ with $\eta = 1/2$ for electrons [11] and $\eta = 1/3$ for holes [12]. Coulomb scattering is introduced as in [13] using the parameter CS, and $q_{\rm bm}$ is the bulk charge per unit channel area at the surface potential midpoint. The latter is defined [54] as the channel point corresponding to $\psi_s = \psi_m$, where $\psi_m = (1/2)(\psi_{\rm ss} + \psi_{\rm sd})$. The factor μ_x describes nonuniversality effects and also accounts (empirically) for nonuniform doping. The term $G_R = U0 \cdot (W/L) \cdot q_{\rm im} \cdot \mathrm{RS}$ accounts for the series resistance. When the series resistance is included externally, G_R is set to zero.

The parameters MUE and THEMU are used to control the shape of the linear $g_m(V_{\rm GS})$ dependence. The introduction of the Coulomb scattering term allows one to account for the deviation of the effective channel mobility from the universal mobility dependence introduced for electrons in [11] and for holes in [12]. Typical results are presented in Fig. 6(a). As shown in [14] using quantitative analysis, the inclusion of the Coulomb scattering term may significantly increase the accuracy of the mobility model. From the model user point of view, the Coulomb scattering term leads to further refinement of the shape of the $g_m(V_{\rm GS})$ curve including a small shift of the transconductance peak [cf. Fig. 6(b)]. If necessary, further deviations from the universality can be included through μ_x [41].

D. Velocity Saturation

With an increase in the lateral electric field, carriers gain sufficient energy to be scattered by optical and short-wavelength

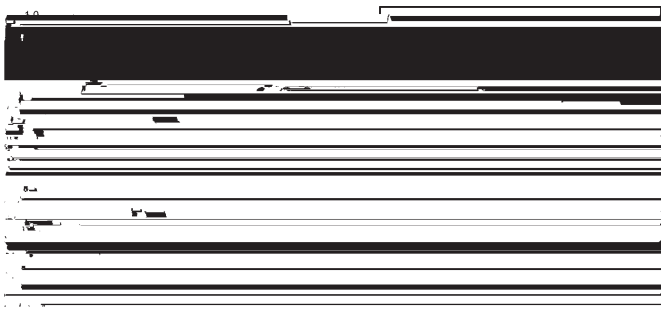


Fig. 6. (a) Nonuniversality of the effective mobility produced by Coulomb scattering and (b) its effects on the MOSFET transconductance. $t_{\rm ox} = 2.5$ nm.

acoustical phonons, resulting in a decrease of mobility and eventually resulting in the saturation of drift velocity. Velocity saturation is critical not only for the accurate modeling of the saturation region but also to ensure nonsingular behavior of the model at zero drain bias essential for simulation of intermodulation effects in RF circuits [21], [55]. The drift velocity model used in PSP is that of MM11 [5], which is based on the Scharfetter–Gummel expression [56]. For n-channel devices, we have

$$v_d = \mu\, E_y \tag{9}$$

where

$$\mu = \mu_{\rm eff}\left[1 + \left(\mu_{\rm eff}\cdot E_y/v_{\rm sat}\right)^2\right]^{-1/2} \tag{10}$$

E_y is the lateral component of the electric field, and $v_{\rm sat}$ denotes the saturation velocity.

For p-channel devices, velocity saturation is more accurately described by [56]

$$\mu = \mu_{\rm eff}\left[1 + \frac{\left(\mu_{\rm eff}\cdot E_y/v_c\right)^2}{G + \mu_{\rm eff}\cdot E_y/v_c}\right]^{-1/2} \tag{11}$$

where v_c is a parameter corresponding to the velocity of the longitudinal acoustic phonons, and G is a fitting parameter. In this case, the integration along the channel is less straightforward. For simplicity's sake, we approximate the term $G + \mu_{\rm eff}\cdot E_y/v_c$ by $G + \mu_{\rm eff}\cdot\Delta\psi/(v_c\cdot L)$. The parameter G has been found to be of minor influence and is set equal to 1. Thus, for holes

$$\mu = \mu_{\rm eff}\left[1 + \frac{\left(\mu_{\rm eff}\cdot E_y/v_c\right)^2}{1 + \mu_{\rm eff}\Delta\psi/(Lv_c)}\right]^{-1/2}. \tag{12}$$

Comparison with (10) shows that all equations derived for n-channel transistors remain valid after changing $v_{\rm sat}$ into $v_c\sqrt{1 + \mu_{\rm eff}\Delta\psi/(Lv_c)}$.

The resulting expressions for n- and p-channel devices are nonsingular, enabling, for example, the modeling of passive RF mixers [21]. As shown in [57], they also enable accurate modeling of RF distortion in the saturation region. We note in passing that the expression $\mu = \mu_{\rm eff}(1 + |E_y|/v_{\rm sat})^{-1}$, commonly used in older compact models, results in the singularity for $V_{\rm DS} = 0$ and, consequently, in the incorrect modeling of intermodulation effects in circuits like passive mixers [21], [55].

Long-channel surface-potential-based models automatically include the pinch-off behavior in the saturation region [37], [38]. Pinch-off implies that the channel at the drain end is forced into weak inversion and that the mobile charge density at the drain approaches zero. In reality, however, the concept of pinch-off is not realistic since carriers reach velocity saturation at the drain end before the pinch-off condition is fulfilled. As a result, the drain–source saturation voltage $V_{\rm dsat}$ may differ significantly from the pinch-off voltage, and this difference needs to be taken into account in the model. This is a general problem for any compact MOSFET model based on the gradual channel approximation, since the latter does not apply near the drain end of the channel in the device operating in the saturation region.

In PSP, $V_{\rm dsat}$ is calculated from the condition $\partial I_{\rm DS}/\partial\Delta\psi = 0$. Next, the drain–source voltage $V_{\rm DS}$ is replaced by an effective drain–source voltage $V_{\rm dse}$, which changes smoothly from $V_{\rm DS}$ in the linear region (i.e., for $V_{\rm DS} \ll V_{\rm dsat}$) to $V_{\rm dsat}$ in the saturation region (i.e., for $V_{\rm DS} \geq V_{\rm dsat}$). The smooth transition is obtained by changing $V_{\rm DS}$ into [39], [55]

$$V_{\rm dse} = V_{\rm DS}\left[1 + \left(V_{\rm DS}/V_{\rm dsat}\right)^{a_x}\right]^{-1/a_x} \tag{13}$$

where a_x is a local parameter that determines the smoothness of the transition. The use of (13) also ensures preservation of the Gummel drain–source symmetry [55].

For an accurate description of the output conductance $g_{\rm DS} = \partial I_D/\partial V_{\rm DS}$, PSP also includes detailed description of the channel length modulation. This description is based on [58] and has been extended to include the impact of pocket implants similar to [59].

E. Symmetric Linearization Method (SLM)

Linearization of the bulk charge as a function of the voltage drop in the channel [1]–[4], [31], [32] or as a function of the surface potential [7], [8], [55], [60] is a common feature of compact MOSFET models enabling relatively simple expressions for the terminal charges suitable for use in circuit simulations. Traditional implementations of this technique, reviewed in [1], [2], and [42], are well known to violate the essential symmetry of the device with respect to the source–drain interchange [61]. To overcome this problem, PSP relies on SLM in a form developed in [54] that is particularly suitable for the ψ_s-based formulation of compact MOSFET model. SLM, as developed in [54] and subsequently in [26], is limited to the original charge-sheet model (CSM) formulation [38] and does not include the velocity saturation effects. The latter was included within the SLM context in [7] within the SP model context using Grotjohn–Hofflinger [62] description of the velocity saturation effect.

Other versions of the SLM were also used in [55] and [60]. More recently, formulation of SLM given in [54] and [7] was used in the analysis of ballistic MOSFET [63]. In the PSP model, the description of velocity saturation follows that of MM11 and is particularly suitable for the analysis of harmonic

distortion in RF applications (cf. Section V). Hence, it became necessary to formulate SLM in a way that is compatible with (10) and (12). This is done as follows. The fundamental approximation for the inversion charge density q_i per unit channel area remains unchanged, i.e.,

$$q_i = q_{\rm im} - \alpha s \tag{14}$$

where α is the linearization coefficient, and

$$s = \psi_s - \psi_m. \tag{15}$$

The drain–current [38], [42]

$$I_{\rm DS} = W\mu\left(q_i\frac{d\psi_s}{dy} - \phi_T\frac{dq_i}{dy}\right) \tag{16}$$

with μ given by (10) becomes

$$I_{\rm DS} = \frac{\mu_{\rm eff}W\left[q_i - \phi_T(dq_i/d\psi_s)\right]}{\sqrt{1+(E_y/E_c)^2}}\cdot\frac{d\psi_s}{dy} \tag{17}$$

where

$$E_c = v_{\rm sat}/\mu_{\rm eff}. \tag{18}$$

With reference to (15), we have

$$I_{\rm DS} = \frac{\mu_{\rm eff}Wq^\star_{\rm im}}{\sqrt{1+(E_y/E_c)^2}}\cdot\frac{d\psi_s}{dy} \tag{19}$$

where $q^\star_{\rm im} = q_{\rm im} + \alpha\phi_T$. Following the analysis in [60], [64], we have

$$I_{\rm DS}\,dy = \mu_{\rm eff}W\left[q_i - I^2_{\rm DS}/\left(2W^2v^2_{\rm sat}q_i\right)\right]d\psi_s. \tag{20}$$

After integration

$$I_{\rm DS} = \mu_{\rm eff}(W/L)\Delta\psi\left[\bar{Q} - I^2_{\rm DS}/\left(2W^2v^2_{\rm sat}\bar{\bar{Q}}\right)\right] \tag{21}$$

where

$$\bar{Q} = \frac{1}{\Delta\psi}\int\limits_{\psi_{\rm ss}}^{\psi_{\rm sd}} q_i d\psi_s \tag{22}$$

and

$$\bar{\bar{Q}} = \Delta\psi\left(\int\limits_{\psi_{\rm ss}}^{\psi_{\rm sd}}\frac{d\psi_s}{q_i}\right)^{-1}. \tag{23}$$

In SLM, according to (14) and (22), $\bar{Q} = q_{\rm im}$. Strictly speaking, $\bar{Q}$ is different from $\bar{\bar{Q}}$, but for the sake of simplicity, we follow [60] and set $\bar{\bar{Q}} = \bar{Q}$. This approximation, as well as the one involved in obtaining (20) from (19), is responsible for the empirical bias dependence of saturation velocity in PSP.

Solving (21) with respect to $I_{\rm DS}$ yields

$$I_{\rm DS} = \mu_{\rm eff}\cdot W\cdot q^\star_{\rm im}\cdot\Delta\psi/(G_{\rm vsat}L) \tag{24}$$

where

$$G_{\rm vsat} = \frac{1}{2}\left[1+\sqrt{1+2\left(\theta_{\rm sat}\Delta\psi\right)^2}\right] \tag{25}$$

and

$$\theta_{\rm sat} = \mu_{\rm eff}/(v_{\rm sat}\cdot L). \tag{26}$$

As shown in Section III-D, for a p-channel transistor, (24) and (25) remain valid but with

$$\theta_{\rm sat} = (\mu_{\rm eff}/v_cL)\left[1+\mu_{\rm eff}\Delta\psi/(Lv_c)\right]^{-1/2}. \tag{27}$$

Apart from leading to a relatively simple expression for the drain–current, SLM yields an explicit form of the $\psi_s(y)$ dependence. It is obtained from (21) and (24) in the form

$$dy/d\psi_s = (L/\Delta\psi)\left[1-(s/H)\right] \tag{28}$$

where $H = H_{\rm PSP}$

$$H_{\rm PSP} = q^\star_{\rm im}/\left(\alpha' G_{\rm vsat}\right) \tag{29}$$

and

$$\alpha' = \alpha\left[1+(1/2)\left(\theta_{\rm sat}\Delta\psi/G_{\rm vsat}\right)^2\right]. \tag{30}$$

It is remarkable that apart from the expression for H, the functional form of (28) is independent of the velocity-field relation. For example, if one neglects velocity saturation, then $H = H_0$, where [54] $H_0 = q_{\rm im}/\alpha$, while using the Grotjohn–Hofflinger formulation yields [7] $H = H_{\rm SP}$, where

$$H_{\rm SP} = H_0\left[1+(\delta_0\Delta\psi)/(E_cL)\right]^{-1} \tag{31}$$

and δ_0 is the Grotjohn–Hofflinger factor [62]. Note also that in the absence of velocity saturation (i.e., $v_{\rm sat}\to\infty$), $H_{\rm PSP} = H_{\rm SP} = H_0$.

Integration of (28) yields an explicit form of the $\psi_s(y)$ relation as

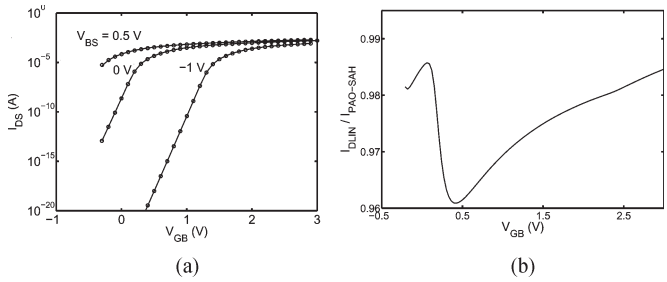
$$\psi_s(y) = \psi_m + H\left[1-\sqrt{(2\Delta\psi/HL)(y-y_m)}\right] \tag{32}$$

where the position of the ψ_s midpoint is given by

$$y_m = (L/2)(1+0.25\phi/H). \tag{33}$$

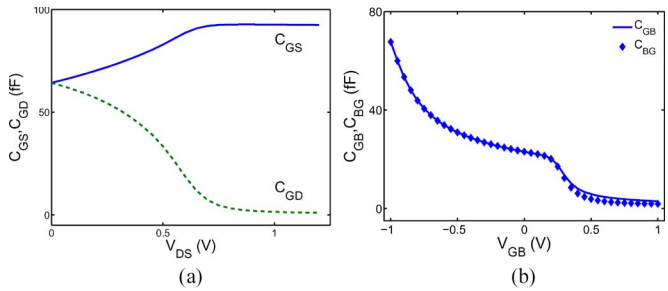
Comparison with [54] and [7] indicates that the functional form of the $\psi_s(y)$ dependence is also not sensitive to the details of the velocity field dependence, which only enters through the position-independent variable H.

Verification of SLM has been performed in [54] and [26] by comparison with the worst case of the long-channel device. In this case, the drain–current is given by the CSM [38], while the corresponding $y(\psi_s)$ dependence was obtained in [43] and [26]. An excellent agreement was found in all cases. Since CSM itself represents an approximation of the complete Pao–Sah model [37], in this paper, we extend the verification by comparing symmetrically linearized CSM directly with the Pao–Sah model. The results shown in Fig. 7(a) and (b) indicate



(a) (b)

Fig. 7. (a) Transfer characteristics for $V_{\rm DS} = 0.5$ V and different back biases. Solid lines represent the Pao–Sah model, while symbols correspond to symmetrically linearized charge sheet model. (b) Ratio of drain–currents for symmetrically linearized charge sheet model $I_{\rm DLIN}$ and Pao–Sah model $I_{\rm PAO-SAH}$. $T = 27$ °C, $W/L = 2$, $t_{\rm ox} = 2$ nm, $N_{\rm SUB} = 5 \times 10^{17}$ cm^{-3}, $\mu = 400$ cm^2/s, and $V_{\rm FB} =$ -1 V.



(a) (b)

Fig. 8. Bias dependence of (a) $C_{\rm GS}$ and $C_{\rm GD}$ and (b) $C_{\rm GB}$ and $C_{\rm BG}$.

the accuracy of symmetrically linearized CSM as a computationally efficient representation of the Pao–Sah model. The accuracy of SLM is also essential for the accurate modeling of the ratio-based circuits such as R2R circuits [65]. The latter is now considered as a new benchmark test for the advanced MOSFET models.

F. Intrinsic Charges

Quasi-static versions of the state-of-the-art compact MOSFET models, including PSP, are charge based. The source and drain terminal charges are calculated using the Ward–Dutton charge partitioning [66]. For example

$$Q_D = -W \int_0^L (y/L) \cdot q_i dy. \tag{34}$$

Using SLM, the integrals of the type encountered in (34) are easily computed by transforming them into a form

$$\int_0^L f dy = L/(H\Delta\psi) \int_{-\Delta\psi/2}^{\Delta\psi/2} (H - s) f ds \tag{35}$$

where s is defined in (15). For the drain charge, this yields

$$Q_D = \frac{q_{\rm im}}{2} + \alpha \cdot \frac{\Delta\psi}{12} \cdot \left(1 - \frac{\Delta\psi}{2 \cdot H} - \frac{\Delta\psi^2}{20 \cdot H^2}\right). \tag{36}$$

The accuracy of this result has also been verified by comparison with the drain charge expression derived using the complete charge sheet model in [43] and [26].

Comparison with the experimental data and the discussion of various benchmarks imposed on the compact models is usually performed in terms of the transcapacitances $C_{ij} = (2\delta_{ij} - 1)(\partial Q_i/\partial V_j)$, where δ_{ij} is the Kronecker delta, and the indices i, j label different terminals. The typical results shown in Fig. 8(a) illustrate the symmetry of the PSP charge model. The reciprocity $C_{\rm GB} = C_{\rm BG}$ for a special case of $V_{\rm DS} = 0$ is shown in Fig. 8(b). Note that in linear electrostatics, the reciprocity $C_{ij} = C_{ji}$ is automatic, but in MOSFET, it holds only for a special case of $V_{\rm DS} = 0$.

G. Quantum-Mechanical Correction and Polysilicon Depletion Region

The PSP model includes quantum-mechanical corrections in the form described in [64] and the effects of polysilicon depletion region as presented in [67]. A complete set of equations can be found in [41, Section 4].

IV. Extrinsic Model

The extrinsic model includes contributions of the gate/source and gate/drain overlap regions and the gate and bulk current. As is the case for the intrinsic model, the electrical behavior in the overlap regions can be most easily described in terms of the surface potential.

A. Surface Potential in the Overlap Regions

For a quantitative description of the gate/source and gate/drain overlap regions, the overlap regions are treated as n^+-gate/oxide/n^+-bulk MOS capacitances, where the source (or drain) acts as the bulk terminal. Assuming the doping profile in the n^+-source extension can be approximated by a uniform constant doping concentration $N_{\rm ov}$, we can define a body factor $\gamma_{\rm ov}$ and a flat-band voltage $V_{\rm FBov}$ in this region. A surface potential $\psi_{\rm OV}$ can be calculated (both at source and drain side) using the SPE (2), which can be further simplified by neglecting the minority carrier contribution to the space charge[1]

$$(V_{\rm GX} - V_{\rm FBov} - \psi_{\rm OV})^2 = \gamma_{\rm ov}^2 \phi_T \left[\exp(-u_{\rm ov}) + u_{\rm ov} - 1\right] \tag{37}$$

where $u_{\rm ov} = \psi_{\rm OV}/\phi_T$, and $V_{\rm GX}$ denotes either $V_{\rm GS}$ or $V_{\rm GD}$. Note that to facilitate the comparison with (2), (37) is written for the p^+ overlap region, i.e., for the case of p-channel transistors.

The analytical approximation for the noniterative solution of this equation has been initially given in [68], and the final version can be found in [10] and [41]. Typical results are shown in Fig. 9. We note in passing that while the high doping levels are more important for the modeling of the overlap regions, this analytical approximation appears (in a totally different physical context) in the problem of dynamic varactor modeling [10] and in the development of the nonquasi-static model [28]. Hence, it

[1]This approach disallows description of the inversion channel, but since the source/drain extension is highly doped, the inversion channel can only be formed at unrealistically negative gate–source or gate–drain bias.

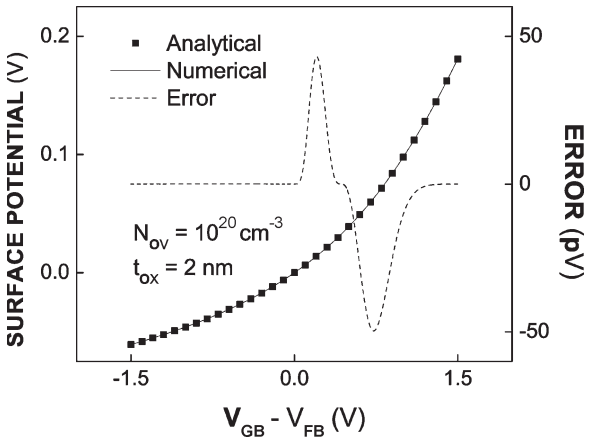


Fig. 9. Absolute error of the analytical approximation for the surface potential neglecting the minority carrier contribution in a highly doped source/drain overlap region.

is essential that the accuracy of the approximation is quite high regardless of the doping level [10].

The derivation of currents and charges in the overlap regions is most easily performed in terms of the oxide voltage in the overlap region $V_{\rm OV}$ given by

$$V_{\rm OV} = V_{\rm GX} - V_{\rm FBov} - \psi_{\rm OV}. \tag{38}$$

This variable is extensively used in the subsequent sections on bulk current, gate current, and extrinsic charges.

B. Bulk Current

Up to this point, it has been assumed that the bulk current in a MOSFET is equal to zero. Bulk current may, however, be generated between drain and bulk or between source and bulk by impact ionization and GIDL. These effects are all included in PSP and are briefly discussed in this section. The contribution of junction leakage to the bulk current is modeled by the JUNCAP2 model and is described elsewhere [17]–[19].

1) Impact Ionization: Subjected to a high lateral electric field, the electrons in the channel will accelerate traveling from source to drain and gain so much energy that they can create extra electron–hole pairs by exciting electrons from the valence band into the conduction band. This effect is generally referred to as impact ionization, and it results in a current $I_{\rm ii}$ between drain and bulk. The impact-ionization current is conventionally written as [1], [69]

$$I_{\rm ii} \propto I_{\rm DS} \cdot E_m \cdot \exp(-b/E_m) \tag{39}$$

where b is a parameter, and E_m is the maximum lateral field in the channel. In PSP, this conventional description has been extended with an accurate description of the subthreshold region and the impact of back bias [70].

2) GIDL: When the MOSFET is in the OFF state, a significant leakage current flowing from drain to bulk can be detected at a drain voltage much lower than the breakdown voltage (BV) [71]. This drain leakage current is caused by the gate-induced high electric field in the gate-to-drain overlap region, and as a result, it has been named GIDL. For a negative gate–drain bias $V_{\rm GD}$, a high transversal field is created in the depletion region formed in the gate-to-drain overlap region. Electron–hole pairs are generated by the band-to-band tunneling[2] of valence band electrons into the conduction band and collected by the drain and bulk separately. A simple expression for GIDL current based on [72] is given by

$$J_{\rm GIDL} \propto E_{\rm tov}^2 \cdot \exp\left(-B^{\star}_{\rm GIDL}/E_{\rm tov}\right) \tag{40}$$

where $B^{*}_{\rm GIDL}$ is a physical parameter, and $E_{\rm tov}$ is the maximum electric field at the Si/SiO_2 interface in the drain overlap region. The latter consists of a (dominant) transversal component (equal to $C_{\rm ox} \cdot V_{\rm OV}/\epsilon_{\rm Si}$) and a lateral component empirically proportional to $V_{\rm DB}$. The maximum electric field $E_{\rm tov}$ can be written as

$$E_{\rm tov} = (C_{\rm ox}/\epsilon_{\rm Si}) \cdot \sqrt{V_{\rm OV}^2 + (C_{\rm GIDL} \cdot V_{\rm DB})^2} = (C_{\rm ox}/\epsilon_{\rm Si}) \cdot V_{\rm tov} \tag{41}$$

where $C_{\rm GIDL}$ is an empirical parameter. Using (40) and (41), the total GIDL current becomes

$$I_{\rm GIDL} = A_{\rm GIDL} \cdot V_{\rm DB} \cdot V_{\rm tov}^2 \cdot \exp(-B_{\rm GIDL}/V_{\rm tov}) \tag{42}$$

where $A_{\rm GIDL} \propto W \cdot \Delta L_{\rm ov} \cdot C_{\rm ox}/\epsilon_{\rm Si}$, and $B_{\rm GIDL} = \epsilon_{\rm Si} \cdot B^{*}_{\rm GIDL}/C_{\rm ox}$, but they are both considered as local parameters. The $V_{\rm DB}$ term in (42) is empirical and has been added in order to ensure that $I_{\rm GIDL} = 0$ for $V_{\rm DB} = 0$ and that $I_{\rm GIDL}$ changes sign when $V_{\rm DB}$ changes sign.

In the above derivation, we have focussed on the GIDL. The same phenomenon, however, can also occur at the source side, in which case it is referred to as GISL. The electric field in the overlapped source region is typically not as high as the field in the drain region, and as a result, GISL will not really impact the source leakage. Nonetheless, GISL has been incorporated in the PSP model in order to preserve the drain–source symmetry [55], [61].

C. Gate Current

From a classical point of view, the gate current in a MOSFET is nonexistent since carriers in the inversion layer cannot cross the potential barrier χ_B of the gate oxide (see Fig. 10) (where $\chi_B = \chi_{B_N}$ for electrons and $\chi_B = \chi_{B_P}$ for holes). From a quantum-mechanical point of view, however, carriers may tunnel through the potential barrier resulting in a nonzero gate current density J_G. The probability of tunneling increases exponentially with decreasing oxide thickness $t_{\rm ox}$, resulting in an exponentially increasing J_G.

With CMOS technology scaling, $t_{\rm ox}$ is continuously scaled down, and consequently, the gate current can no longer be neglected for modern and future CMOS technologies as it may start to affect circuit performance [73], [74]. The PSP model includes the gate current model that accurately describes gate leakage in MOSFETs. This gate current model is a further development of the gate current model in SP [68], which in

[2]Trap-assisted tunneling may also occur, but at present, it is neglected in the calculation of GIDL.

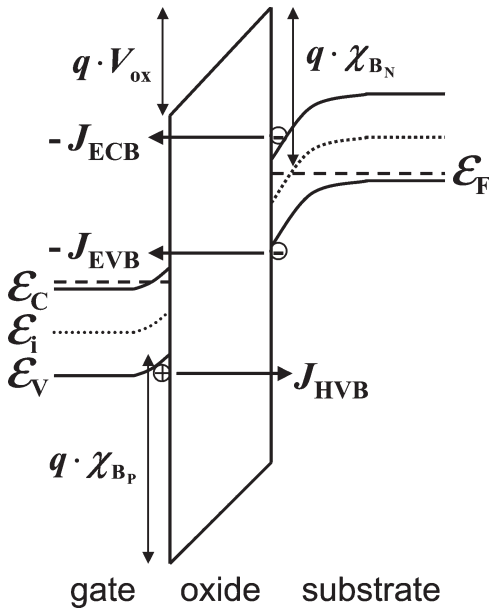


Fig. 10. Energy band diagram of an n-MOS in inversion where χ_{B_N} and χ_{B_P} are the oxide potential barriers for electrons and holes, respectively. Carriers may tunnel through the gate oxide resulting in a nonzero gate current density J_G. Three major mechanisms of gate tunneling can be distinguished: electron conduction band tunneling ($J_{\rm ECB}$), electron valence band tunneling ($J_{\rm EVB}$), and hole valence band tunneling ($J_{\rm HVB}$). ECB tunneling is important for n-MOS devices, whereas HVB tunneling is important for p-MOS devices. EVB tunneling only becomes important for high $V_{\rm ox}$ and is therefore neglected in the remainder of this section.

itself is an extension of the gate current model in MM11 [15]. In a typical MOSFET structure, we can distinguish two main gate current components, namely: 1) the gate-to-channel $I_{\rm GC}$ and 2) the gate overlap component $I_{\rm Gov}$. In the channel or overlap regions of an n-type MOSFET, mainly, conduction band tunneling (ECB) is important.[3] The direct tunneling gate current density [68]

$$J_G(y) = J_0 \cdot F_S(y) \cdot D(y) \tag{43}$$

where J_0 is a physical constant, $F_S(y)$ is the supply function [75], and $D(y)$ is the tunneling transmission coefficient. In WKB approximation, $D(y) = \exp[-B \cdot f(z_g)]$, where B is a physical constant, $z_g = V_{\rm ox}/\chi_B$, $V_{\rm ox} = q_g/C_{\rm ox}$, and

$$f(z_g) = \left[1 - (1 - z_g)^{3/2}\right] z_g^{-1} \approx -1.5 + G_2 \cdot z_g + G_3 \cdot z_g^2. \tag{44}$$

Ideally, the coefficients $G_2 = 3/8$ and $G_3 = 1/16$ can be obtained from a second-order Taylor expansion. However, here, they have been turned into adjustable parameters to absorb inaccuracies included in the derivation of (43). The supply function [75] is given by

$$F_S(y) = \ln\left\{\frac{1 + \exp\left[(\psi_s - V - \alpha_b - \psi_t)/\phi_T\right]}{1 + \exp\left[(\psi_s - V_{\rm GB} - \alpha_b - \psi_t)/\phi_T\right]}\right\} \tag{45}$$

[3]In p-type MOSFETs, on the other hand, mainly valence band tunneling is important. In the following, the same derivation can be used for p-type MOSFETs but a different value for oxide potential barrier χ_B has to be used (see Fig. 10).

where $q \cdot \alpha_b$ is the difference between the conduction band edge and the electron quasi-Fermi potential, and the variable ψ_t reflects the fact that there are few electrons having kinetic energy higher than a few $k \cdot T$. Specifically, $\psi_t = 0$ for $V_{\rm ox} \geq 0$ and $\psi_t = -V_{\rm ox} + G_0 \cdot \phi_T$ for $V_{\rm ox} < 0$, where G_0 is an adjustable parameter accounting for the possibility of a difference between the conduction band offset at the Si/SiO_2 and poly-Si/SiO_2 interfaces. In contrast to more empirical models, the use of the supply function F_S automatically ensures that the gate current is zero for zero applied bias. In the following, we briefly discuss the gate-to-channel and the gate overlap current components separately.

1) Gate-to-Channel Current: The total contribution $I_{\rm GC}$ of the channel region to the gate tunneling current is given by

$$I_{\rm GC} = W \cdot \int_0^L J_{\rm GC}(y) \cdot dy. \tag{46}$$

In order to calculate the above integral, the current continuity equation has to be solved as

$$\partial I_{\rm DS}(y)/\partial y = -W \cdot J_{\rm GC}(y) \tag{47}$$

where $I_{\rm DS}$ is given by (16) and is no longer constant along the channel. Equation (47) cannot be solved explicitly and needs to be approximated for compact modeling purposes. The current continuity equation is solved under the assumption that $J_{\rm GC}$ only induces a small perturbation of the potential distribution along the channel (i.e., $\partial I_{\rm DS}/\partial y \approx 0$). We note in passing that this assumption implies that $I_{\rm DS}$ is approximately constant along the channel, and that all equations derived in Section III-E are still valid. With reference to the SLM

$$I_{\rm GC} = I_{\rm GINV} \cdot F_S(y_m) \cdot D(y_m) \cdot p_{\rm gc} \tag{48}$$

where, theoretically, $I_{\rm GINV}$ is $J_0 \cdot W \cdot L$, but is considered as an model parameter, y_m is given by (33), and $p_{\rm gc}$ is a function of ψ_m and $\Delta\psi$ [41]. The total gate-to-channel current $I_{\rm GC}$ is partitioned into a source ($I_{\rm GCS}$) and a drain component ($I_{\rm GCD}$) [15], [16]

$$I_{\rm GCD} = \frac{W}{L} \cdot \int_0^L y \cdot J_G(y) \cdot dy \tag{49}$$

and $I_{\rm GCS} = I_{\rm GC} - I_{\rm GCD}$. Again, using the SLM, the above integral results in

$$I_{\rm GCD} = I_{\rm GINV} \cdot F_S(y_m) \cdot D(y_m) \cdot p_{\rm gd} \tag{50}$$

where $p_{\rm gd}$ is a function of ψ_m and $\Delta\psi$ [41].

2) Gate Overlap Current: Essentially the same model for the tunneling current is used in both the channel and the overlap regions. However, in the latter case, the position dependence of the surface potential is negligible, and hence, the tunneling current density is approximately uniform. As a consequence, the gate overlap current $I_{\rm Gov}$ in an overlap region with applied

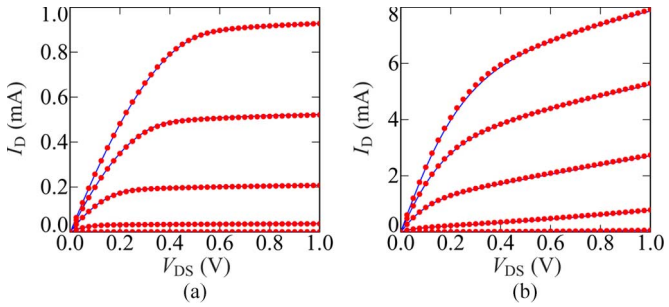


Fig. 11. Output characteristics of n-channel MOSFET for (a) $W/L = 10\ \mu m/1\ \mu m$ and (b) $W/L = 10\ \mu m/0.04\ \mu m$. $V_{GS} = 0$ to 1 V in steps of 0.2 V. Symbols and solid lines represent measured data and PSP, respectively.

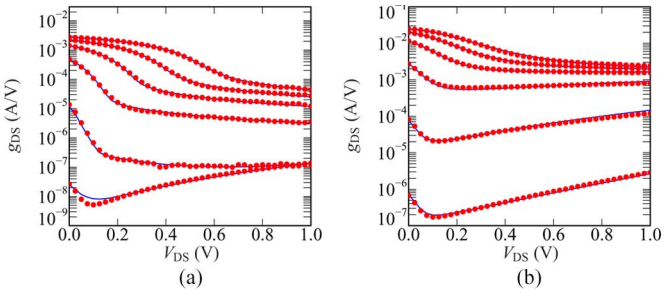


Fig. 12. Output conductances g_{DS} of n-channel MOSFET for (a) $W/L = 10\ \mu m/1\ \mu m$ and (b) $W/L = 10\ \mu m/0.04\ \mu m$. $V_{GS} = 0$ to 1 V in steps of 0.2 V. Symbols and solid lines represent measured data and PSP, respectively.

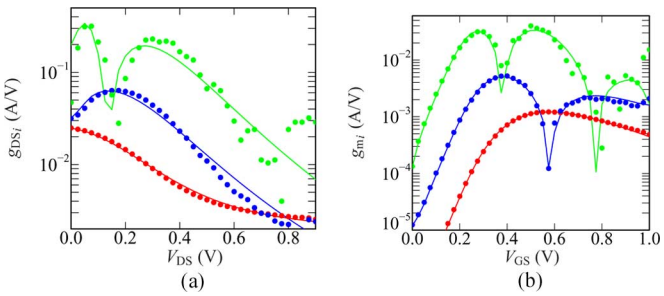


Fig. 13. (a) Higher-order conductances g_{DS_i} for $V_{GS} = 1$ V and (b) higher-order transconductances g_{m_i} for $V_{DS} = 0.025$ V; $W/L = 10\ \mu m/0.04\ \mu m$ n-channel MOSFET. $V_{SB} = 0$ V, i = 1 (lower curve), 2 (middle curve), and 3 (upper curve). Symbols and solid lines represent measured data and PSP, respectively.

gate bias V_{GX} (X denotes either S or D) and surface potential ψ_{OV} is written as

$$I_{Gov} = I_{Gov} \cdot F_S(\psi_{OV}, V_{GX}) \cdot D(z_{gov}) \tag{51}$$

where I_{Gov} is theoretically equal to $J_0 \cdot W \cdot L_{ov}$, L_{ov} is the length of the gate/source or gate/drain overlap region, and z_{gov} is equal to V_{OV}/χ_B. The above equation is used for both gate–source and gate–drain overlap current by making V_{GX} equal to V_{GS} or V_{GD}, respectively.

Including the above components, the model gives an accurate description of gate current over the whole operation region for both n- and p-channel devices. The PSP gate current model is symmetric with respect to the source–drain interchange [61].

D. Extrinsic Charges

For short-channel transistors, a major part of the total input capacitance C_{GG} is determined by the gate-to-source and gate-to-drain overlap capacitances. An accurate modeling of these bias-dependent overlap capacitances is thus important. In particular, the total charge in the overlap region becomes $Q_{XOV} = \text{CGOV} \cdot V_{OV}$, where CGOV is a model parameter accounting for the geometry of the overlap region. Here again, X denotes either source or drain (with corresponding changes in ψ_{OV}). Taken together with the analytical approximation of ψ_{OV} illustrated in Fig. 9, this expression provides a physical and computationally efficient description of the bias-dependent overlap charges, eliminating the need for the mostly empirical modeling of Q_{XOV} in older compact models.

V. Comparison With Test Data

The PSP model has been extensively verified by fitting MOSFET characteristics for several 180-, 130-, 90-, and 65-nm processes.

Typical dc results for the 65-nm process are shown in Figs. 11(a)–13(b). It has long been understood that to be useful in analog circuit simulations, the compact MOSFET model should accurately reproduce not only the drain current [Fig. 11(a) and (b)] but also the output conductance [Fig. 12(a) and (b)]. Note that in the PSP model, $g_{DS}(V_{DS})$ dependence is accurately reproduced for both short-channel and long-channel transistors. The latter includes almost linear variation of g_{DS} with V_{DS} in the saturation region associated with HALO implants.

The wide applications of CMOS technology in RF circuits make it essential to reproduce signal distortions associated with the nonlinearity of MOSFET characteristics. In particular, it becomes important to accurately model higher-order output conductances and transconductances. The ability of the PSP to accomplish this goal is illustrated in Fig. 13(a) and (b), where the higher-order drain conductances and transconductances are defined as $g_{DS}^{(i)} = \partial^i I_{DS}/\partial V_{DS}^i$ and $g_m^{(i)} = \partial^i I_{DS}/\partial V_{GS}^i$, respectively. Comparison with experimental data for the capacitance is presented in Fig. 14. Finally, the gate tunneling current is shown in Fig. 15, illustrating the model's accuracy for different values of the drain bias.

VI. Noise Model

For analog and RF applications, a good description of the low- and high-frequency noise properties of the MOSFET is a prerequisite. Consequently, PSP has the most complete and accurate models of all relevant noise sources.

A. Flicker Noise

The PSP flicker noise model is based on the correlated mobility fluctuation theory [76], [77], which is capable of capturing the rather different bias dependences of flicker noise for n- and p-channel MOSFETs. This theory also formed the basis of the BSIM3/4 flicker noise model. In PSP, however, it has been developed within the surface potential framework

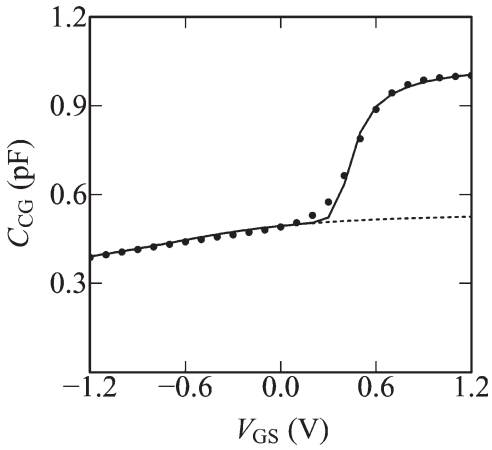


Fig. 14. Gate-to-channel capacitance C_{CG} $(= C_{SG} + C_{DG})$ for short-channel n-type MOSFET. $V_{SB} = V_{DS} = 0$ V, $W/L = 800\ \mu$m/90 nm. Symbols denote measurements, solid line denotes modeled extrinsic and intrinsic capacitances using PSP, and dashed line denotes modeled extrinsic capacitance using PSP.

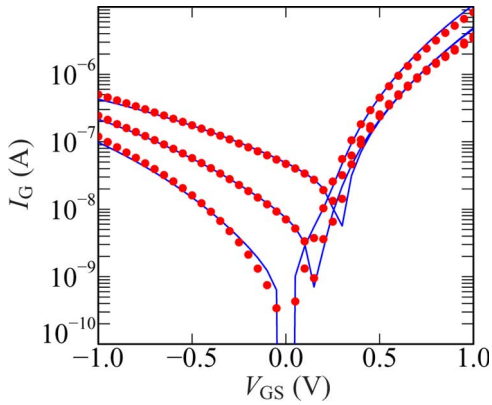


Fig. 15. Gate current I_G at $V_{SB} = 0$ V and $V_{DS} = 0$, 0.5, and 1 V for a $W/L = 10\ \mu$m/1 μm n-channel MOSFET. Symbols denote measurements, and lines represent modeled results using PSP.

leading to a smooth single-piece expression valid in all operation regions [64], [78], thereby removing the need for separate weak and strong inversion expressions, being glued together using smoothing functions.

B. Thermal Noise (Including Induced Gate Noise) and Other Noise Sources

The PSP thermal noise model is based on the so-called "improved Klaassen–Prins equation" [79], [80], which is a modification of the original Klaassen–Prins equation [81] to correctly include the effect of velocity saturation. Not only drain–current thermal noise but also induced gate noise and its correlation with drain–current thermal noise are included in PSP. This is mandatory for realistic simulations of circuits such as low-noise amplifiers. A key merit of our thermal noise modeling approach is that it only uses model parameters that are already determined from the standard dc and CV characterization: as opposed to, e.g., older models, no additional parameters are introduced to fit the noise data. The noise model has been verified extensively against experimental data. An example is

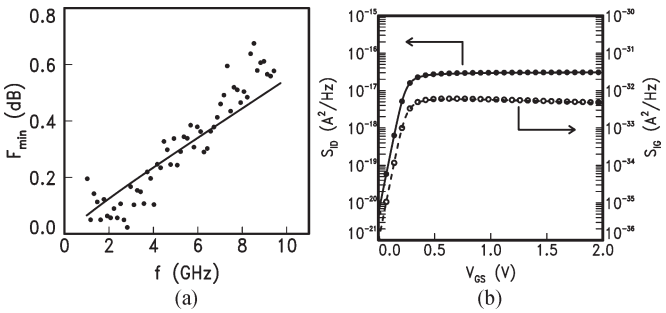


Fig. 16. (a) Minimum noise figure versus frequency for an $L = 100$ nm n-channel MOSFET in 90-nm CMOS technology. Markers are measured, line is PSP prediction. The bias condition is $V_{GS} = 0.85$ V and $V_{DS} = 0.9$ V. (b) Noise spectral densities of drain–current thermal noise (filled symbols) and induced gate noise ($f = 1$ kHz, open symbols) calculated with the PSP model for a $W/L = 10/0.1\ \mu$m n-channel MOSFET using the default parameter set with qmc $= 0$, $T = 290$ K, and $V_{DS} = 0$ V. The solid and dashed lines are the expected values for drain–current noise and induced gate noise, i.e., $4k_BTg_{DS}$ and (52), respectively.

shown in Fig. 16(a), where the minimum noise figure of a 100-nm n-channel MOSFET is shown to be correctly predicted by PSP. Further noise model verification on CMOS technologies from 0.35 μm down to the 100-nm node is available in [23], [25], [79], and [22]. Here, we will now focus on the behavior of the thermal noise model under some special bias conditions in order to demonstrate model consistency.

First, let us consider the situation of $V_{DS} = 0$. The drain–current noise spectral density is expected to be given by the simple Nyquist relation $S_{I_D} = 4k_BTg_{DS}$. Less well known, but noted in [80] and [82], the induced gate noise spectral density should under this condition reduce to

$$S_{I_G} = 4k_BT\left(2\pi f C_{GC}\right)^2 / 12g_{DS} \tag{52}$$

where C_{GC} is the intrinsic channel-to-gate capacitance. The above equation can be interpreted as the thermal noise emanating from the real part of the MOSFET input impedance, which is $1/(12g_{DS})$ at $V_{DS} = 0$ [29]. Indeed, for zero source–drain bias, both in subthreshold and strong inversion, the PSP expressions for drain–current thermal noise and induced gate noise reduce to $4k_BTg_{DS}$ and (52), respectively. This is demonstrated in Fig. 16(b). Note that the zero source–drain bias condition applies to the situation when the MOSFET is used as a capacitor. In this case, drain–current thermal noise has no contribution to the device noise since the source and drain are connected to each other, thereby short circuiting the thermal noise source between source and drain. Induced gate noise, as given by (52), becomes the dominant source of noise. Noise from the gate resistance [22] is less important in such cases because usually long channels are used when the MOSFET is used as a capacitor.

Another bias condition of special interest is the subthreshold region, which is becoming increasingly important in low-power applications. Also in this region, the drain–current noise is given by $4k_BTg_{DS}$ when $V_{DS} = 0$ (see above). For V_{DS} larger than a few ϕ_T, however, the noise in this region is known to be given by the shot-noise expression $2qI_{DS}$. Physically, shot noise in the subthreshold region and thermal noise in the inversion

stem from the same mechanism, i.e., velocity fluctuations of the charge carriers in the channel. In the surface-potential-based framework of PSP, they are automatically captured within the single-piece thermal noise equation. It has been shown analytically [22] that this equation indeed reduces to $2qI_{\rm DS}$ in the subthreshold region (for $V_{\rm DS}$ larger than a few ϕ_T). In addition to flicker noise, thermal noise, and induced gate noise, the PSP model contains shot noise of the gate leakage current, shot noise of the junction currents, and shot-like noise of the avalanche current [83].

VII. Conclusion

The development of the PSP model conclusively demonstrates the validity of the ψ_s-based approach to compact modeling for next-generation MOS transistors. The new model has been verified by comparison with test data for several advanced CMOS processes and accurately describes all physical phenomena—from HALO doping and retrograde profile to quantum effects—encountered in scaled MOS transistors. The mathematical structure of the model takes advantage of the rapid progress in MOS device physics and modeling accomplished during the last decade. In particular, both the intrinsic and extrinsic components of the model are essentially physics based and formulated in terms of the surface potential using the extended SLM. Traditional benchmark tests, as well as new requirements brought about by the extensive use of MOS technology for analog and RF applications, are automatically satisfied in view of the physical nature of the model. The PSP model has been placed in public domain, implemented in all major circuit simulators, and selected by the Compact Model Council as the new standard model for MOS transistors [84].

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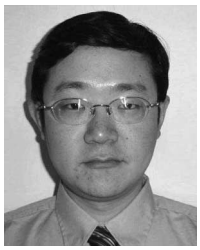

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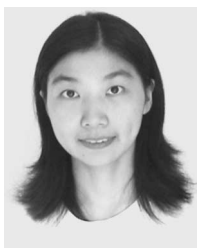

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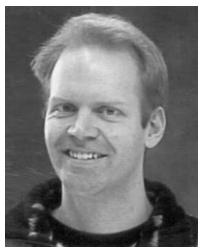

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