Extraction of Speculative SOI MOSFET Models Using Self-Heating-Free Targets

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Abstract—***Speculative SPICE models (also referred to as evaluation-level or guess models), which are extracted based on projected device electrical characteristics (called 'targets') rather than actual measurement data, are required to support concurrent IC designs. The self-heating effect in silicon-on-insulator (SOI) technologies presents additional challenges in obtaining quality speculative SOI MOSFET models. A novel 'shift-and-ratio' technique is developed to generate self-heating free device targets from raw targets provided only at room temperature, and a corresponding speculative model extraction methodology is proposed. The shift-and-ratio technique is validated by using silicon data of 65nm partially-depleted (PD) SOI technologies. The adequacy and self-consistency of the speculative model extraction methodology is demonstrated in field testing where a large number of 65nm and 45nm PD SOI speculative models are extracted. Availability of self-heating free targets proves to be critical not only for improved speculative model extraction efficiency, but also for model quality in general by ensuring physical and reasonable temperature dependences in the resulting speculative models.***

Index Terms—**Compact modeling, self-heating, SOI**

I. INTRODUCTION

Concurrent IC engineering, in which the circuitry is designed in parallel with process development, is highly desired for long-design-cycle products, such as microprocessors, in which the design time represents a significant fraction of the total time to market [1]. To support concurrent designs, speculative electrical (SPICE) models (variably referred to as evaluation-level [2] or guess models) must be provided early in the development cycle – in many cases, before significant silicon data is available.

Speculative models are extracted by fitting to device 'targets' – electrical characteristics projected based on extrapolation of previous technologies, key findings from unit process development, and committed performance predictions. Major device targets for digital applications often include conventional linear/saturation threshold voltages (V_{tlin} and V_{tsat}), saturation current (I_{dsat}), as well as less conventional ones such as 'high' drive current (I_{dh}), 'low' drive current (I_{dl}), and 'effective' drive current (I_{deff}) [3], as illustrated in Figure 1. To meet the challenges of high-performance and low-power circuit/system designs and ensure desired geometric dependences, targets are typically needed across multiple supply voltages (V_{DD}) per device and across devices of various dimensions [4].

In silicon-on-insulator (SOI) technologies, significant temperature rise in the device above ambient temperature, known as the self-heating effect, can occur under DC conditions because of low thermal conductivity of buried SiO_2 [5]. In compact models, it is handled by an auxiliary thermal circuit with a controlling model flag (such as *shmod* in [6]). When the thermal circuit is turned on, a compact model iteratively computes electrical characteristics and device temperature until both reach equilibrium. As the targets are ultimately based on regular DC measurement of some silicon (by inference or extrapolation), they are affected by self-heating. Consequently, fitting directly to these targets for model extraction requires inclusion of the thermal circuit during simulations, *i.e.*, simultaneous tuning of both non-temperature-related and temperature-related model parameters. Such a model extraction flow is usually characterized by a considerable number of extraction iterations [7].

As described above, extraction of SOI models even at room temperature alone requires certain knowledge about the model's response to temperature. The device targets, however, are usually available at room temperature only because of lack of information, and it is unclear which temperature dependences should be followed. In addition, a large number of model parameters are often used in model extraction as device improvement may result from various sources, such as stress engineering in conjunction with conventional gate oxide thickness and gate length scaling [3, 8]. A compact model, such as the industry-standard BSIM PD/SOI model [6], which meets very well most of the needs of digital designs and offers great flexibility, may exhibit certain undesired and unexpected correlations among model parameters. As a result, simultaneous modification of many model parameters (even if they are non-temperature related) can lead to significantly different temperature behavior, as it will be shown in Section V.

To overcome these difficulties, device targets free of the self-heating effect at multiple temperatures are highly desired for speculative SOI MOSFET model extraction. In this paper, a novel technique to generate self-heating-free targets and a corresponding model extraction methodology are described in Section II. Their field testing results and verification are demonstrated in Sections III and IV.

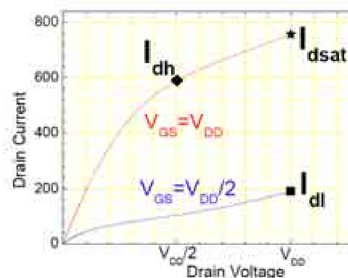

Figure 1. Illustration of sample device targets.

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II. METHODOLOGY

The self-heating effect under DC conditions is characterized by the device's thermal resistance (R_{th}) [5, 6]. For an SOI MOSFET with drain current I_D and drain voltage V_{DS}, the actual device temperature (T_D) is given as [7], $T_D=T_A+(I_D V_{DS})R_{th}$, where T_A is the ambient temperature. Therefore, raw device targets given at the same ambient temperature (typically room temperature) in fact correspond to different device temperatures set by their respective power levels.

This insight leads to a straightforward way of converting raw targets to self-heating-free targets by assigning each target its own (actual) temperature, thus allowing the thermal circuit to be turned off in simulations. Several limitations of this approach, however, may be quickly noticed. First and foremost, as numerous temperatures are now involved in model simulations, temperature-related parameters still need to be tuned simultaneously with other non-temperature-related parameters. Second, the temperature dependencies that need to be followed remain elusive. Finally, target visualization through familiar I-V characteristics (such as in Figure 1) becomes meaningless, for each target point now corresponds to a unique temperature. Therefore, simple though it may seem, such an approach fails to solve the technical issues that it is intended to address.

A more effective and practical solution may be proposed by exploiting the fact that the starting point for a speculative model usually is a known good model extracted using the latest available silicon data. It is helpful to conceptualize the drain current in a simplified, yet physical, form, $I_D=\left[W/(Lt_{ox})\right]\mu_{eff}f(V_T)$, where W/L are device's width and length, t_{ox} is the equivalent oxide thickness, μ_{eff} is the effective mobility, and $f(V_T)$ is a function of the threshold voltage (V_T) corresponding to a particular drain voltage at which I_D is measured. For a given bias condition, the drain current improvement (in ratio or percentage) from technology to technology might be assumed to remain constant over device temperature (although such a constant may vary with the bias condition such as following the mobility universal curve) *if* V_T and its dependence on temperature are kept unchanged between technologies. In this case, self-heating-free targets can be generated as illustrated in Figure 2. For a drain current target $I_{D,Raw}$ given at ambient temperature T_1, the actual device temperature T_2 is determined as $T_2=T_1+\delta T$, where $\delta T=I_{D,Raw}V_{DS}R_{th0}/W$, R_{th0} is the normalized thermal resistance in the starting model. Meanwhile, the starting model is simulated with the corresponding bias condition to yield drain currents I_1 and I_2 at device temperatures T_1 and T_2 (*i.e.*, by setting *shmod*=0 to turn off the thermal circuit), respectively. The current increase ratio is thus obtained as $I_{D,Raw}/I_2$ for the given bias condition, and the self-heating-free target at T_1 ($I_{1,SH0}$) is obtained as $I_1(I_{D,Raw}/I_2)$. Similarly, a self-heating-free target ($I_{X,SH0}$) at any temperature of interest, T_X, is obtained as $I_X(I_{D,Raw}/I_2)$, where I_X is the drain current of the starting model at device temperature T_X. Such a technique may be dubbed 'shift-and-ratio' for the way the current improvement is evaluated.

In case the targeted V_T is different from that of the starting model for a given drain voltage, the starting model is first modified to compensate for the amount of V_T difference (*e.g.*, by accordingly changing the model parameter V_{th0} in BSIM PD/SOI [9]), then followed by the shift-and-ratio technique. The whole procedure is repeated for each of the drain current targets to extract three sets of self-heating-free targets at three temperatures (*e.g.*, 0, 27, and 100°C). The speculative model is then extracted by fitting to all three sets of self-heating-free targets while keeping the same threshold voltage versus temperature dependence as in the starting model, as illustrated in Figure 3.

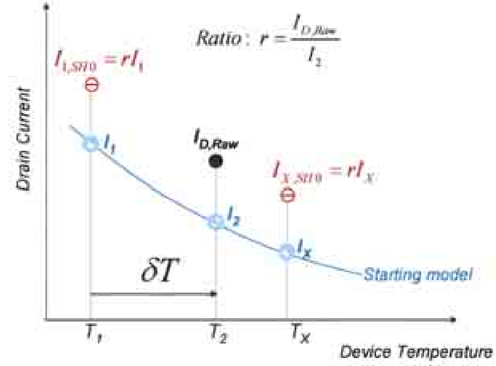

Figure 2. Illustration of the 'shift-and-ratio' method. $I_{D,Raw}$ is the raw drain current target at room temperature T_1.

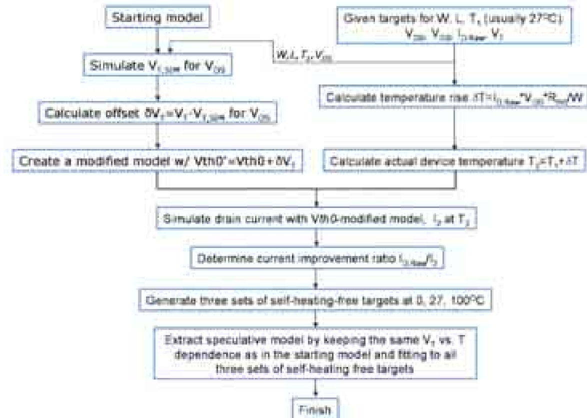

Figure 3. Flow chart of self-heating free target generation and proposed speculative model extraction methodology.

III. FIELD TESTING RESULTS

If the newly proposed shift-and-ratio technique and model extraction methodology work, the speculative model extracted by fitting to self-heating-free targets at three temperatures should fit to the raw drain current targets equally well once the thermal circuit is turned on to include self-heating (*i.e.*, *shmod*=1). The model-to-target fit quality for the example of a 65nm PD SOI speculative model extracted as described in Section II is illustrated in Figure 4, where the fit to the raw targets is indeed satisfactory.

The efficiency and self-consistency of the novel self-heating-free target generation technique and speculative model extraction methodology can be studied in a more quantitative way, through the correlation plot shown in

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Figure 5. in this plot, the relative error between the speculative model and a raw target at the room temperature is compared to its self-heating-free counterpart. A large number of 65nm and 45nm PD SOI speculative models, which were extracted by various engineers, are used in the study. As can be seen in Figure 5, the data points fall tightly along the unity-slope line that goes through the origin, clearly confirming adequacy of the new methodology. That is, a speculative model extracted to fit to self-heating-free targets satisfying a certain model quality assurance (QA) tolerance would satisfy the same QA tolerance when compared to the raw device targets.

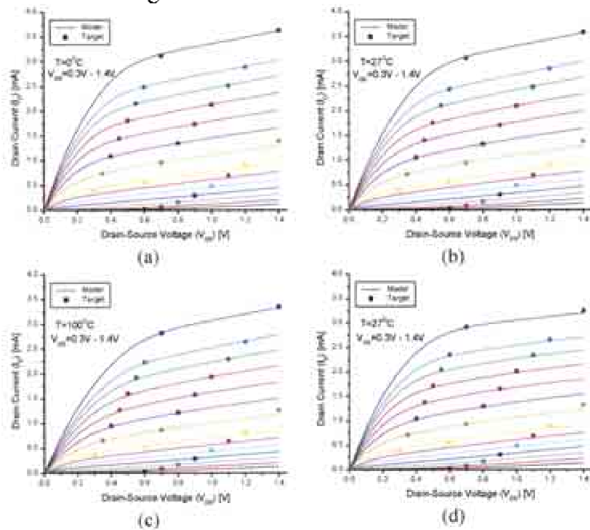

Figure 4. Fitting example of model to self-heating-free targets at 0, 27, and 100°C (a-c) & to raw targets at 27°C (d).

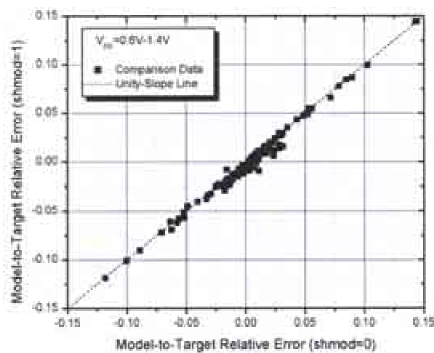

Figure 5. Fitting error correlation between model vs. raw targets and model vs. self-heating-free targets.

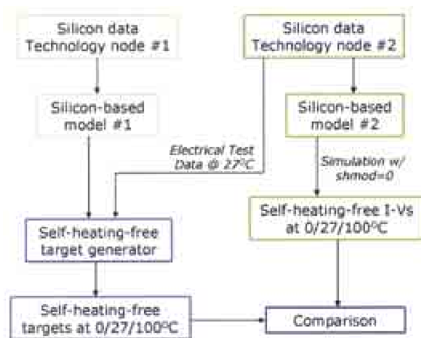

Figure 6. Si-data based verification scheme of shift-and-ratio technique and speculative model extraction methodology.

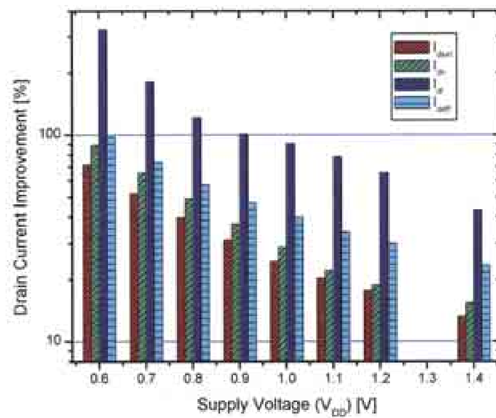

Figure 7. Drive current improvement (in percentage increase) of 65nm PD SOI technology node #2 over node #1.

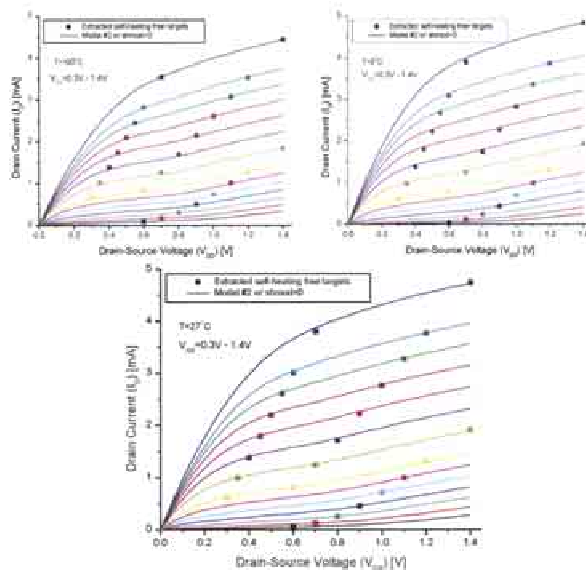

Figure 8. Comparison of self-heating-free I-V curves of model #2 with self-heating-free targets that are generated using model #1 and electrical test data of technology node #2.

IV. VERIFICATION RESULTS

While the field testing results have demonstrated the applicability and usefulness of the new methodology for speculative model extraction, they do not, however, answer the question of whether the temperature dependencies of the resulting speculative model, which are actually prescribed by the self-heating free targets, are physical and true to silicon data that will become available in the future. In essence, it is a question of the validity of the assumption that mobility enhancement remains constant over temperature as a first-order approximation. To address this issue and validate the methodology, an experiment using 65nm PD SOI silicon data is carried out (Figure 6). First, by closely fitting to measured silicon data from two nodes of the 65 nm technology, nodes #1 and #2 with considerable overall improvement (Figure 7), two respective silicon-based models, models #1 and #2, are generated independently. Second, key electrical test data from technology node #2 at

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room temperature and model #1 are used to generate 'self-heating-free targets' at three temperatures for technology node #2. Finally, these 'self-heating-free targets' are compared to simulated I-V curves of model #2 with *shmod*=0. The results are shown in Figure 8, where the close agreement validates the self-heating-free target generation and speculative model extraction methodology.

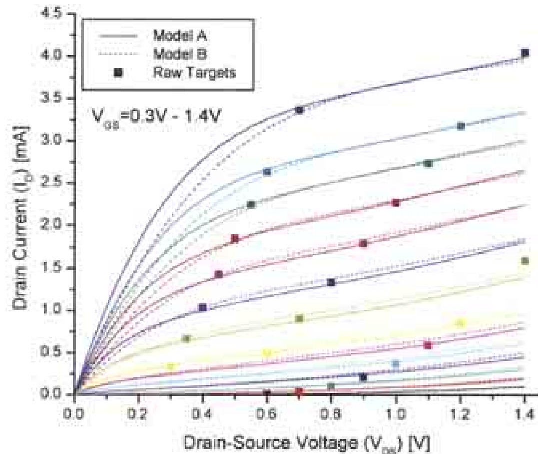

Figure 9. Comparison of two models having comparable fit to raw device targets.

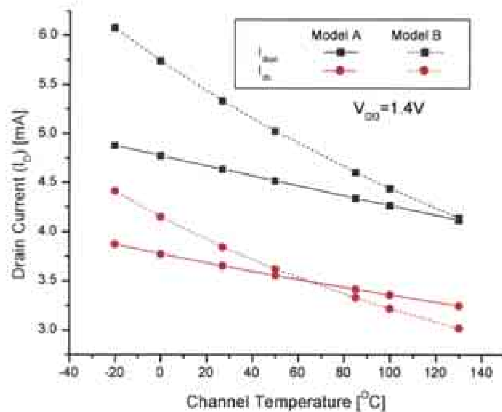

Figure 10. Illustration of drastic difference in temperature dependences between two models.

V. IMPACT ON MODEL QUALITY

The new self-heating-free target generation and speculative model extraction methodology removes uncertainty in temperature dependencies of the model being extracted by providing specific device targets at three temperatures. A case in point is comparison of two 65nm speculative models with raw device targets, illustrated in Figure 9. Both models are extracted from the same starting model. Model A is extracted using the new methodology, *i.e.*, by fitting to self-heating-free targets at three temperatures generated from the raw device targets, whereas Model B is generated by directly fitting to the same raw device targets. It is noteworthy that both models are obtained by changing only non-temperature-related model parameters. Visual inspection in Figure 9 may suggest that both models pass model QA in terms of model-to-raw-target fit for similar QA tolerance. However, when the two models are compared for temperature dependences (Figure 10), a drastic difference is observed: Model B reveals pathologically strong temperature dependencies. Without the new methodology, it would have been inefficient and difficult to identify, diagnose, and fix such a model defect.

VI. CONCLUSION

A novel shift-and-ratio technique is developed to generate self-heating-free targets from room-temperature raw device targets in SOI technologies, and a corresponding methodology is proposed for speculative SOI MOSFET model extraction to support concurrent IC designs. It is enabled by utilizing the temperature dependencies of the starting model and assuming that the drain current improvement from technology to technology is constant over device temperature for a given drain bias and a given gate overdrive. An experiment using 65nm PD SOI silicon data is carried out that validates the shift-and-ratio technique. The new model extraction methodology is verified in field testing where a large number of 65nm and 45nm PD SOI speculative models are extracted demonstrating its efficiency and self-consistency. Availability of self-heating-free targets not only improves efficiency of speculative SOI model extraction, but also ensures physical and reasonable temperature dependences in the resulting models.

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REFERENCES

[1] L. Bair, "Process/product interactions in a concurrent design environment," *Proc. IEEE CICC*, Sep. 2007, pp. 779-782.

[2] M.H. Na, *et al.*, "Predicting the SOI history effect using compact models," *Proc. Int. Conf. Modeling and Simulation of Microsystems*, 2004, vol. 2, pp. 183-186.

[3] M.H. Na, *et al.*, "The effective drive current in CMOS inverters," *Proc. IEEE IEDM*, Dec. 2002, pp.121-124.

[4] Q. Chen, Z.-Y. Wu, A.B. Icel, J.-S. Goo, S. Krishnan, C. Thuruthiyil, N. Subba, S. Suryagandh, J.X. An, T. Ly, M. Radwin, J. Yonemura, and F. Assad, "On Idlow with emphasis on speculative SPICE modeling," *Proc. Int. Conf. Modeling and Simulation of Microsystems*, May 2006, vol. 3, pp. 831-834.

[5] L.T. Su, J.E. Chung, D.A. Antoniadis, K.E. Goodson, and M.I. Flik, "Measurement and modeling of self-heating in SOI NMOSFET's," *IEEE T-ED*, vol. 41, pp. 69-75, 1994.

[6] P. Su, S.K.H. Fung, S. Tang, F. Assaderaghi, and C. Hu, "BSIMPD: a partial-depletion SOI MOSFET model for deep-submicron CMOS designs," *Proc. IEEE CICC*, Sep. 2000, pp. 197-200.

[7] Q. Chen, Z.-Y. Wu, R.Y.K. Su, J.-S. Goo, C. Thuruthiyil, M. Radwin, N. Subba, S. Suryagandh, T. Ly, V. Wason, J.X. An, and A.B. Icel, "Extraction of self-heating free I-V curves including the substrate current of PD SOI MOSFETs," *Proc. IEEE Int. Conf. Microelectronic Test Structures (ICMTS)*, Mar. 2007, pp. 272-275.

[8] S. Narasimha, *et al.*, "High performance 45-nm SOI technology with enhanced strain, porous low-k BEOL, and immersion lithography," *Proc. IEEE IEDM*, Dec. 2006, pp. 1-4.

[9] BSIM PD/SOI manual, University of California at Berkeley, http://www-device.eecs.berkeley.edu/~bsimsoi/get.html.

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