Critical Current (I_{CRIT}) Based SPICE Model Extraction for SRAM Cell

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Abstract—***Critical currents (I_{CRIT}) extracted from the N-curves of a 6-T SRAM bit cell have been shown in recent research to be important and effective figures of merit for the cell's stability and write-ability. SPICE models of cell transistors, therefore, not only need to fit closely to individual transistor's I-V characteristics, but also faithfully reproduce I_{CRIT}s' behavior of the cell as a whole. A branch current analysis is performed to reveal individual transistors' impact on I_{CRIT}s' and their key bias regions. Based on the insight from the analysis, an efficient SPICE model extraction flow is proposed that enables decoupled fine tuning of the pass-gate, pull-down, and pull-up transistor models to achieve satisfactory fit to I_{CRIT}s without model extraction iterations.***

Index Terms—**I_{CRIT}, N-Curve, Parameter extraction, SNM, SRAM, Stability, Write-ability**

I. Introduction

Static noise margin (SNM) of an SRAM bit cell is conventionally measured by the opening in the butterfly curve [1]. Two drawbacks of SNM, i.e., the inability to measure it with automatic inline testers and the inability to generate statistical information on SRAM stability fails, can be overcome by using the N-curve of the SRAM bit cell [2]. An N-curve is obtained by applying a voltage sweep to the internal storage node (Q) and measuring the resulting current flowing into the same node (Figure 1). Specifically, the peak current (I_{CRIT_RD}) in the N-curve for read (with both bit-lines clamped the supply voltage V_{DD}) was proposed as the cell stability margin parameter for it enables linear analysis and extrapolation in studying process variations' impact [2]. Its applicability to statistical study of cell stability was further illustrated in [3], and its linear correlation with SNM was experimentally demonstrated in [4]. Overall, I_{CRIT_RD} provides critical information of cell stability with respect to transistor sizing and V_{DD} scaling and can be used as a modeling metric [5].

The N-curve can be exploited to characterize not only cell stability, but also its write-ability. To this end, I_{CRIT_WR} is used and defined as the lowest current in the N-curve for *write* (Figure 2), which is obtained with one bit-line clamped to ground and the other to V_{DD}. I_{CRIT_WR} is similar to the write-trip current (WTI) [5], whereas the latter is extracted from the N-curve for *read*.

Given the criticalness of read stability and write-ability in SRAM cell operation, SPICE models of cell transistors not only need to closely fit to each transistor's I-V characteristics, but also faithfully reproduce these two key characteristics of the cell as a whole. Consequently, good agreement between silicon data and SPICE model simulations is required in I_{CRIT_RD}, I_{CRIT_WR}, and their behavior (such as V_{DD}, temperature dependences).

As SRAM cell transistors are usually of the minimum geometries found in the entire integrated circuit, SPICE model's scalability and process variations present a considerable challenge in model extraction. Individual SPICE models dedicated for the pass-gate and pull-down transistors, although they both are N-type MOSFETs, may be desired to yield improved I-V fit accuracy. Seemingly close I-V fit between simulation and silicon in all three SPICE models (pull-down, pull-up, and pass-gate), however, does not necessarily translate into acceptable fit in I_{CRIT_RD} and I_{CRIT_WR} across V_{DD} and temperature. Numerous ensuing model extraction iterations may normally be required.

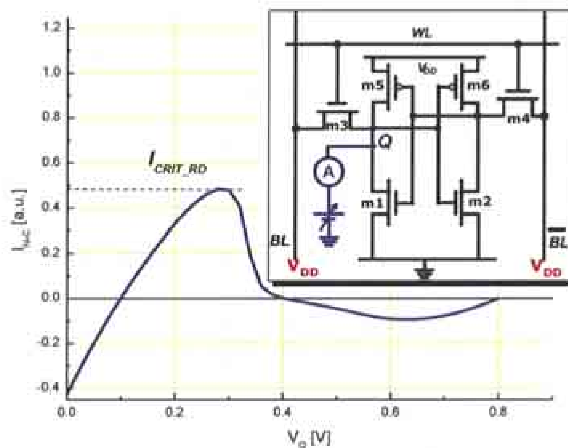

Figure 1. N-curve for read and definition of I_{CRIT_RD}. Measurement scheme is shown in the inset.

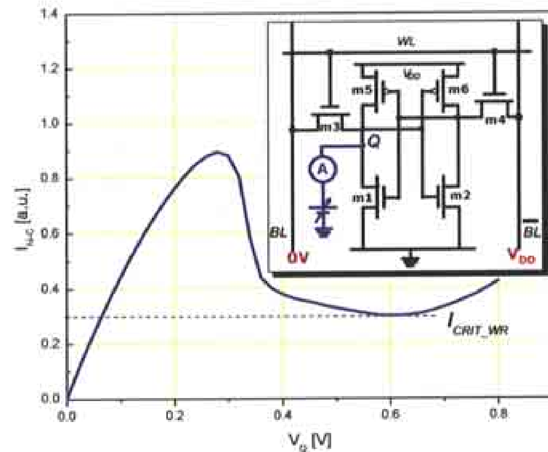

Figure 2. N-curve for write and definition of I_{CRIT_WR}. Measurement scheme is shown in the inset.

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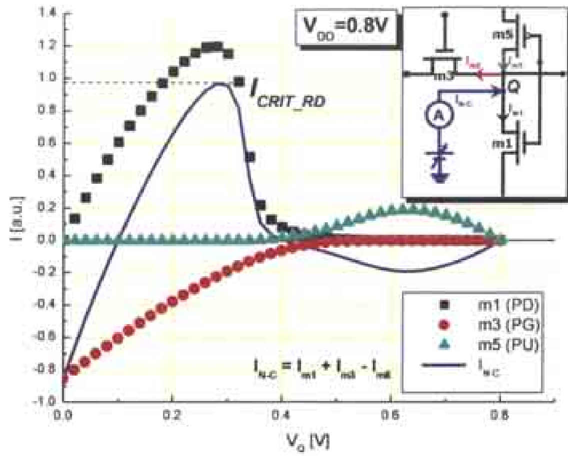

Figure 3. N-curve for read and other branch currents in response to voltage sweep (V_Q).

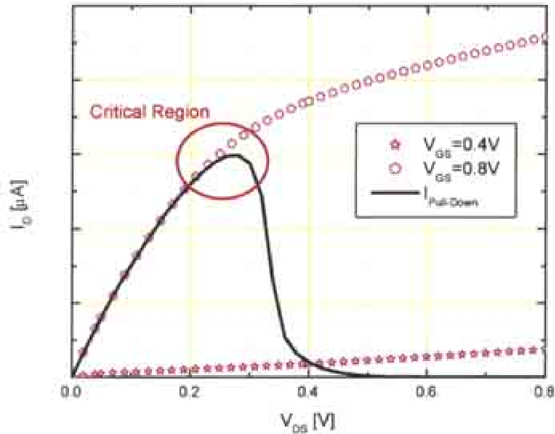

Figure 4. I_{m1}-V_Q sweep trajectory embedded in I_D vs. V_{DS} characteristics of the pull-down transistor (m1).

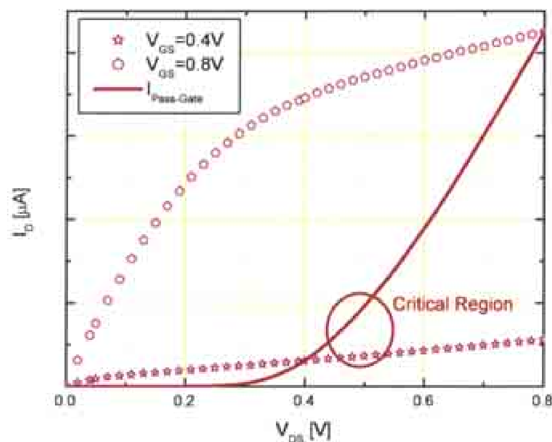

Figure 5. I_{m3}-V_Q sweep trajectory embedded in I_D vs. V_{DS} characteristics of the pass-gate transistor (m3).

In this paper, a branch current analysis is performed (in Section II) to identify key bias regions in cell transistors critical to I_{CRIT_RD} and I_{CRIT_WR}. An efficient SPICE model extraction flow is then proposed in Section III that delivers all three SPICE models for pull-down, pull-up, and pass-gate transistors, and ensures excellent I_{CRIT_RD} and I_{CRIT_WR} fit right in the first pass.

II. I_{CRIT} Branch Current Analysis

In order to explore individual transistor's effect on I_{CRIT}s, all the branch currents around the internal node Q can be measured in response to the voltage sweep, as shown in the inset of Figure 3. As dictated by KCL, the current that forms the N-curve, I_{N-C}, can be expressed as

$$I_{N-C} = I_{m1} + I_{m3} - I_{m5}, \quad (1)$$

where $I_{m1}/I_{m3}/I_{m5}$ are currents through the pull-down, pass-gate, and pull-up transistors, respectively. Figure 3 illustrates a typical N-curve for read and other corresponding branch currents. As can be seen, the peak current, I_{CRIT_RD} is determined by the currents through the pull-down (m1) and the pass-gate (m3) transistors only. Moreover, I_{m1} exerts much stronger influence on I_{CRIT_RD} than I_{m3} for the same percentage change as I_{m1} is generally much larger than I_{m3} under this particular bias condition. From the model extraction perspective, it clearly indicates that tuning of the pull-down device model is far more effective than tuning of the pass-gate device model in order to achieve a desirable I_{CRIT_RD} fit.

To further understand the actual device bias conditions where the model tuning is needed, it is instructive to embed the I-V_Q sweep trajectory in the regular I_D vs. V_{DS} characteristics of the pull-down and pass-gate devices. It is readily done by noticing $V_{DS,m1}=V_Q$ and $V_{DS,m3}=V_{DD}-V_Q$. The result is shown in Figure 4 for the pull-down device, where two I_D-V_{DS} curves are given with $V_{GS}=V_{DD}$ and $V_{GS}=V_{DD}/2$. It is apparent that the linear region of the pull-down transistor influences I_{CRIT_RD} most, and consequently deserves extra attention in model tuning and model-to-silicon fit accuracy. Similarly, embedding of the I-V_Q sweep trajectory in the I_D vs. V_{DS} curve family for the pass-gate transistor (Figure 5) indicates that its contribution to I_{CRIT_RD} comes from the saturation region with low to moderate gate-overdrive.

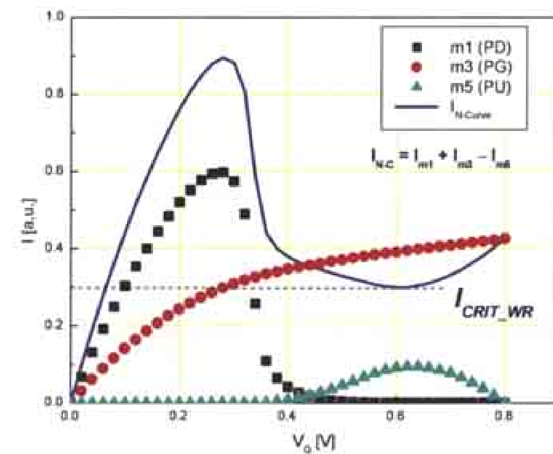

Figure 6. N-curve for write and other branch currents in response to voltage sweep (V_Q).

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The same branch current analysis and embedding technique can be applied for the N-curve for write and I_{CRIT_WR} (Figure 6). The pass-gate and pull-up transistors determine I_{CRIT_WR}, and the former exerts a stronger influence. I-V_Q sweep trajectories are embedded in the regular I_D vs. V_{DS} curves for the pass-gate and pull-up devices, in Figure 7 and Figure 8, respectively, by noticing $V_{DS,m3}=V_Q$ and $V_{DS,m5}=V_{DD}-V_Q$. In the pass-gate device, the saturation region, specifically between the 'high current' (I_{DH}) [6] and I_{DSAT}, is critical to I_{CRIT_WR}. In the pull-up device, the linear region contributes to I_{CRIT_WR}.

III. Model Extraction Methodology

The branch current analysis has revealed individual cell transistors' impact on I_{CRIT}s, and embedding of I-V_Q sweep trajectories in transistors' I-V characteristics have indicated critical bias regions where good model-to-silicon fit accuracy is particularly required and most effective to achieve satisfactory I_{CRIT} fit. The complex of these interactions and their relative strengths can be conveniently summarized in Table 1. Overall, the pull-up device model has the least effect on I_{CRIT}s, and the pass-gate device model and the pull-down device model have dominant influences on I_{CRIT_WR} and I_{CRIT_RD}, respectively.

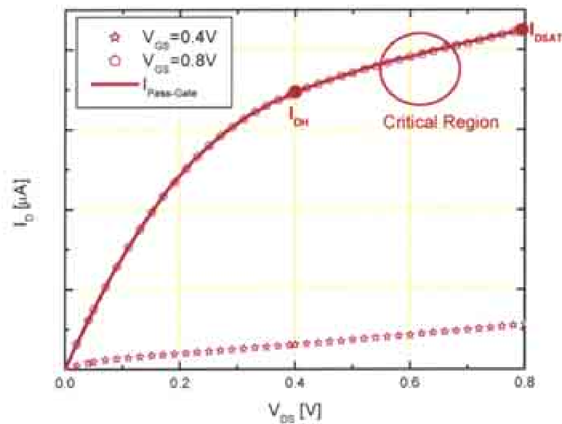

Figure 7. I_{m3}-V_Q sweep trajectory embedded in I_D vs. V_{DS} characteristics of the pass-gate transistor (m3).

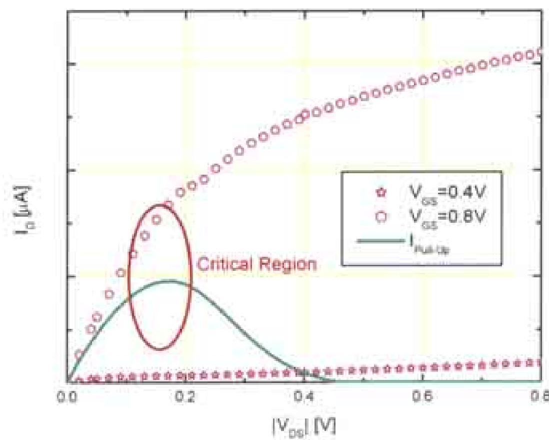

Figure 8. I_{m5}-V_Q sweep trajectory embedded in I_D vs. V_{DS} characteristics of the pull-up transistor (m5).

*Table 1. Interactions between individual models and I_{CRIT}s (**bold** font indicates dominant influence)*

Individual Models	*SRAM Cell Figures of Merit*	
	I_{CRIT_WR}	I_{CRIT_RD}
Pass-Gate	**I_{DH}-I_{DSAT} region**	Saturation region
Pull-Down		**Linear Region**
Pull-Up	Linear region	

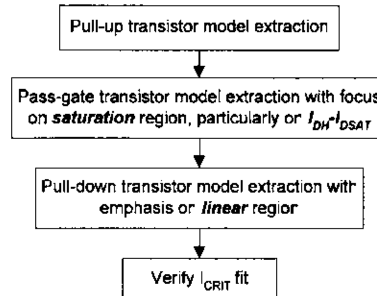

Figure 9. Proposed model extraction flow.

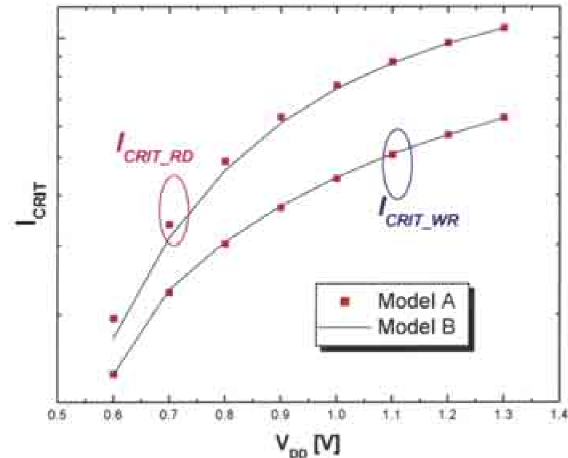

Figure 10. I_{CRIT} simulation comparison between pull-down transistor models A and B (with common pull-up and pass-gate transistor models).

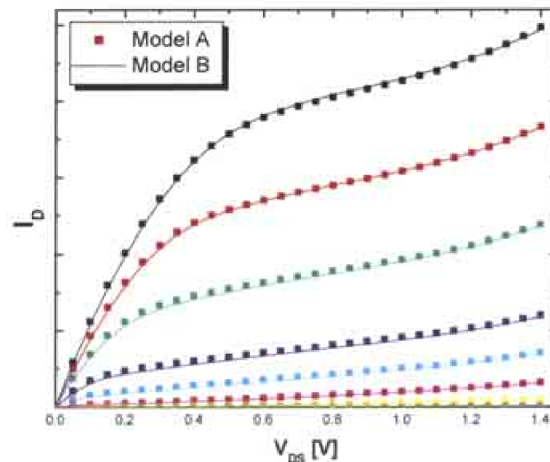

Figure 11. I_D-V_{DS} comparison between models A and B in the full bias range.

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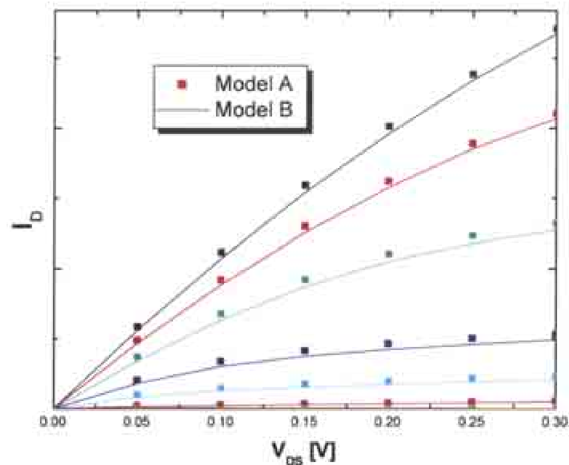

Figure 12. I_D-V_{DS} comparison between models A and B in the linear region.

Based on the above findings, a general extraction flow for all three cell transistor models is proposed, illustrated in Figure 9. It starts with extraction of the pull-up device model following the general fit quality guidelines. Second, the pass-gate device model is extracted, and the fit accuracy in the I_{DH}-I_{DSAT} region across V_{DD} is given the highest priority. Finally, extraction is done for the pull-down device model to ensure satisfactory fit in the linear region.

The proposed model extraction flow has been shown to be efficient in 65nm and 45nm SPICE model production for SRAM cell. In general, the resulting SPICE models of the pass-gate, pull-down, and pull-up device models deliver excellent model-to-silicon fit in I_{CRIT}s right in the first pass. In addition, the guidelines in the new model extraction flow on specific bias regions for model tuning enable effective implementation of automated SRAM cell model extraction by using commercial optimization engines. As an example, a 65nm experiment is demonstrated in Figure 10, where the I_{CRIT_RD} vs. V_{DD} dependence is fine tuned to the desired behavior (from Model A to Model B), particularly for supply voltages below 0.9V. Low-voltage I_{CRIT_RD}'s have been changed by as much as 12%. Such modifications are achieved by targeted adjustment in the linear region of the pull-down device model. While models A and B appear largely similar to each other in the overall bias range (Figure 11), the subtle changes in the linear region (Figure 12) are sufficient to obtain the desired I_{CRIT_RD}'s V_{DD} dependence.

IV. CONCLUSION

A branch current analysis is performed in the N-curve characterization of an SRAM bit cell. It reveals the effect of individual cell transistors on peak currents on the N-curves, known as I_{CRIT}s, which are important and effective figures of merits of SRAM cell's stability and write-ability. By embedding the sweep trajectories of branch currents in the regular I_D-V_{DS} curve family of corresponding cell transistors, specific bias regions of each cell transistor that are important to I_{CRIT}s' model-to-silicon fit are identified. Based on various interactions between individual transistors and the SRAM cell as whole and their relative strengths, a new model extraction flow is proposed. It enables efficient delivery of all three SPICE models for the pull-down, pull-up, and pass-gate devices that ensure excellent model-to-silicon fit in I_{CRIT}s across operating conditions right in the first pass.

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