Off-State Leakage Current Modeling in Low-Power/High-Performance Partially-Depleted (PD) Floating-Body (FB) SOI MOSFETs

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Abstract—***Off-state leakage current in a 65 nm partially depleted (PD) floating-body (FB) SOI technology is modeled and analyzed with emphasis on its drain-voltage dependence. Modeling accuracy of the off-state leakage current is highly dependent on modeling of parasitic currents, although their direct contribution to the leakage may be negligible in lower-power/high-performance technologies. The underlying physical mechanism, i.e., the FB effect, is also shown to be responsible for observed varying drain-induced-barrier-lowering (DIBL) or highly non-linear dependence of the threshold voltage on drain voltage. While characterization of parasitic currents may present a challenge because of unconventional geometry dependences, the off-state leakage current and its fitting accuracy may be used as an indirect, effective figure of merit.***

Index Terms—**Drain-induced barrier lowering (DIBL), Floating-body (FB) effect, Leakage current, Partially-depleted (PD), Silicon-on-insulator (SOI), Threshold voltage**

I. Introduction

As the design complexity increases and MOSFET scaling continues relentlessly, the overall power consumption of integrated circuits is an urgent challenge. Its standby or static component, however, may be even more severe, threatening the survival of CMOS technology itself [1]. It is further exacerbated by the exponential nature of the leakage current's dependences on process/voltage/temperature (PVT) in light of increased technology variability. Therefore, accurate modeling of the off-state leakage current in MOSFETs is imperative for circuit- and system-level design to properly estimate and achieve manageable static power.

The off-state leakage current of an MOSFET (I_{OFF}), *i.e.*, the drain current at zero gate voltage (V_{GS}) and non-zero drain voltage (V_{DS}), consists of various components [2]: 1) the subthreshold (*i.e.*, channel) leakage, 2) the drain-to-body reverse biased junction current, 3) the impact ionization current, 4) the gate-induced-drain-leakage (GIDL) current, and 5) the gate-to-drain tunneling current through the overlap region, as shown in Figure 1. With the advent of high-k gate dielectrics [3], the gate tunneling current may be controlled to a level lower than other components [2]. The GIDL and impact ionization currents both reduce as the supply voltage (V_{DD}) is scaled down [2,4].

In low-power/high-performance technologies, the supply voltage is chosen as low as feasible to minimize the overall power consumption, whereas the threshold voltage (V_t) is reduced as much as possible to provide enough gate over-drive for performance. As a result of such a V_{DD} vs. V_t optimization, the subthreshold leakage current, which is directly determined by V_t, overwhelms all the other leakage mechanisms. In this paper, such an off-state leakage current scenario is analyzed in a 65 nm partially-depleted (PD) floating-body (FB) SOI technology, and PD FB SOI-specific modeling techniques are proposed (Section II). In Section III, characterization challenges and opportunities for accurate leakage current modeling are discussed.

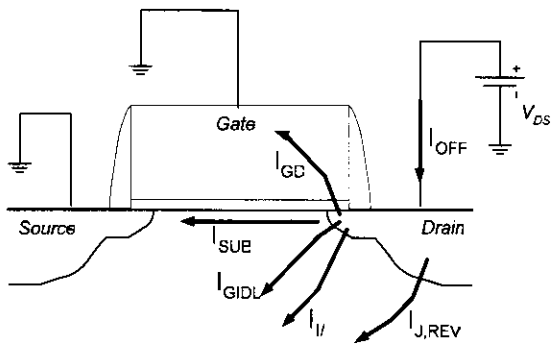

Figure 1. Illustration of currents contributing to the off-state leakage current in a MOSFET.

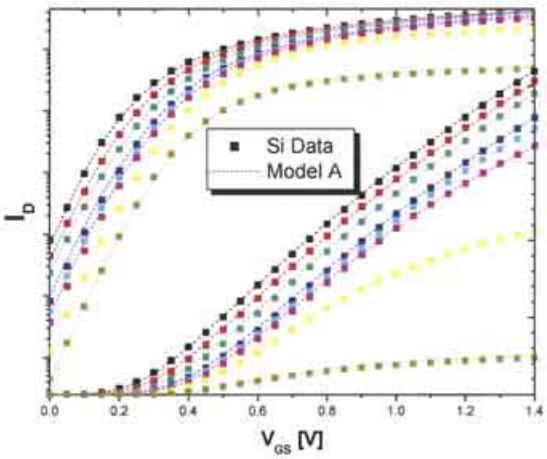

Figure 2. Model-to-Si data comparison for a 65 nm PD FB SOI MOSFET (in log and linear scales, respectively).

II. I_{OFF} Modeling Techniques in PD FB SOI MOSFETs

An N-type MOSFET Spice model (denoted as Model A) based on BSIMSOI [5] is extracted in a 65 nm PD SOI technology, using Si data of devices that are selected to be representative of multi-wafer, multi-site measurement results [6]. The model fits to the body-effect and parasitic currents of companion tied-body devices, and then fits to the FB transistors' I-V characteristics. The resulting model-to-Si fit, illustrated in Figure 2 on the example of I_D-V_{GS} curves,

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appears rather close across various V_{DS}. A more detailed examination in the subthreshold region and the off-state leakage, however, reveals noticeably different dependencies of I_{OFF} on V_{DS} between the model and Si, as shown in Figure 3. While I_{OFF} vs. V_{DS} fit is indeed good at V_{DS}=0.05V and 1.0V, the model-to-Si discrepancy V_{DS} may be as high as 40% at moderate and low V_{DS}.

To explore the causes for such I_{OFF} modeling inaccuracy, I_{OFF} vs. V_t correlation is studied in Figure 4, for I_{OFF} is known to be dominated by the subthreshold channel current in the technology of interest. Tight data/model distribution confirms that the subthreshold slope is of purely electrostatic nature and well modeled in general. In particular, in the low-to-moderate V_{DS} region, where I_{OFF} vs. V_{DD} discrepancy is prominent, I_{OFF} vs. V_t exhibits very little difference between the model and Si data.

The above observation naturally leads to inspection of the V_t modeling, given in Figure 5, which compares the model and Si for DIBL. In this comparison, the model-to-Si discrepancy in the low-to-moderate V_{DS} once again manifests itself. Modifying the DIBL-related parameters (*dsub*, *etao*) in BSIMSOI's Vt formulation [5],

$$V_t = V_{th0} + \ldots - \left[\exp\left(-D_{sub}\frac{L_{eff}}{2l_{te}}\right) + 2\exp\left(-D_{sub}\frac{L_{eff}}{l_{te}}\right)\right](E_{tae} + E_{taeb}V_{bseff})V_{DS} \quad (1)$$

however, will not resolve the issue because it affects V_t across V_{DS} and leads to deterioration of the already good V_t fit at 1V. Consequently, the I_{OFF} vs. V_{DS} modeling inaccuracy seems traceable to the body-voltage (V_{PS}) modeling, which is the only other remaining factor that influences V_t through the body effect.

A modeling experiment is carried out to verify the hypothesis. As V_{PS} in DC conditions is determined by various parasitic currents [7], the junction I-V characteristics are chosen for modification to look for improvement in I_{OFF} vs. V_{DS} fit. For simplicity, only the reverse bias I-V characteristics are manipulated while the forward bias region is kept unchanged (Figure 6), which is possible because of great flexibility of BSIMSOI. Changing a few recombination and tunneling parameters (such as *nrecro*, *isrec*, *istun* and *vtuno* [5]) results in Model B, greatly improving the I_{OFF} vs. V_{DS} fit as well as the overall subthreshold region fit (Figures 7 and 8). Meanwhile, the model-to-Si fit in other regions of I_D-V_{GS} and I_D-V_{DS} is not compromised (Figures 7, 9, and 10).

III. Characterization Challenges & Opportunities

Adjustment of the reverse bias junction I-V characteristics has been shown to achieve excellent I_{OFF} vs. V_{DS} fit. The necessary adjustment, however, appears rather significant. Given the importance of parasitic currents in PD SOI-specific circuit phenomena, such as hysteresis [7], such an adjustment requires comprehensive understanding and substantiation.

To this end, junction I-V characteristics of three companion tied-body transistors of various geometries are compared with models A and B (Figure 11). It turns out that Model A was originally extracted to fit to the junction characteristics of the widest ('4*W') tied-body device (which also happens to be a long-channel transistor). It was so selected because it provides a relatively high current level in measurement for better signal-to-noise ratio. Model B, on the other hand, is remarkably close to the Si data of the short-channel tied-body transistor of nominal width ('W'), although the model itself was arrived at from the FB I_{OFF} vs. V_{DS} fit perspective only.

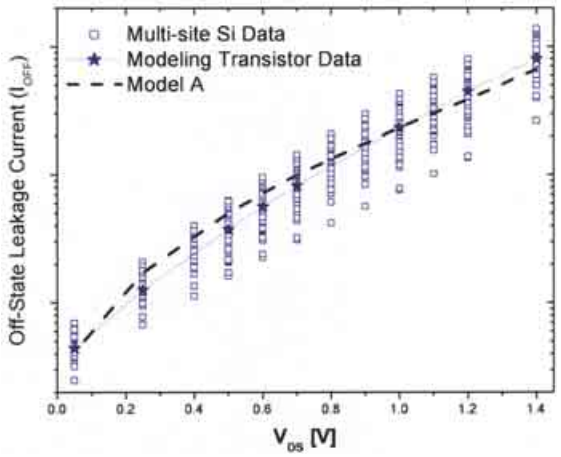

Figure 3. I_{OFF} comparison among the model, the modeling transistor data, and in-line/multi-site measurement data.

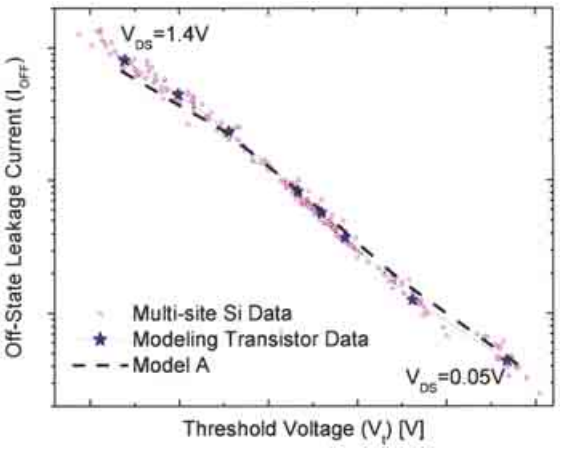

Figure 4. Correlation plot of I_{OFF} vs. threshold voltage (V_t) at different V_{DS}.

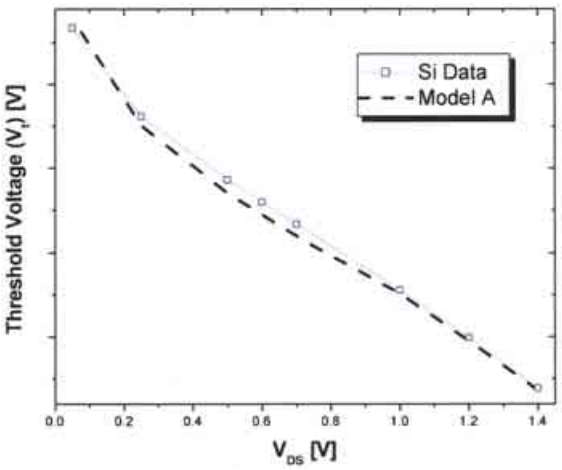

Figure 5. DIBL comparison: V_t vs. V_{DS}.

The apparent geometry dependence of junction I-V characteristics in the large reverse bias region may be explained by the width-dependent trap-assisted-tunneling (TAT) current [8]. As a result of the un-scalable portion of the tunneling current near the Si-STI (shallow-trench-isolation) interface, narrow-width devices exhibit a higher width-normalized TAT current. In addition, certain geometry dependence is also observed in the low reverse bias region (Figure 11), where the generation current is supposed to dominate. Whether such dependence is merely measurement inconsistency or caused by physical mechanisms needs further exploration.

The off-state body voltage in a FB PD SOI MOSFET is not only determined by the source- and drain-junction currents, but also by other parasitic currents such as GIDL and impact ionization current [7]. Consequently, both of these components also need to be modeled well.

As discussed above, to capture and model all the parasitic currents, accurate measurement, careful selection of modeling transistors for Si data, and perhaps additional model improvement are required. These rigorous requirements, however, may not all be satisfied in industry environment for various reasons such as schedule pressure, limited modeling transistor matrix, and data imperfection. The modeling experiment discussed in this paper, nonetheless, encouragingly demonstrates that the I_{OFF} vs. V_{DS} dependence in FB SOI transistors can, in effect, be used to guide parameter extraction for parasitic currents. The I_{OFF} vs. V_{DS} fit quality can serve an indirect figure of merit for parasitic currents modeling.

Finally, V_t vs. V_{DS} dependence in FB PD SOI MOSFETs becomes highly-nonlinear because of, and is influenced by, parasitic currents (Figure 12). While it is well captured in physical compact models such as BSIMSOI, the constant DIBL approach that is used in conventional I_{OFF}-specific modeling [2,9] is less adequate in lower supply voltage technologies. Simply taking the difference between the linear V_t (ex., V_{DS}=0.05V) and 1V saturation V_t as DIBL and using it for other V_{DS} will lead to considerable inaccuracy in V_t estimate as well as I_{OFF} calculation.

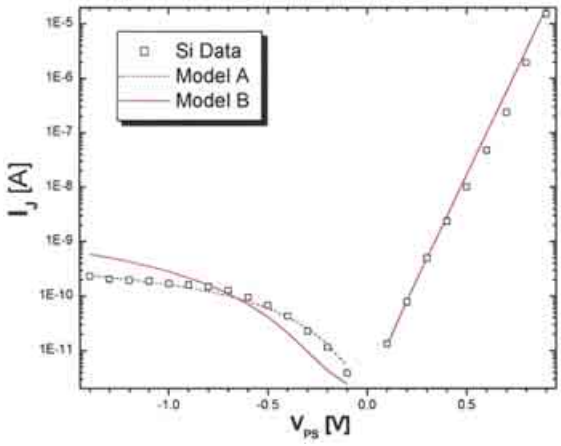

Figure 6. Junction I-V adjustment needed to improve I_{OFF} vs V_{DS} fit.

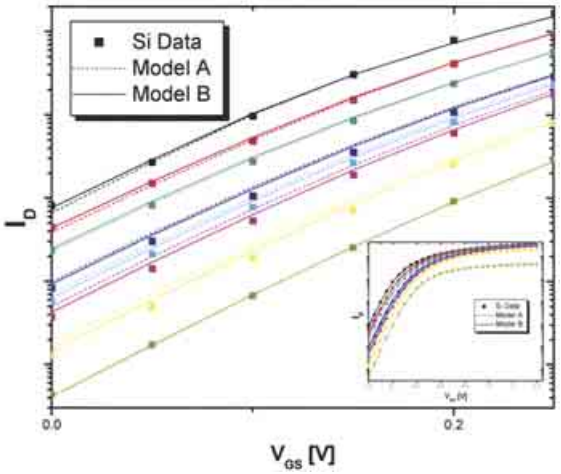

Figure 7. Subthreshold region and overall I_D-V_{GS} comparison before and after junction I-V adjustment.

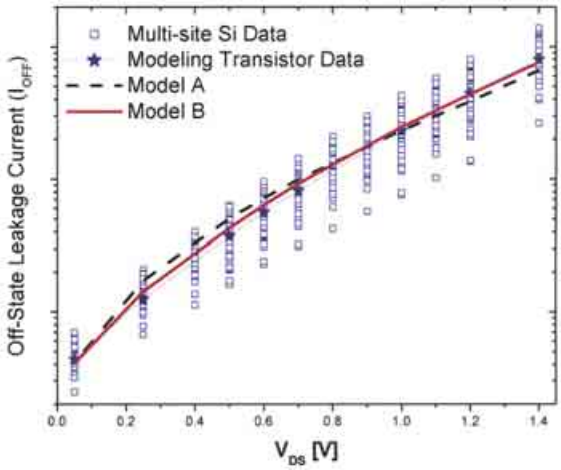

Figure 8. I_{OFF} comparison among the model, the modeling transistor data, and in-line/multi-site measurement data before and after junction I-V adjustment.

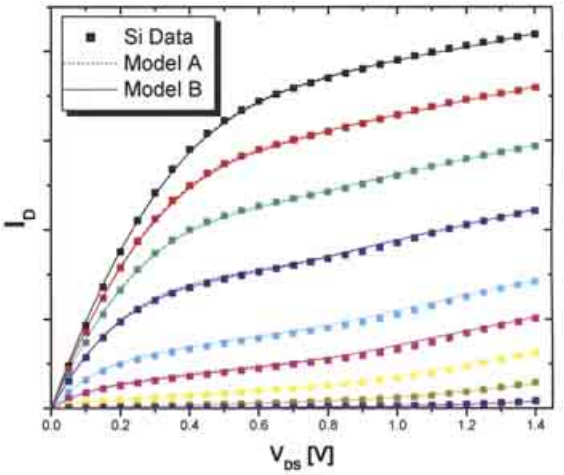

Figure 9. I_D-V_{DS} comparison before and after junction I-V adjustment.

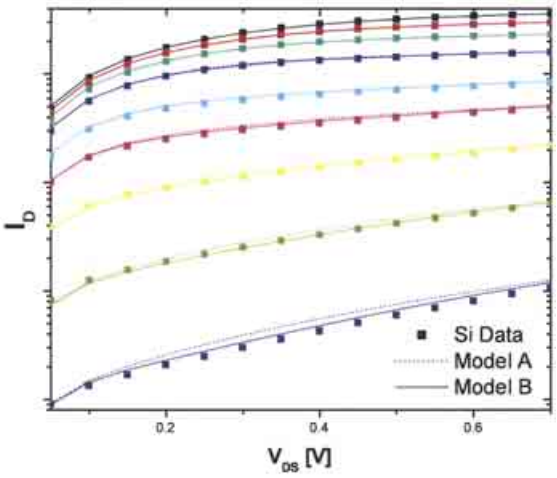

Figure 10. Low-to-moderate bias I_D-V_{DS} comparison before and after junction I-V adjustment.

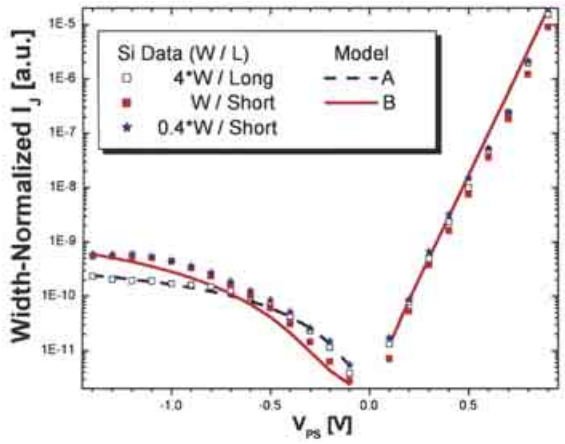

Figure 11. Comparison of width-normalized junction I-V characteristics in three tied-body transistors and two models.

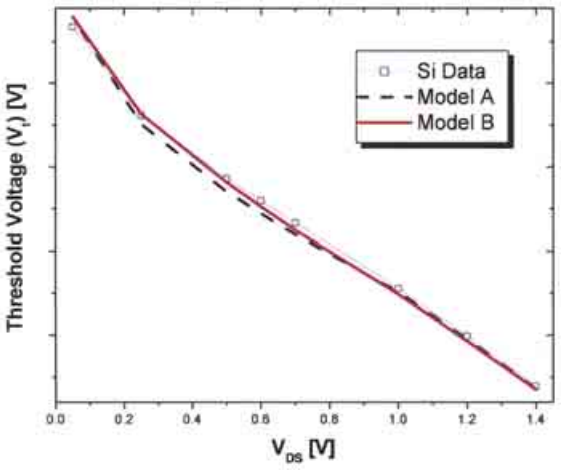

Figure 12. Non-linear V_t vs. V_{DS} dependence and effect of parasitic currents adjustment.

IV. Conclusion

Model-to-Si fit of the off-state leakage across drain voltage is analyzed in a 65 nm low-power/high-performance PD FB SOI technology, in which the subthreshold channel current dominates as a result of device optimization. It is shown that the I_{OFF} vs. V_{DS} dependence is heavily influenced by modeling of parasitic currents through the FB effect. Accurate I_{OFF} vs. V_{DS} modeling thus requires accurate measurement of parasitic currents, careful selection of modeling transistors, and improvement in compact models to take into account geometry dependence of TAT. On the other hand, it is demonstrated that the I_{OFF} vs. V_{DS} dependence can be effectively used to guide parameter extraction in parasitic currents modeling, and its fit quality can serve as an indirect figure of merit. Finally, highly non-linear V_t vs. V_{DS} dependence results from parasitic currents and the FB effect, and the conventional constant DIBL approach used in I_{OFF}-specific modeling may become inadequate even in low-supply-voltage technologies.

Acknowledgment

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