

Extraction of Self-Heating Free I-V Curves Including the Substrate Current of PD SOI MOSFETs

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Abstract—A new methodology is proposed to extract self-heating free I-V curves, including the substrate current, of SOI MOSFETs based on triple-temperature, regular DC measurement. It is verified to be accurate with Hspice simulations and suitable for SPICE model parameter extraction. It is also demonstrated that extraction of self-heating free I-V curves is not only desired for efficient SPICE model generation, but also required to accurately capture the true temperature dependences in the models.

Index Terms—Compact modeling, self-heating, SOI, substrate current

I. INTRODUCTION

The low thermal conductivity of SiO₂ leads to significant self-heating in silicon-on-insulator (SOI) MOSFETs in comparison to bulk FETs [1]. Such a self-heating effect is taken into account in compact SPICE models by using an auxiliary $R_{th}C_{th}$ circuit [2], where R_{th} and C_{th} are the effective thermal resistance and thermal capacitance of the device structure, respectively, as illustrated in Figure 1. As the self-heating mode (SHMOD) is turned ON (SHMOD=1) in the models, for example, the DC simulated I-V characteristics are the result of converged balance between the power dissipation ($I_{ds}V_{ds}$, i.e., drain current by drain voltage) and the heat transfer ($\Delta T/R_{th}$), where ΔT is the temperature rise in the device over the ambient temperature (T_A). Consequently, direct use of the I-V characteristics of SOI devices obtained from regular DC measurement for model extraction necessitates simultaneous tuning of non-temperature related and temperature related model parameters. It may lead to numerous iterations in model extraction (Figure 2), and more importantly, as shall be seen later, may degrade the model quality in general.

Sophisticated direct measurement techniques for self-heating free I-V characteristics, such as pulsed I-V measurement [3], have been commercialized and made more accessible recently [4]. Many technical challenges characteristic to high-frequency measurement, such as cable impedance match and signal compensation, have been specifically addressed in the tools [4]. Delicate RF pads and device layout design aside, however, a number of other issues continue to pose inherent limitations on the pulsed I-V technique in its application to compact model extraction [5]: 1) a limited range of suitable device width bounded by voltage resolution of the oscilloscope and the loadline's restriction on measurable I-V values; 2) additional complication by the floating body (FB) in the case of partially depleted (PD) FB SOI MOSFETs, manifest as I-V's dependence on pulse period; 3) inability to measure

subthreshold I-V characteristics as well as the substrate current, which is considerably influenced by self-heating in PD SOI MOSFETs [6].

In this paper, a new methodology is proposed to extract self-heating free I-V characteristics of PD SOI MOSFETs, including the substrate current, based on triple-temperature, regular DC I-V measurement. The new methodology is verified by Hspice simulations and benchmarked against a previously reported method [7]. Implications of the new methodology for PD SOI SPICE model extraction and model quality assurance (QA) are also discussed.

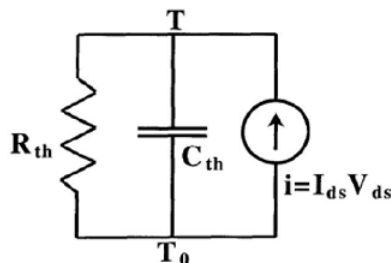


Figure 1 Thermal auxiliary circuit in SOI SPICE models [2] controlled by a model flag, SHMOD, the “self-heating mode”, SHMOD=1 or 0 for its inclusion or exclusion, respectively.

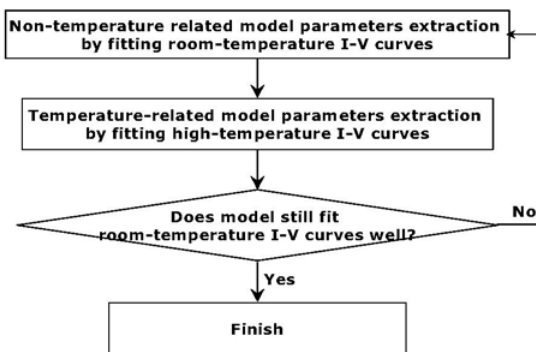


Figure 2 Scheme of typical model extraction flow by *directly* fitting regular, DC-measured I-V curves of SOI MOSFETs.

II. METHODOLOGY AND RESULTS

In the regular DC I-V measurement at a fixed wafer chuck temperature T_A , the actual channel temperature, T_D , is established to balance the power dissipation and heat transfer from the device under test, and varies with the device's

terminal voltages (Figure 3). For a given set of terminal voltages, the channel temperature can be evaluated as $T_D = T_A + \Delta T$, where $\Delta T = I_{ds} V_{ds} R_{th0} / W$, and W is the device width. R_{th0} is the normalized thermal resistance, which can be obtained by electrical resistance measurement of the polysilicon gate [8]. Consequently, the current value I_M obtained from regular DC measurement at the wafer chuck temperature T_A , which is affected by self-heating, is actually the “self-heating free” current at T_D (Figure 4). Such a (T_D, I_M) pair is unique for a given device biased at a given set of terminal voltages, and an assembly of similar pairs form the unique dependence of the current on the channel temperature, $I=f(T)$. Therefore, the task of extracting the self-heating free current for the given terminal voltages at any temperature T_A is simply to compute the function $f(T)$ at $T=T_A$.

The simplest approximation to $I=f(T)$ is the linear function with two constants a_0 and a_1 , $I(T)=a_0+a_1T$, determination of which requires regular DC measurement at just two different wafer chuck temperatures. It is essentially the previously reported method for self-heating effect removal [7]. Simple as it is, such a method has been observed to give inaccurate extraction results with respect to Hspice simulations. Moreover, the percentage difference between the self-heating-OFF and -ON currents, which is often used in SPICE model QA, can be shown to be equal to $-a_1 V_{ds} R_{th0} / W$ with this method. It is a quantity independent of temperature, which is inconsistent with Hspice simulation results. An example of above mentioned observations is given in Table 1 using a 65nm PD SOI model.

A natural improvement is to exploit the quadratic approximation to $I=f(T)$, $f(T)=a_0+a_1T+a_2T^2$, which can be accomplished through regular DC I-V measurement at triple wafer chuck temperatures (Figure 5). The quadratic dependence may be particularly needed for the substrate current, which may have a stronger non-linear relationship to channel temperature, as illustrated in Figure 6. The increase of the substrate current with channel temperature [9] explains enhanced impact ionization in SOI MOSFETs in comparison to bulk devices [6, 10] as a result of self-heating.

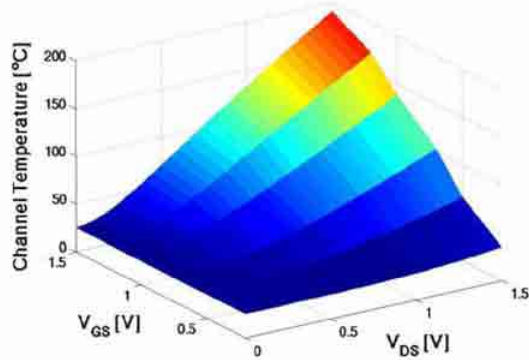


Figure 3 Hspice-simulated channel temperature of PD SOI MOSFETs in regular DC I-V measurement as a function of terminal voltages.

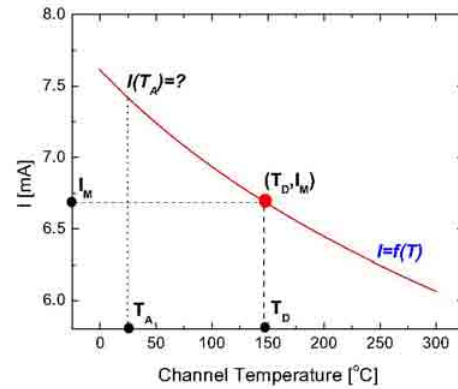


Figure 4 General concept of self-heating free current extraction for a given set of terminal voltages.

Table 1 Self-heating free drive current I_{dsat} ($V_{DD}=1.5V$), extracted from Hspice simulated I_{dsat} with self-heating mode turned ON (SHMOD=1) at two temperatures, in comparison with Hspice simulated I_{dsat} with self-heating mode turned OFF (SHMOD=0)

T [°C]	$I_{d,SH=1}$ [μA]	$I_{d,SH=0}$ [μA]			$I_{d,SH=0}/I_{d,SH=1}-1$	
		Hspice	Extracted	Diff%	Hspice	Extracted
25	519	678	653	-3.8%	30.8%	25.8%
100	472	601	594	-1.2%	27.4%	25.8%

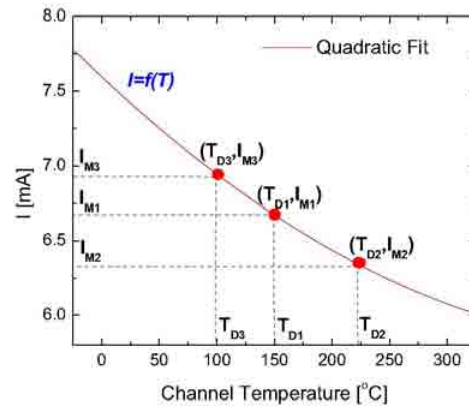


Figure 5 Illustration of triple-temperature based extraction methodology

The new extraction methodology can be efficiently implemented (Figure 7), and applied to the channel current as well as the substrate current. Comparison of the extracted self-heating free I-V curves and Hspice simulated I-V curves with self-heating mode turned OFF demonstrates encouraging results in both cases (Figure 8 and Figure 9). Noticeable improvement in the extraction results has been achieved in comparison to the previously reported dual-temperature based method (Figure 10) (on the example of the same SPICE model card used in Table 1).

It is worth pointing out that the validity and accuracy of the new extraction methodology is verified against self-heating free Hspice simulations, which themselves are reasonable

approximations to physical reality contingent upon certain assumptions, such as evaluation of the normalized thermal resistance R_{th0} . Determined as the channel temperature versus device's power dissipation slope per reciprocal of device width, R_{th0} 's measurement involves [8]: 1) gate temperature profiling to deduce the actual gate temperature right above the channel region, and 2) systematic uncertainty between deduced gate temperature and the actual channel temperature. Consequently, accuracy of the new extraction methodology with respect to actual self-heating free I-V curves such as obtained from pulsed I-V measurement relies on accuracy of R_{th0} just as accuracy of Hspice simulations does. In the context of compact modeling and circuit simulation, however, the new extraction methodology does reproduce self-heating free I-V curves consistent with Hspice results, and thus is suitable for SPICE model generation.

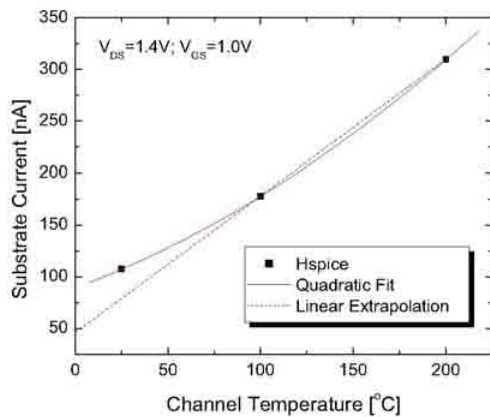


Figure 6 Hspice-simulated substrate current vs. channel temperature.

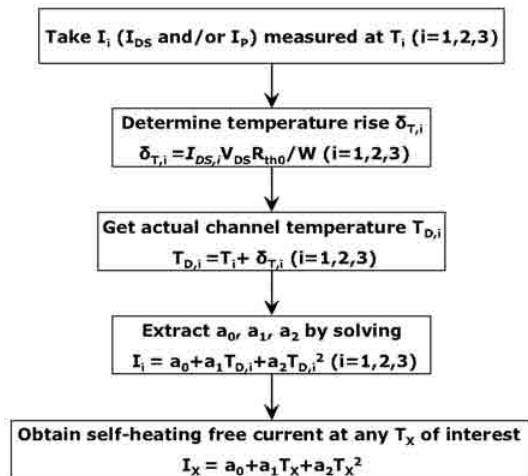


Figure 7 Flow chart of extraction of self-heating free I-V characteristics based on triple-temperature measurement.

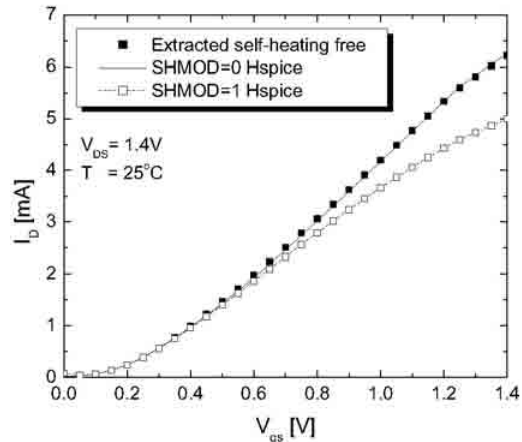


Figure 8 Verification of extraction of self-heating free drain current against Hspice simulations.

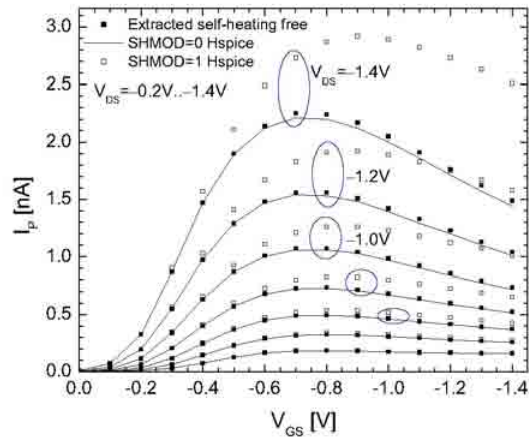


Figure 9 Verification of extraction of self-heating free substrate current against Hspice simulations.

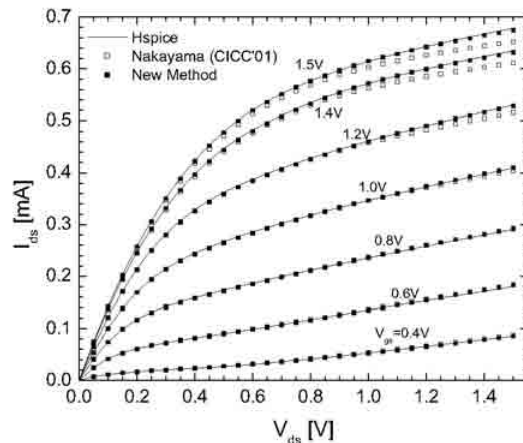


Figure 10 Comparison of extraction results between the new method and the previously reported method [7] against Hspice simulated self-heating free I-V curves.

Table 2 Saturation current ($V_{DD}=1.4V$) comparison between two close PMOS models

Model	$I_{dsat,SH=1}$ [mA]		$I_{dsat,SH=0}/I_{dsat,SH=1}-1$ at 25°C
	25°C	100°C	
#1	3.070	2.920	13.5%
#2	3.070	2.887	18.5%
Diff.	0	1.1%	5 basis points

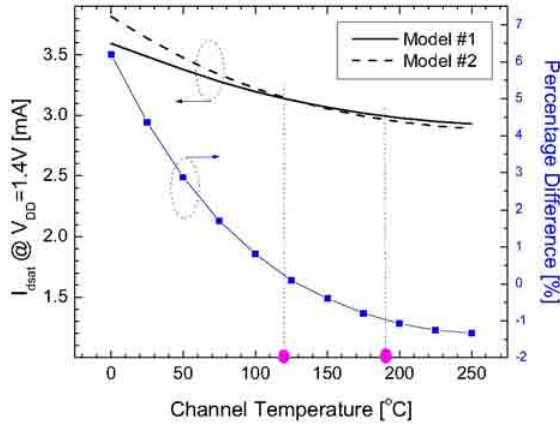


Figure 11 Loss of accuracy in modeling temperature dependences when *directly* fitting regular DC I-V curves for model generation.

III. MODELING IMPLICATIONS

Extraction of self-heating free I-V curves is not only a tool of efficiency that expedites SPICE model generation by reducing the number of modeling iterations, but also may be critical to models' general quality. In Table 2, two slightly different PMOS models that both closely fit raw DC I-V data are compared. Whereas the model-to-data fit is nearly identical at both 25°C and 100°C between the two models, the self-heating-OFF to -ON drive current percentage difference is five basis points apart!

Such a seemingly paradoxical result is caused by the very self-heating effect, as illustrated in Figure 11. The saturation currents at 1.4V DC-measured at 25°C and 100°C, in the case under study, actually correspond to channel temperatures of 120°C and 190°C (points marked on the x-axis in Figure 11), respectively. The slightest model-to-raw-data (or model-to-model) difference (~1%), which in fact occurs in this elevated temperature range and may be well within the model's QA specifications, is amplified very much (~4-6%) toward lower channel temperatures (0°C-100°C) due to the increasing temperature sensitivity. Consequently, two seemingly close models with self-heating mode turned ON produce noticeably different self-heating free I-V characteristics.

The implications for model QA and model-to-data correlation can be acute because of several practical considerations. As NMOS and PMOS SPICE models are often extracted by different individuals, the uncertainty in

models' temperature dependences results in a number of possible model combinations, corner (i.e., extreme) cases of which may, as a result, exhibit considerable cumulative difference in circuit simulations, such as ring-oscillator frequency prediction. Such uncertainty may also be encountered in comparison and benchmarking between various models in multi-threshold voltage technologies as well as between technology nodes. Consequently, availability of self-heating free I-V data may prove to be not only convenient, but also necessary.

IV. CONCLUSION

A generalized approach for extraction of self-heating free I-V curves for SOI MOSFETs is introduced. Examination of linearity or lack thereof in the general current vs. temperature dependence reveals and explains limitations of a previously reported method. A new extraction methodology based on triple-temperature regular DC I-V measurement is proposed that equally applies to both the channel current and the substrate current. The new methodology is verified to be accurate with Hspice simulations, and therefore suitable for SPICE model generation. Finally, it is demonstrated that extraction of self-heating free I-V curves is not only desired, but also required to accurately capture the true temperature dependences in SPICE models.

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REFERENCES

- [1] K. Bernstein and N.J. Rohrer, *SOI circuit design concepts*, Kluwer Academic Publishers, 1999.
- [2] P. Su, S.K.H. Fung, S. Tang, F. Assaderaghi, and C. Hu, "BSIMPD: a partial-depletion SOI MOSFET model for deep-submicron CMOS designs," in Proc. *IEEE CICC*, 2000, pp. 197-200.
- [3] K.A. Jenkins and J.Y.-C. Sun, "Measurement of I-V curves of silicon-on-insulator (SOI) MOSFET's without self-heating," *IEEE EDL*, vol. 16, pp. 145-147, 1995.
- [4] Bill Verzi, *10ns pulsed IV characterization of SOI and high-k transistors*, Agilent, July 2006, http://seminar2.techonline.com/s/agilent_jul2506.
- [5] K.A. Jenkins, J.Y.-C. Sun, and J. Gautier, "Characteristics of SOI FET's under pulsed conditions," *IEEE T-ED*, vol. 44, pp. 1923-1930, 1997.
- [6] P. Su, K. Goto, T. Sugii, and C. Hu, "Self-heating enhanced impact ionization in SOI MOSFETs," in Proc. *IEEE Int. SOI Conf.*, 2001, pp. 31-32.
- [7] H. Nakayama, P. Su, C. Hu, M. Nakamura, H. Komatsu, K. Takeshita, and Y. Komatsu, "Methodology of self-heating free parameter extraction and circuit simulation for SOI CMOS," in Proc. *IEEE CICC*, 2001, pp. 381-384.
- [8] L.T. Su, J.E. Chung, D.A. Antoniadis, K.E. Goodson, and M.I. Flik, "Measurement and modeling of self-heating in SOI NMOSFET's," *IEEE T-ED*, vol. 41, pp. 69-75, 1994.
- [9] N.G. Einspruch and G. Goldenblat, *Advanced MOS device physics - VLSI Electronics Microstructure Science*, vol. 18, p. 225, Academic Press Inc., 1989.
- [10] K.K. Young and J.A. Burns, "Avalanche-induced drain-source breakdown in silicon-on-insulator n-MOSFET's," *IEEE T-ED*, vol. 35, pp. 426-431, 1988.