BSIM-MG: A Versatile Multi-Gate FET Model for Mixed-Signal Design

Mohan V. Dunga[1], Chung-Hsun Lin[1], Darsen D. Lu[1], Weize Xiong[2], C. R. Cleavelin[2], P. Patruno[3], Jiunn-Ren Hwang[4], Fu-Liang Yang[4], Ali M. Niknejad[1] and Chenming Hu[1]
[1]Department of Electrical Engineering and Computer Sciences, University of California, Berkeley, CA 94720 USA
[2]Texas Instruments Inc., SiTD, Dallas, TX USA
[3]SOITECH S.A., Bernin, France
[4]Taiwan Semiconductor Manufacturing Company (TSMC), Hsin-Chu City, Taiwan
Tel: +1-510-643-2638, E-mail: dunga@eecs.berkeley.edu

Abstract

A novel surface-potential based multi-gate FET (MG-FET) compact model has been developed for mixed-signal design applications. For the first time, a MG-FET model captures the effect of finite body doping on the electrical behavior of MG-FETs. A unique field penetration length model has been developed to model the short channel effects in MG-FETs. A multitude of physical effects such as poly-depletion effect and quantum-mechanical effect (QME) have been incorporated. The expressions for terminal currents and charges are ∞–continuous making the model suitable for mixed-signal design. The model has been verified extensively with TCAD and experimental data.

Introduction

The improved short-channel effects (SCE) in multi-gate FETs (MG-FET) due to the stronger electrostatic control from multiple gates makes them an ideal candidate to extend CMOS scaling [1]. To enable efficient MG-FET circuit design, an accurate compact model for MG-FETs is necessary. Most of the modeling efforts [2,3] are limited to undoped or lightly doped body for double-gate FETs (DG-FET).

In this work, a new surface-potential based model is developed which incorporates the effect of finite body doping on the electrical characteristics of the transistor. Starting from a symmetric DG-FET framework, the model is extended to tri-gate FETs using 3-D modeling of SCE. Substrate current model enables modeling of both SOI FinFETs [4,5], and bulk FinFETs [6] (Fig.1). A full fledged compact model BSIM-MG has been developed through incorporation of additional physical effects and leakage currents. The model has been verified against TCAD and experimental MG-FET data for long and short channel lengths. Accurate fitting to drain current (I_d), transconductance (g_m), g_m-efficiency (g_m/I_d) and output conductance (g_{ds}) are observed indicating excellent model efficiency for digital and analog design applications.

Core Model

Fig. 2 shows the schematic of DG-FET. Surface potential (ψ_s) in the finite-doped body is obtained through a solution of the 1-D Poisson's equation using perturbation method [7]. For numerical robustness, an analytical approximation to the resulting transcendental ψ_s equation is implemented with an error limited to few nano-Volts. The calculated ψ_s shows very good agreement with TCAD [8] for a wide range of body doping (Fig. 3). Surface potentials calculated at the source and drain end form the basis of *I-V* and *C-V* models.

I-V model is obtained from drift-diffusion formulation. By using a simplified expression for inversion charge, I_d is derived. The *I-V* model was verified against TCAD for a wide range of body doping (Fig. 4(a)). A unique behavior of lightly doped FinFETs is volume inversion. In subthreshold, band bending in the body is minimal and the electronic potential is nearly independent of body thickness (T_{Si}) (Fig. 4(b)). As a result, the subthreshold leakage is linearly proportional to T_{Si}. Fig. 4(c) shows that the core *I-V* model is able to capture the volume inversion in DG-FETs.

Terminal charges and transcapacitances are derived using current continuity in conjunction with Ward-Dutton charge partition [9]. *C-V* model predicts very accurate transcapacitances over different gate and drain voltages as seen in Fig. 5. At V_{ds}=0, $C_{sg} = C_{dg}$ and $C_{gs} = C_{gd}$ showing the inherent symmetry in the model which is required for certain analog and RF applications. The verification of core *I-V* and *C-V* model with TCAD (Fig. 3 – Fig. 7) is done without the use of any fitting parameters.

Physical Effects

Numerous physical effects such as poly depletion (PDE), QME, SCE and mobility degradation have been added over the core model which can be activated when needed. For example, by switching PDE model ON/OFF, I_d can be obtained for poly-gate/metal gate (Fig. 6). The degree of SCE depends on strength of gate control which is modeled by a characteristic field penetration length ($\lambda = f(T_{ox},T_{si})$). Fig 7(a),(b) compares the threshold voltage (V_{th}) roll-off extracted from the model against 2-D TCAD results without the use of any fitting parameter. Good scalability over T_{ox} and T_{si} down to 30nm channel length (L_g) is clearly visible. For tri-gate FETs, the physical location of maximum I_d leakage is different than DG-FETs (Fig. 7(c)), which causes V_{th} roll-off to increase as fin height (H_{fin}) increases. By making $\lambda = f(T_{ox},T_{si},H_{fin})$, model scalability includes H_{fin} (Fig. 7(d)) extending the DG-FET core model to tri-gate FETs. The SCE model implementation captures V_{th} roll-off, DIBL and subthreshold slope degradation for short channel MG-FETs simultaneously.

Leakage current mechanisms such as gate tunneling and gate-induced drain leakage are also modeled. The substrate current model comprising of impact ionization current and diode current extends the 3-terminal SOI MG-FET model to 4-terminal bulk MG-FET. BSIM-MG can model DG-FETs and tri-gate FETs fabricated on either SOI wafers or bulk Si substrate making it a truly versatile model.

Experimental Verification

The model is verified against two different FinFET technologies – SOI FinFETs and bulk FinFETs. BSIM-MG was able to describe the trends in I_d and its derivatives for long and short channel FETs for both technologies. Important metrics for analog design are g_m, g_{ds} and g_m/I_d. Fitting results to short channel FETs and selected analog design metrics for long channel FETs are shown for SOI FinFETs (Fig. 8) and bulk FinFETs (Fig. 9).

Conclusion

A full-fledged, versatile, surface-potential based multi-gate FET model has been developed with several novel modeling features. The agreement of core model with TCAD without any fitting parameter demonstrates the inherent physical predictivity and scalability of the model. BSIM-MG has also been verified against experimental data (drain current and its derivatives) demonstrating its applicability for mixed signal design.

References

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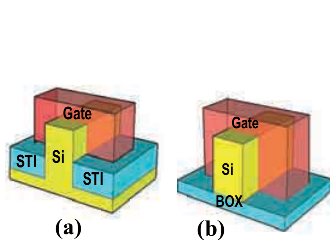


Fig. 1 (a) Bulk MG-FET (b) SOI MG-FET

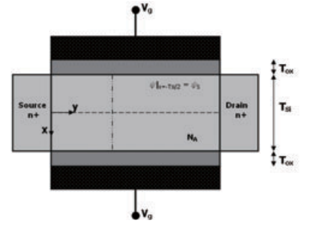
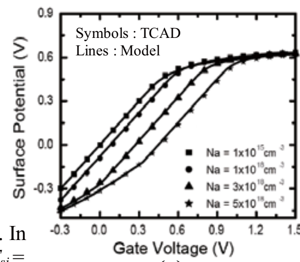


Fig. 2 Schematic of a symmetric DG-FET. In all comparisons with TCAD, T_{ox} = 2nm, T_{si} = 20nm, L_g = 1μm and metal gate with mid-gap work-function has been used unless specified.



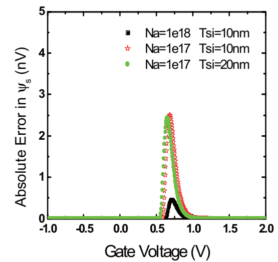


Fig. 3 Surface potential calculation (a) Verification with TCAD. Both partial and full depletion regions are modeled accurately. (b) The analytical approximation for ψ_s is very accurate with error in nV for different N_A and T_{si}.

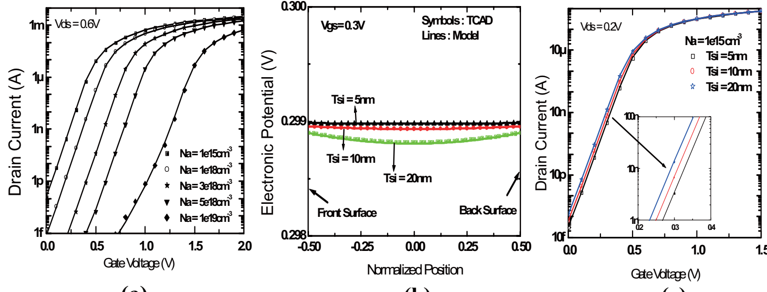


Fig. 4 Drain current model (a) Verification against TCAD for different body doping. I_d is modeled accurately in both partial and full depletion regions. (b) Potential profile in the body between front and back surface in volume inversion. (c) Volume inversion is predicted very well by the I-V model. (Symbols: TCAD, Lines: Model)

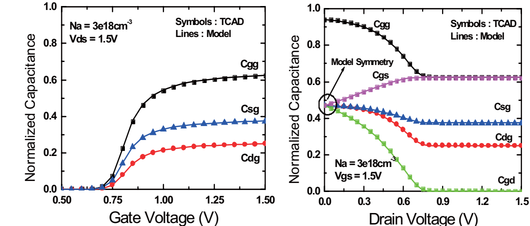


Fig. 5 Model predicts accurate transcapacitances as a function of (a) gate voltage and (b) drain voltage. Model symmetry can be seen at V_{ds}=0 where $C_{dg(gd)} = C_{sg(gs)}$ which is necessary for accurate analog simulations.

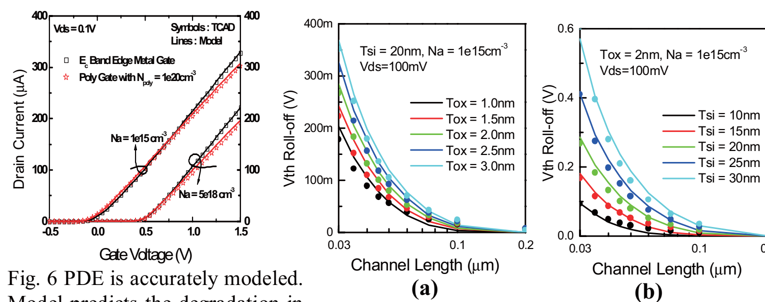


Fig. 6 PDE is accurately modeled. Model predicts the degradation in drain current in strong inversion due to voltage drop in poly-gate.

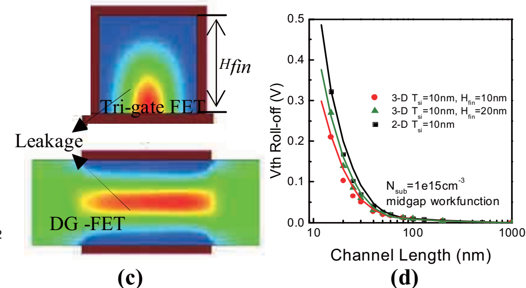


Fig. 7 Scalability of SCE model has been demonstrated through threshold voltage roll-off for different (a) oxide thickness and (b) body thickness for DG-FETs. (c) Leakage current path is different in tri-gate FETs due to 3D effects. (d) SCE model also exhibits fin height scalability for tri-gate FETs (Symbols: TCAD, Lines: Model)

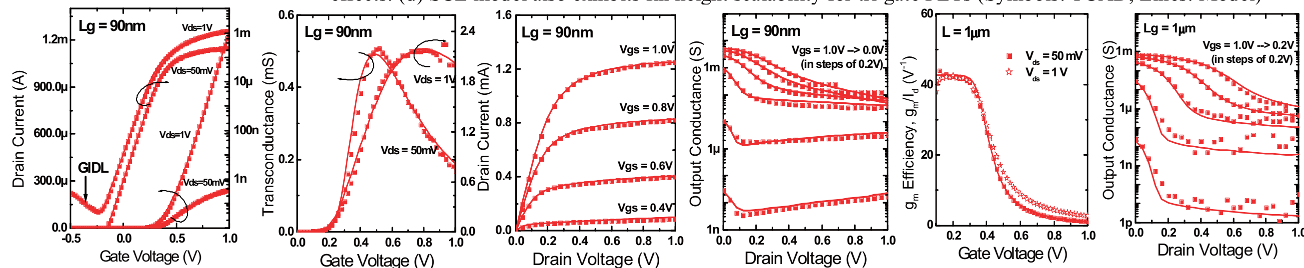


Fig. 8 SOI FinFETs were fabricated on lightly doped 60nm thick film with 2nm SiO_2 dielectric and strained TiSiN gate[4] which strains the channel to enhance carrier moblity. Measured devices have 20 parallel fins with T_{Si} = 22nm. Short channel (L_g = 90nm) fitting to measured I_d, g_m and g_{ds} and long channel (L_g = 1μm) g_m/I_d and g_{ds} are shown. (Symbols: measured data, Lines: model). GIDL leakage is also modeled as shown in I_d-V_g.

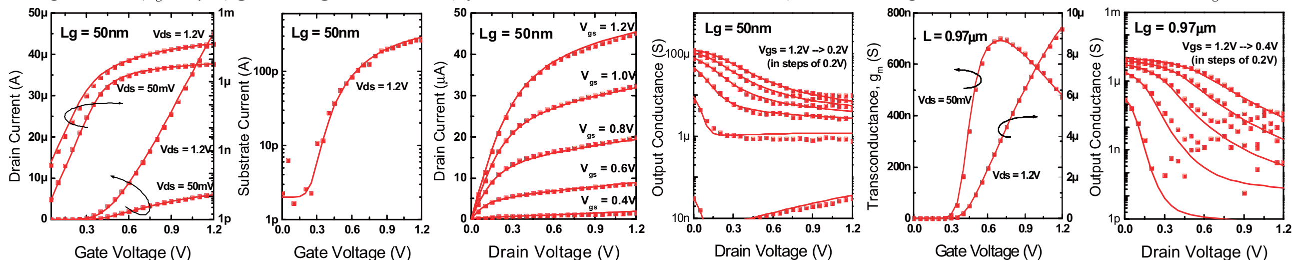


Fig. 9 Bulk FinFETs with moderate doping were fabricated with a TiN gate. Measured devices have T_{Si} = 25nm and EOT = 1.95nm. Short channel (L_g =50nm) fitting to measured I_d, I_{sub} and g_{ds} and long channel (L_g = 0.97μm) g_m and g_{ds} are shown. (Symbols: measured data, Lines: model) The model is able to describe both bulk FinFETs and SOI FinFETs.