An *A Priori* Hysteresis Modeling Methodology for Improved Efficiency and Model Accuracy in Advanced PD SOI Technologies

Qiang Chen, Jung-Suk Goo, Niraj Subba, Xiaowen Cai, Judy X. An, Tran Ly,
Zhi-Yuan Wu, Sushant Suryagandh, Ciby Thuruthiyil, Martin Radwin, Luis Zamudio,
James Yonemura, Farzin Assad, Mario M. Pelella, and Ali B. Icel

Advanced Micro Devices
One AMD Place, MS 79, Sunnyvale CA 94088-3453, USA, qiang.chen@amd.com

ABSTRACT

An *a priori* hysteresis modeling methodology in partially depleted (PD) silicon-on-insulator (SOI) technologies is proposed that constitutes an essential part of an improved compact model extraction flow. By focusing on the parasitic currents, the capacitance network, the body effect, and fine-tuning the diode characteristics especially, the proposed methodology aims to closely capture the voltage and temperature dependences of hysteresis well before the full-fledged MOSFET model extraction begins. The resulting benefits, such as improved model extraction efficiency, relatively high fidelity to hardware data, and improved model accuracy, are demonstrated on a state-of-the-art 90 nm PD SOI technology.

Keywords: silicon-on-insulator (soi), partially depleted (pd), hysteresis (history effect), compact modeling

1 INTRODUCTION

Hysteresis (the history effect) in partially depleted (PD) floating-body (FB) silicon-on-insulator (SOI) circuits [1], namely, the dependence of the propagation delay of a logic gate on its pre-switch state, is important for accurate circuit timing and is critical to predict for proper circuit design and functionality. It is a delicate function of complex interactions among the following three components: 1) parasitic currents, including the gate tunneling current, the source/drain junction diode current, the parasitic bipolar transistor (BJT) current, and the impact ionization (II) current; 2) the body/gate/junction capacitance network, and 3) the body effect defined as threshold voltage's dependence on the body potential [2]. The parasitic currents and the capacitance network determine the potential of a PD SOI device's floating body through the DC current balance and the AC capacitive coupling, respectively, while the body effect relates the body potential to the threshold voltage and subsequently the switch delay. As the silicon body thickness scales, measurement and characterization of parasitic currents become increasingly challenging [3]. Hysteresis modeling is further complicated for target-based (i.e., evaluation-level) model extraction where only limited device information is available because of technology immaturity and the forward-looking nature of time-to-market driven microprocessor designs.

2 A PRIORI HYSTERESIS MODELING METHODOLOGY

To address these issues, it was proposed [3] that three characteristics, the gate-to-body tunneling current (I_{gb}), the gate-to-body capacitance (C_b), and the body effect be used to adjust hysteresis. The body effect, however, is known in practice to have noticeable impact on MOSFET DC characteristics, causing considerable re-tweaking of the entire device model. Meanwhile, the quantitative component-based analysis of hysteresis modeling indicates [4] that I_{gb} might need to be altered significantly (often by an order of magnitude) to meet expected hysteresis levels. On the other hand, for a given technology, as it matures toward performance goals, the body effect and I_{gb}, which mainly depend on the vertical structure of the transistor, may incur only limited changes, thus making it unwarranted to dramatically adjust their behavior in compact models.

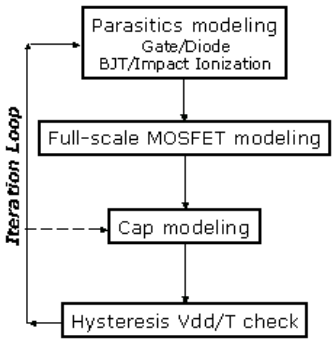

Figure 1 Diagram of the conventional model extraction flow with hysteresis modeling at the end.

The hysteresis adjustment discussed in [3] deals with a single supply voltage (V_{dd}) at a given temperature (T). Accurate hysteresis modeling at the nominal V_{dd} and T, however, does not guarantee an adequate fit for other operating conditions. A vastly extended hysteresis fitting strategy taking into account both V_{dd} and T dependences is provided in [4], using a complete combination of parasitic currents, capacitances, and the body effect. A common feature of both approaches is that the hysteresis modeling is checked after the MOSFET model is extracted, and hysteresis adjustment is carried out along with the comprehensive MOSFET model refinement during each

iteration, as shown in Figure 1. While the addition of the hysteresis-level evaluation step towards the end brings minimal disruption to the overall modeling flow, it causes several implementation issues. As the device technology advances, the parasitic currents play an increasingly large role in comparison to the MOSFET currents. Adjustment of parasitic currents and the body effect for the sake of the hysteresis alignment generally leads to noticeable changes in the MOSFET characteristics, as illustrated in Figure 2. Consequently, the MOSFET/hysteresis iteration loop becomes extremely time and labor consuming. In addition, significant deviation from the measured data for parasitic currents and a sub-optimum hysteresis alignment may still result because of resource limitations typical in industry.

Adjustment of MOSFET characteristics, on the other hand, has very limited impact on parasitic currents modeling (Figure 2). And as empirically observed, MOSFET characteristics do not assert strong influence on hysteresis either. It is vividly exemplified in Figure 3, which shows the absolute change of an inverter's hysteresis (H) in response to 10% increase of model parameters *ndiode* (the diode ideality factor) or $u0$ (the low-field mobility) in the PMOS model. Taking advantage of both observations, a new model extraction flow with *a priori* hysteresis modeling can be proposed, as shown in Figure 4. The essence of the new flow is to correctly model V_{dd} and T dependences of hysteresis first, i.e., *a priori* to the full-blown MOSFET model extraction. The reduced hysteresis iteration removes from the loop the unproductive intermediate MOSFET fitting effort for improved overall efficiency.

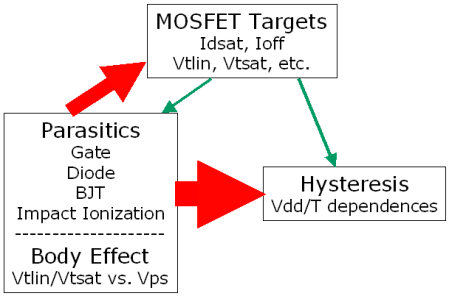

Figure 2 Interaction among DC, nonFET, and hysteresis characteristics. The arrow width corresponds to the degree of impact.

A second distinct feature of the new methodology is that only diode characteristics are to be exploited in the hysteresis adjustment loop. The diode characteristics are chosen mainly for three reasons. First of all, it is their unique role in the physical mechanisms of hysteresis (Figure 5), where the reverse- and forward-bias diode characteristics determine the body potential in the first switch, and the forward-bias diode characteristics, along with the gate current, determines the *initial* body potential in the second switch [4]. Secondly, they are the dominant factor for hysteresis' V_{dd} and T dependences [4], and subtle changes of I-V *slopes* in appropriate bias regions, rather than significant changes in *absolute current levels*, can accomplish desired hysteresis behavior over different V_{dd} and T. Lastly, diode currents can be measured accurately [3] so that any deviation from real data needed for the hysteresis alignment can be clearly understood and closely monitored.

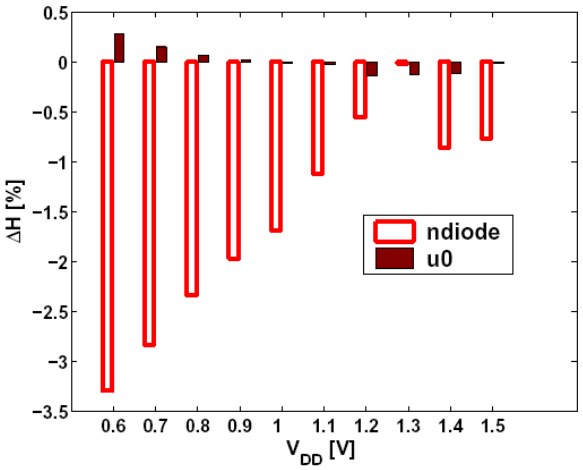

Figure 3 *Absolute* change of hysteresis in response to 10% increase of individual model parameters such as *nidode* (the diode ideality factor) and $u0$ (the low-filed mobility).

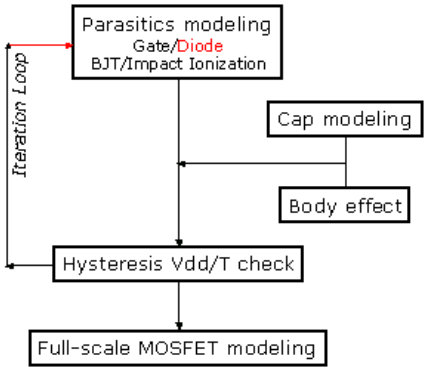

Figure 4 Diagram of the proposed model extraction flow.

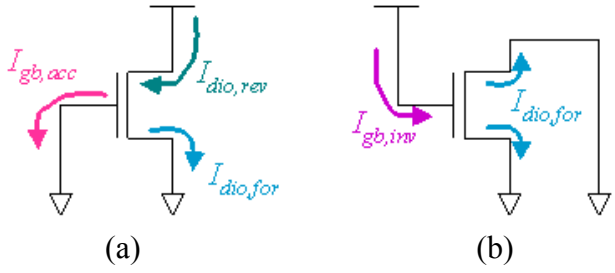

Figure 5 Illustration of component currents determining the *initial* body potentials in (a) the first and (b) second switches in PD SOI. The gate-body current in accumulation, $I_{gb,acc}$, typically can be ignored [4].

Use of diode characteristics alone to adjust hysteresis significantly reduces the number of involved model parameters. It makes feasible automatic optimization of V_{dd}

and T dependences of hysteresis, a complex task where the running time usually exponentially explodes with each added model parameter.

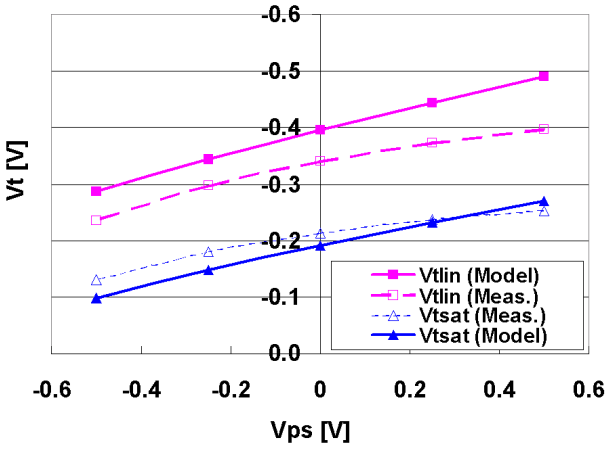

Figure 6 Illustration of the body effect modeling in a target-based PMOS model: the threshold voltage vs. the body potential V_{ps}.

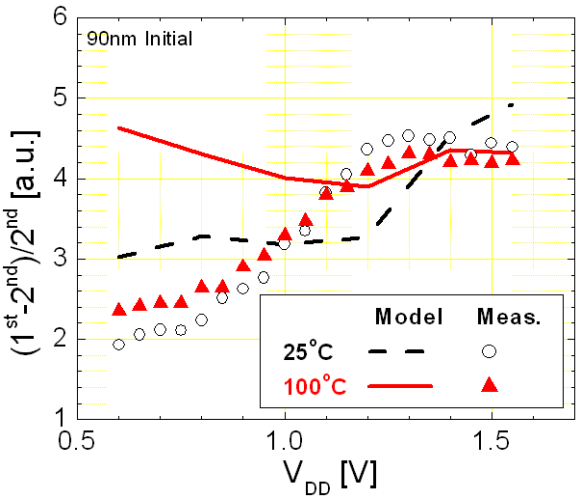

Figure 7 The initial hysteresis comparison: model vs. measured data. Hysteresis values are normalized.

3 FIELD IMPLEMENTATION

The novel, a priori hysteresis modeling methodology is implemented for a target-based model extraction on a state-of-the-art 90 nm PD SOI technology. BSIMPD SOI MOSFET models are used [5]. In both measurement and circuit simulations, hysteresis is defined in a chain of successive inverter stages as follows

$$H = \left(t_{pd,1} - t_{pd,2}\right) / t_{pd,2},$$

where $t_{pd,1}$ and $t_{pd,2}$ are the propagation delays of the first- and second-switch, respectively.

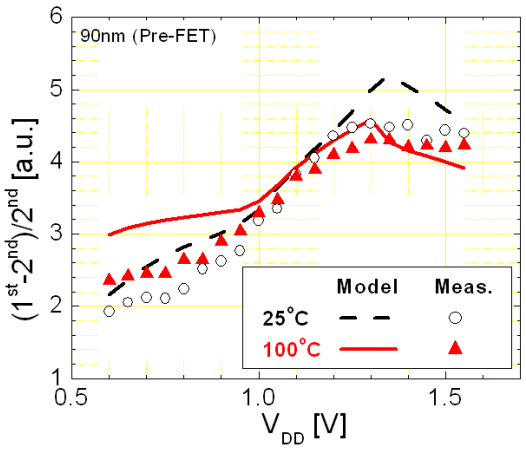

Figure 8 A priori hysteresis-modeling results, i.e., prior to the full-blown MOSFET model extraction, compared to measured data.

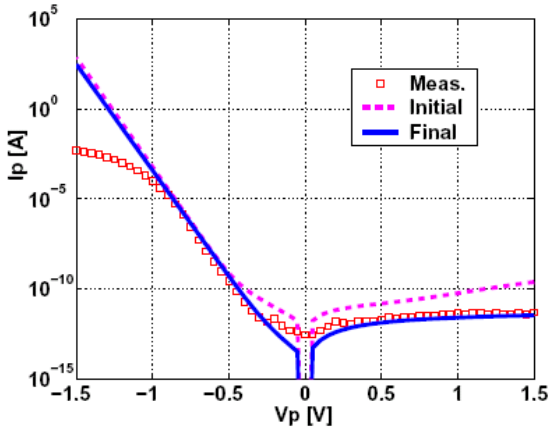

Figure 9 Illustration of the diode characteristics modeling: the initial and final fit vs. measured data.

Following the new methodology, the capacitances, the body effect, and the parasitic currents (except for the diode characteristics) are checked and fit closely to measured data, an example of which is shown in Figure 6. It is worth pointing out in Figure 6 that the body effect, which is the threshold voltage (V_t) vs. the body voltage (V_{ps}) slope, is well captured in the forward bias region (i.e. with negative body voltages for PMOS), and the difference in absolute V_t values between the model and measurement is a result of the model being fit to targets rather than the hardware data. In the reverse bias region (with positive body voltages), the measured V_t shows a trend of saturation with increasing V_{ps}, which is physically caused by the full depletion of the body, while the model fails to mimic such a behavior because of BSIM PD SOI's deficiency. The degraded fitting quality in this region, however, has few ramifications since the *pre-switch* body potential generally does not fall into the region. Overall, the model-predicted V_{dd} and T dependences of hysteresis significantly differ from measurement (Figure 7), greatly overestimating hysteresis at low V_{dd}'s. It emphasizes the inadequacy of using a single V_{dd}/T point for hysteresis adjustment.

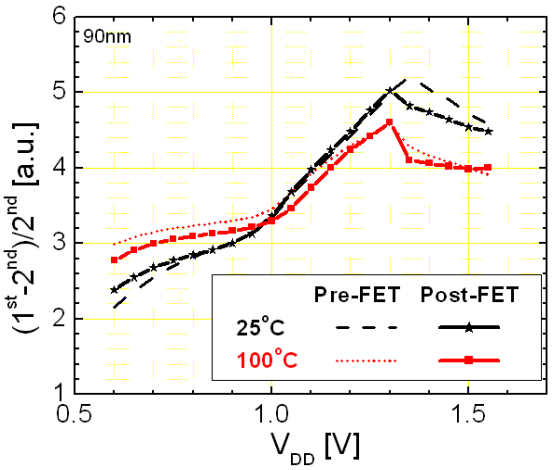

Figure 10 Comparison of the model's hysteresis behavior before and after the full-fledged MOSFET modeling.

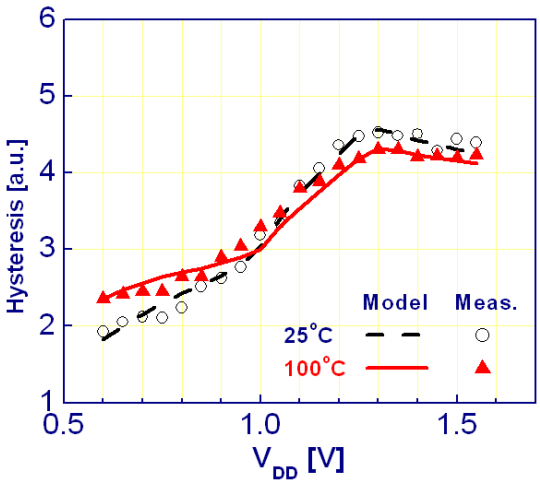

Figure 11 Automatic hysteresis optimization results with diode model parameters only using a software package.

The initial close match between the model and the measurement at high V_{dd}'s (Figure 7) suggests that the ensuing hysteresis adjustment focus on the diode current in two regions only, namely, the forward low bias and the reverse bias. The iteration starts with the room-temperature hysteresis behavior using temperature-independent model parameters, followed by modeling the hysteresis behavior at elevated temperature using temperature parameters alone. In a few iterations, a reasonably good match of hysteresis across all V_{dd}'s and T's is achieved (Figure 8). A comparison of the initial and final fit of the diode characteristics to measured data is given in Figure 9. While the majority of the diode model adjustment is based on measured data, the deviation of the model from the measurement in low biases is both needed for hysteresis fit and justifiable by the fact that the measurement itself may be marred by noise at extremely low current levels.

With the V_{dd} and T trends of hysteresis closely captured *a priori*, the full-blown MOSFET modeling is carried out. It is made sure that only MOSFET model parameters are used in this stage so that parasitic characteristics remain unaltered. Moreover, the body effect is kept under close watch to avoid unintended modification with respect to the a priori (pre-FET) fit. The hysteresis behavior predicted by the resulting complete device models (post-FET) that meet all MOSFET targets is compared to that of the pre-FET models in Figure 10. Despite the large number of model parameters that were adjusted during the full-blown MOSFET modeling (41 and 18 for NMOS and PMOS, respectively), the hysteresis fit changes only marginally, well preserving the V_{dd} and T trends.

Aside from the manual hysteresis adjustment toward the a priori models, automatic hysteresis optimization is experimented using a software package, exploiting exactly the same strategy, i.e., by using diode parameters and their temperature dependent ones exclusively. It has produced very good alignment between the model and measured data for hysteresis' V_{dd} and T dependences (Figure 11), lending a promising prospect to further improvement in both model extraction efficiency and model accuracy.

4 CONCLUSIONS

By taking advantage of the asymmetric nature of interactions among hysteresis, parasitic, and MOSFET characteristics, an *a priori* hysteresis modeling methodology has been proposed as an essential part of an improved model extraction flow for advanced PD SOI technologies. It has been successfully implemented on a state-of-the-art 90 nm technology demonstrating projected benefits, such as minimum deviation of parasitic characteristics from hardware data, improved overall model extraction efficiency, improved model accuracy for hysteresis over a wide range of supply voltages and temperatures, and efficient implementation of automatic hysteresis optimization.

ACKNOWLEDGMENT

The authors would like to thank Mr. Nick Kepler of Advanced Micro Devices for promoting and supporting this project.

REFERENCES

[1] M. M. Pelella, et al., "Analysis and control of hysteresis in PD/SOI CMOS," *Proc. IEEE IEDM*, 1999, pp.831-834.

[2] K. Bernstein and N. J. Rohrer, "SOI circuit design concepts," *Kluwer Academic Publishers*, 2000.

[3] M. H. Na, et al., "Predicting the SOI history effect using compact models," *Proc. Int. Conf. Modeling and Simulation of Microsystems*, 2004, vol.2, pp.183-186.

[4] J. S. Goo, et al., "History-effect-conscious SPICE model extraction for PD-SOI technology," *Proc. IEEE Int. SOI Conf.*, 2004, pp.156-158.

[5] BSIMPD User's Manual, University of California, Berkeley.