UNIVERSITY OF CALIFORNIA

Los Angeles

Extraction of SPICE Parameters for CMOS at 300 K and 77 K

A thesis submitted in partial satisfaction of the requirements for the degree Master of Science in Electrical Engineering

by

Clifford Y.C. Hwang

1994

© Copyright by

Clifford Y.C. Hwang

1994

The thesis of Clifford Y.C. Hwang is approved.

Dee-Son Pan

Ming Wu

Jason C.S. Woo, Committee Chair

University of California, Los Angeles

1994

To My Father–Thanks for Your Support

Contents

1 Introduction **1**

1.1 Motivation 1

1.2 Organization 3

2 Extraction Technique and Results at 300 K **5**

2.1 Introduction 5

2.2 Extraction Recipe 6

2.2.1 Device Inventory and Measurements 6

2.2.2 Effective Channel Length and Source/Drain Resistance 8

2.2.3 Effective Channel Width 8

2.2.4 Threshold Voltage 10

2.2.5 Effective Mobility 17

2.3 PMOS Fit 18

2.3.1 I_{ds} vs. V_{gs} At Low V_{ds} 19

2.3.2 I_{ds} vs. V_{ds} With V_{gs} Varied 21

2.3.3 I_{ds} vs. V_{gs} With V_{sb} Varied 25

2.3.4 Short Channel Width Fit 27

2.4 NMOS Fit 29

2.5 Ring Oscillator Fit 33

2.6 Conclusion 35

3 Extraction Results at 77 K **39**

3.1 Introduction 39

3.2 Extraction Problems at 77 K 40

3.2.1 Effective Channel Dimensions and Source/Drain Resistance . . 40

3.2.2 Threshold Voltage Fluctuations 40

3.3 I-V Fit at 77 K 44

3.3.1 I_{ds} vs. V_{gs} Curves 44

3.3.2 I_{ds} vs. V_{ds} Curves 46

3.3.3 Ring Oscillator Performance 49

3.4 Comparison with 300 K HSPICE Parameters 52

3.5 Conclusion 55

4 Extraction of the Gate Dependent Source/Drain Resistance and Effective Channel Length **56**

4.1 Introduction 56

4.2 Extraction Technique 58

4.3 Simulation Results and Discussion 63

4.4 Conclusion 70

5 Conclusion **73**

5.1 Summary 73

5.2 Suggestions for Future Work 74

List of Figures

2.1 Total Resistance versus Drawn Channel Length for PMOS devices at 300 K. . . . 9

2.2 Total Conductance versus Drawn Channel Width for PMOS Devices at 300 K. . . . 10

2.3 Threshold Voltage versus Drawn Channel Length for PMOS Devices at 300 K. . . . 12

2.4 Threshold Voltage versus Drain Bias for a 25 x 1 μm PMOS Device at 300 K. . . . 14

2.5 Threshold Voltage versus $(PHI + V_{sb})^{1/2} - (PHI)^{1/2}$ for a 25 x 25 μm PMOS Device at 300 K. . . . 16

2.6 Effective Mobility versus Gate Bias for a 25 x 25 μm PMOS Device at 300 K. . . . 18

2.7 I_{ds}-V_{gs} Curves (linear scale) for PMOS Devices at 300 K. . . . 20

2.8 I_{ds}-V_{gs} Curves (logarithmic scale) for PMOS Devices at 300 K. . . . 21

2.9 I_{ds}-V_{ds} curve for a 25 x 25 μm PMOS Device at 300 K. . . . 22

2.10 I_{ds}-V_{ds} Curve for a 25 x 3 μm PMOS Device at 300 K. . . . 23

2.11 I_{ds}-V_{ds} Curve for a 25 x 1 μm PMOS Device at 300 K. . . . 23

2.12 I_{ds}-V_{gs} Curve with Variable V_{ds} for a 25 x 25 μm PMOS Device at 300 K. 24
2.13 I_{ds}-V_{gs} Curve with Variable V_{sb} for a 25 x 25 μm PMOS Device at 300 K. 25
2.14 I_{ds}-V_{gs} Curve with Variable V_{sb} for a 25 x 3 μm PMOS Device at 300 K. 26
2.15 I_{ds}-V_{gs} Curve with Variable V_{sb} for a 25 x 1 μm PMOS Device at 300 K. 26
2.16 I_{ds}-V_{gs} Curves for a 10 x 6 μm and a 6 x 1 μm PMOS Device at 300 K. 28
2.17 I_{ds}-V_{ds} Curve for a 10 x 6 μm PMOS Device at 300 K. 28
2.18 I_{ds}-V_{ds} Curve for a 6 x 2 μm PMOS Device at 300 K. 29
2.19 I_{ds}-V_{gs} Curves for NMOS Devices at 300 K. 30
2.20 I_{ds}-V_{ds} Curve for a 25 x 3 μm NMOS Device at 300 K. 31
2.21 I_{ds}-V_{ds} Curve for a 25 x 2 μm NMOS Device at 300 K. 32
2.22 Effective Mobility versus Gate Bias for a 25 x 25 μm NMOS device at 300 K. 32
2.23 I_{ds}-V_{ds} Curve for a 6 x 2 μm NMOS Device at 300 K. 33
2.24 I_{ds}-V_{ds} Curve for a 6 x 1 μm NMOS Device at 300 K. 34
2.25 Propagation Delay per Stage versus Power Supply Voltage of Ring Oscillators at 300 K. 36

3.1 Total Resistance versus Drawn Channel Length for NMOS Devices at 77 K. 41
3.2 Threshold Voltage versus Drawn Channel Length for NMOS devices at 77 K. 42

3.3 I_{ds}-V_{gs} Curves (linear scale) for NMOS Devices at 77 K. 44

3.4 I_{ds}-V_{gs} Curves (logarithmic scale) for NMOS Devices at 77 K. 45

3.5 I_{ds}-V_{ds} Curve for a 25 x 25 μm NMOS Device at 77 K. 46

3.6 I_{ds}-V_{ds} Curve for a 25 x 3 μm NMOS Device at 77 K. 47

3.7 I_{ds}-V_{ds} Curve for a 25 x 1.5 μm NMOS Device at 77 K. 47

3.8 Effective Mobility versus Gate Bias for a 25 x 25 μm NMOS device at 77 K. 48

3.9 I_{ds}-V_{ds} Curve for a 6 x 6 μm NMOS Device at 77 K. 49

3.10 Propagation Delay per Stage versus Power Supply Voltage of Ring Oscillators at 77 K. 51

4.1 Total Resistance versus Drawn Channel Length for Simulated NMOS Devices at 300 K. 59

4.2 Total Resistance versus Drawn Channel Length for Simulated NMOS Devices at 77 K. 60

4.3 R_{locus} and R_{sd} versus $V_{gs} - V_{th}$ for an Abrupt, Uniform Source/Drain Profile at 300 K. 63

4.4 ΔL_{locus} and ΔL versus $V_{gs} - V_{th}$ for an Abrupt, Uniform Source/Drain Profile at 300 K. 64

4.5 R_{locus} and R_{sd} versus $\mu_{eff}(V_{gs} - V_{th})$ for a Gaussian Source/Drain Profile at 300 K. 66

4.6 ΔL_{locus} and ΔL versus $\mu_{eff}(V_{gs} - V_{th})$ for a Gaussian Source/Drain Profile at 300 K. 67

4.7 R_{locus} and R_{sd} versus $\mu_{eff}(V_{gs} - V_{th})$ for a Gaussian Source/Drain Profile at 77 K. 68

4.8 ΔL_{locus} and ΔL versus $\mu_{eff}(V_{gs} - V_{th})$ for a Gaussian Source/Drain Profile at 77 K. 69

4.9 Measured R_{locus} and ΔL_{locus} versus $\mu_{eff}(V_{gs} - V_{th})$ at 300 K for the HP-MOSIS Devices of Chapter 2. 70

4.10 Measured R_{locus} and ΔL_{locus} versus $\mu_{eff}(V_{gs} - V_{th})$ at 77 K for the HP-MOSIS Devices of Chapter 3. 71

List of Tables

2.1 Ring Oscillators Measured at T = 300 K 34

2.2 Extraction Procedure for Obtaining Level 6 HSPICE Parameters. . . 37

3.1 Ring Oscillators Measured at T = 77 K 50

3.2 Level 6 HSPICE Parameters at 300 K and 77 K. 53

Acknowledgements

I wish to express my sincere thanks to Professors Dee-Son Pan, Ming Wu, and my advisor, Jason C.S. Woo, for their assistance in reviewing this manuscript.

I would like to especially thank Professor Woo for his help in guiding and shaping my research here at UCLA as a Master's student.

This work is in part supported by Superconductor Technologies Incorporated. Thanks to Dr. Bob Hammond and Dr. Ching Jeng for both the financial and technical support.

I wish to acknowledge my friends and colleagues in the Solid-State Electronics lab: Dr. Tsung-Chia Kuo, Dr. Neal Kistler, Tommy Hsiao, Janet Wang, Chi-Hung Lin, Vincent Chen, Dr. Miryeong Song, and Baohong Chen. Thanks for all of your help.

ABSTRACT OF THE THESIS

Extraction of SPICE Parameters for CMOS

at 300 K and 77 K

by

Clifford Y.C. Hwang

Master of Science in Electrical Engineering

University of California, Los Angeles, 1994

Professor Jason C.S. Woo, Chair

In recent years, there has been growing interest in the operation of MOS transistors at temperatures below 300 K. Numerous improvements in performance occur when a device is cooled down to 77 K. However, in order to fully realize the advantages of low temperature operation, overall circuit performance must be determined. Circuit simulation programs such as SPICE can be used to achieve this goal. However, it is often unclear how to extract the necessary modeling parameters from a device so that SPICE can be used.

In this thesis, a step-by-step procedure for extracting the necessary parameters for the level 6 model in HSPICE is presented. The principles presented here can be applied towards any SPICE model. Good agreement between simulation and measurement results are shown at 300 K and 77 K. By studying and comparing the extracted parameters, the improvements and tradeoffs between 300 K and 77 K operation can be clearly seen.

Difficulties in extracting the low temperature SPICE parameters are presented. One significant problem is obtaining the effective channel length and parasitic source/drain resistance. A negative resistance and an effective channel length longer than the drawn channel length are almost always obtained at low temperatures. To resolve this problem, an improved extraction technique is presented which assumes that both the effective channel length and source/drain resistance vary with the gate bias. Positive, meaningful results are obtained at 77 K and at 300 K.

Chapter 1

Introduction

As the minimum dimensions of MOS transistors drop into the submicrometer range, packing density continues to increase, but device performance has improved only marginally. Low temperature operation has gained considerable interest recently as a possible way of further enhancing device characteristics. Advantages of 77 K operation include higher mobility, steeper subthreshold slopes (which allow for lower threshold voltages and power supplies), elimination of latchup, higher metal conductivity, and lower junction capacitances [1]-[5]. Circuits running at 77 K can be up to three times faster than at 300 K [4]. This makes low temperature electronics an attractive candidate for future ULSI circuits.

1.1 Motivation

If low temperature electronics is to become a reality, circuit simulation programs, such as SPICE [6], will be needed as a design tool. But in order to use these programs, parameters which are used to model the MOSFET's behavior need to be

obtained. In most circuit simulators, several different models are available. For example, in HSPICE [7], there are over thirty different models, which vary in complexity and in the number of parameters. The BSIM models [8]-[9] are commonly used and produce good agreement with the measurement results. However, due to the pheonomenological nature of the model, it is difficult to get any physical meaning from most of the parameters.

Devices optimized for operation at 300 K will not be optimized at 77 K. Hence, it is important to note what significant changes will occur in a device designed for 300 K operation when it is cooled down to 77 K. By using a semi-empircal model instead of a matrix/table based model such as BSIM, the changes in device behavior and performance at 300 K and 77 K can be more clearly seen, and modifications to the processing parameters can be made so that MOSFETs will run at peak performance at 77 K. Using a model with purely physical parameters will not produce as accurate of a fit with the measurements.

Extracting the parameters for a particular technology of MOSFETs is no easy task in of itself. For models such as BSIM, many devices need to be measured and statistical averages are taken. Often computers perform the statistics and determine the model parameters. Even in a semi-empircal model, the number of parameters can be quite large, and it is often difficult to know where or how to start. In this thesis, a recipe for extracting the modeling parameters for the HSPICE Level 6 MOSFET is presented. This recipe can be extended towards obtaining the modeling parameters for any SPICE model. Good agreement in both the I-V characteristics and circuit behavior will be shown for devices measured at 300 K and 77 K. By

using this semi-empirical model, the physical changes in the transistor's behavior between 300 K and 77 K can be noted.

One of the more difficult modeling issues at 77 K is determining the source/drain resistance and effective channel length. If standard extraction techniques [10] are applied on a set of devices at 77 K, a negative resistance and an effective channel length longer than the drawn channel length are almost always obtained. To resolve this problem, a new extraction technique is presented in which both the source/drain resistance and the effective channel length are functions of gate bias. Simulation results demonstrate the usefulness of this technique. It can be seen that the gate-bias dependence of both parameters is inherent to MOSFETs, both LDD and non-LDD.

1.2 Organization

This thesis is presented as follows. In Chapter 2, a step-by-step procedure is presented for extracting the Level 6 HSPICE parameters. This technique is demonstrated on a set of devices measured at 300 K, resulting in a good fit, both in I-V characteristics and in circuit performance.

In Chapter 3, results are shown for the same devices measured at 77 K. Variations in the measurement data and problems with the fitting at low temperature are discussed. Changes in device performance are noted by comparing the model parameters at 77 K and 300 K.

Chapter 4 presents a new technique for extracting the gate dependent source/drain resistance and the effective channel length. Good results are seen from simulations at both 300 K and 77 K.

Finally, in Chapter 5, the results of this thesis are summarized and suggestions for future work are given.

Chapter 2

Extraction Technique and Results at 300 K

2.1 Introduction

In order to gain an understanding of how well a device works, one can look at the parameters used to model it in a circuit simulation program. This chapter presents the steps used to obtain a Level 6 HSPICE fit to measurements of MOSFETs at 300 K. The procedure is demonstrated in detail for PMOS devices as an example. The source/drain resistance along with the effective channel length and channel width are extracted first, followed by thorough modeling of the threshold voltage and mobility. Three sets of I-V curves will be fitted for a variety of different channel lengths and widths: I_{ds} vs. V_{gs} at low drain bias, I_{ds} vs. V_{ds} for various gate biases, and I_{ds} vs. V_{gs} for various substrate biases at low drain bias. During the actual fitting of the simulation data to the measurements, some adjustment of the originally extracted parameters will be necessary, and additional parameters will be determined.

Results of the 300 K fit for NMOS devices are also shown, along with some of the challenges involved in the fitting. Finally, ring oscillator data is used to verify that circuit simulation using these parameters is feasible.

2.2 Extraction Recipe

2.2.1 Device Inventory and Measurements

Before any fitting can take place, measurements need to be performed on a series of transistors. The choice of devices is important. A list of necessary devices is given below, in order of importance:

- At least three transistors with long, constant channel width and varying channel lengths. These will be used to extract the source/drain resistance and the effective channel length. In addition, these devices will determine how the threshold voltage rolls off with channel length.
- One transistor with long channel width and long channel length. This will be used to extract the mobility and the parameters which model back-gate effects.
- One transistor with long channel width and short channel length. This will be used to model the threshold voltage dependence on drain bias.
- At least three transistors with long, constant channel length and varying channel width. These will be used to extract the effective channel width.
- Transistors that are at or near the "target" dimensions which will be used in circuits.

- Structures which can measure parasitic capacitances. HSPICE will automatically calculate most parasitics based on the extracted parameters if they are not given, but it is better to get a real value for the parasitics.

- Simple circuits, such as ring oscillators or inverters, which can be used to verify that the extracted parameters are correct.

The devices used here to extract the 300 K parameters are NMOS and PMOS transistors manufactured through MOSIS using a 0.8 μm process at Hewlett-Packard. Gate oxide thickness is 200Å. Using a probe station connected to a computerized HP 4142B setup, the following current-voltage measurements were performed on single PMOS transistors of dimensions (in μm): 25 x 25, 25 x 6, 25 x 3, 25 x 2, 25 x 1.5, 25 x 1, 10 x 10, 10 x 6, 6 x 6, 6 x 2, and 6 x 1.

- I_{ds} vs. V_{gs} with V_{ds} = -0.1 volts. V_{gs} was swept from 0 to -5 volts.

- I_{ds} vs. V_{gs} with V_{ds} = -0.5, -1.5, -2.5, -3.5, and -4.5 volts. V_{gs} was swept from 0 to -5 volts for each V_{ds}.

- I_{ds} vs. V_{ds} with V_{gs} = 0, -1, -2, -3, -4, and -5 volts. V_{ds} was swept from 0 to -5 volts for each V_{gs}.

- I_{ds} vs. V_{gs} with V_{sb} = 1, 2, 3, 4, and 5 volts. V_{ds} was swept from 0 to -5 volts for each V_{gs}.

For measurements with NMOS devices, all of the voltage polarities should be reversed.

2.2.2 Effective Channel Length and Source/Drain Resistance

The effective channel length and source/drain resistance should be extracted first. Figure 2.1 shows a plot of total resistance ($= V_{ds}/I_{ds}$) versus drawn channel length for different gate biases above the threshold voltage [11]. Threshold voltage is defined as the gate voltage when the drain current reaches 10 nA * W/L. The I_{ds}-V_{gs} curves at low drain bias for transistors with long, constant channel widths and varying channel lengths are used to generate the data. The intersection of the lines of constant $V_{gs} - V_{th}$ gives the total source and drain resistance (y-coordinate, R_{sd}), and ΔL (x-coordinate), which is the difference between the drawn channel length and the effective channel length. This difference results primarily from the lateral diffusion of the heavily doped source/drain areas into the channel region.

It should be noted that the intersection of the lines is not one single point, indicating that there is a significant margin for error in the extraction technique. The spreading of the intersection is even worse at lower temperatures. This problem is dealt with in more detail in Chapter 4 of the thesis.

The resulting Level 6 HSPICE parameters that this extraction produces are LD ($= \Delta L/2$), RSC ($= R_{sd}/2$), RDC ($= R_{sd}/2$), and XJ (= LD/0.75). Capital letters will be used to designate user-defined HSPICE parameters. A lateral diffusion constant of 0.75 is assumed in determining the junction depth, XJ.

2.2.3 Effective Channel Width

A similar technique is used to extract the effective channel width. Figure 2.2 shows total conductance ($= I_{ds}/V_{ds}$) versus drawn channel width for different gate biases

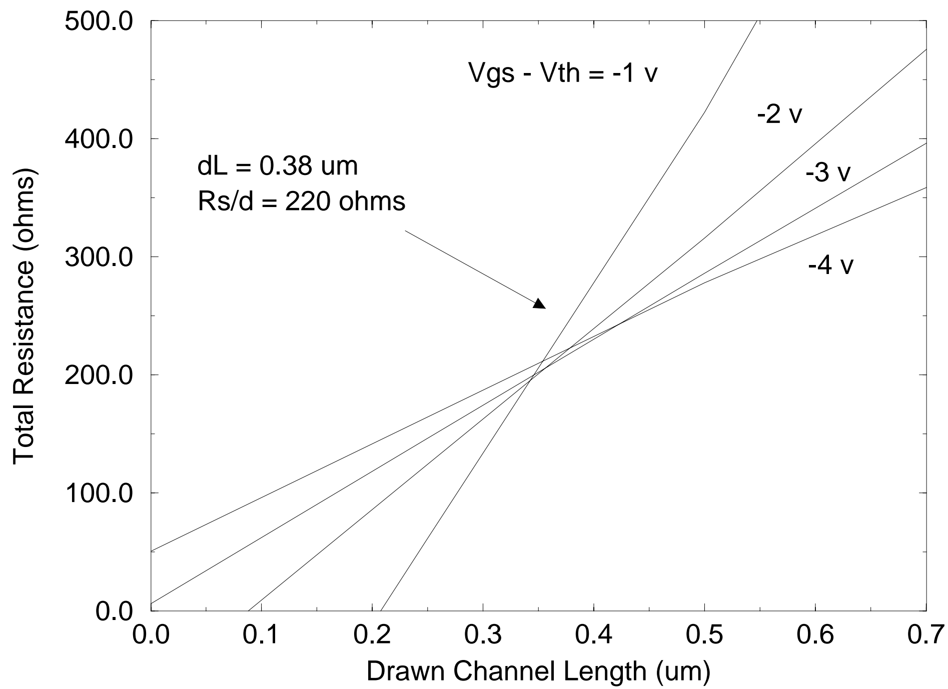

Figure 2.1: Total resistance versus drawn channel length for PMOS devices at 300 K. Channel width of all the devices is 25 μm. Gate biases for each line are indicated on the figure. The intersection point, obtained by extrapolating back the lines of constant gate drive above the threshold voltage, is (ΔL, R_{sd}).

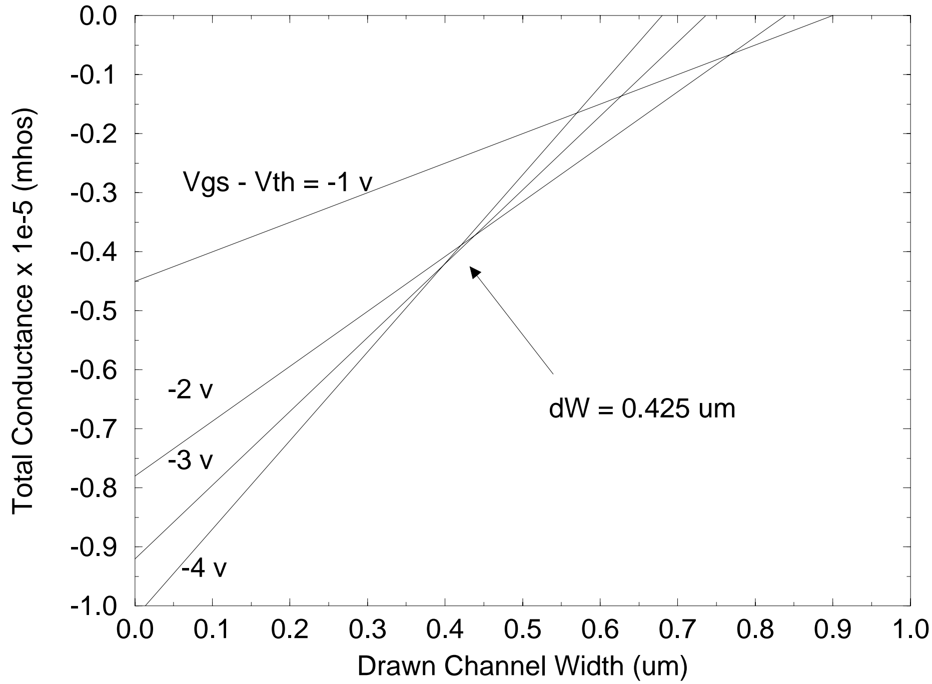

Figure 2.2: Total conductance versus drawn channel width for PMOS devices at 300 K. Channel length of all the devices is 6 μm. Gate biases for each line are indicated on the figure. The x-coordinate of the intersection is ΔW.

above the threshold voltage. Again, I_{ds}-V_{gs} data is used, but this time from transistors of long, constant channel length and varying channel widths. The x-coordinate of the intersection gives ΔW, which equals $W_{drawn} - W_{eff}$. Dividing ΔW by 2 gives the HSPICE parameter WD.

2.2.4 Threshold Voltage

The Level 6 HSPICE threshold voltage is defined as:

$$V_{th} = V_{bi} + \gamma \left(PHI + V_{sb}\right)^{1/2} \tag{2.1}$$

where V_{sb} is the voltage difference between the source and the substrate, PHI is the built-in potential, and V_{bi} is the built-in voltage.

$$V_{bi} = VTO - \gamma \; PHI^{1/2} + (\eta - 1)\,(PHI + V_{sb}) - \frac{LD}{L_{eff}}\,VSH - \frac{\epsilon_{si}}{COX\;L_{eff}}FDS\;V_{ds} \tag{2.2}$$

ϵ_{si} is the permittivity of silicon, C_{ox} is the oxide capacitance, L_{eff} is the effective channel length, and η is $1 + NWE/W_{eff}$, where NWE is the "narrow width effect". In this section, VTO, VSH, FDS, PHI, and GAMMA (which equals γ for large dimensions) will be extracted.

V_{th} Roll-Off with Channel Length

Although V_{bi} appears to be quite complex, many of the terms drop out under certain conditions. For long channel width devices (i.e. NWE $\ll W_{eff}$), η is approximately 1. So under low drain bias and zero substrate bias, (2.1) and (2.2) reduce to

$$V_{th} = VTO - \frac{LD}{L_{eff}}\,VSH \tag{2.3}$$

VSH models the threshold voltage roll-off with channel length, and can be obtained by fitting (2.3) to a plot of threshold voltage versus drawn channel length, as shown in Figure 2.3. VTO is equal to the long channel threshold voltage. Absolute values have been used in order to avoid confusion with signs. If NMOS parameters are to be extracted, no sign changes are necessary in any of the equations presented here. The only HSPICE parameter that is opposite in sign between NMOS and PMOS devices is VTO.

The I_{ds} vs. V_{gs} curves at low drain bias for transistors of constant width and varying length are used to obtain the threshold voltage. Again, a 10 nA*W/L drain

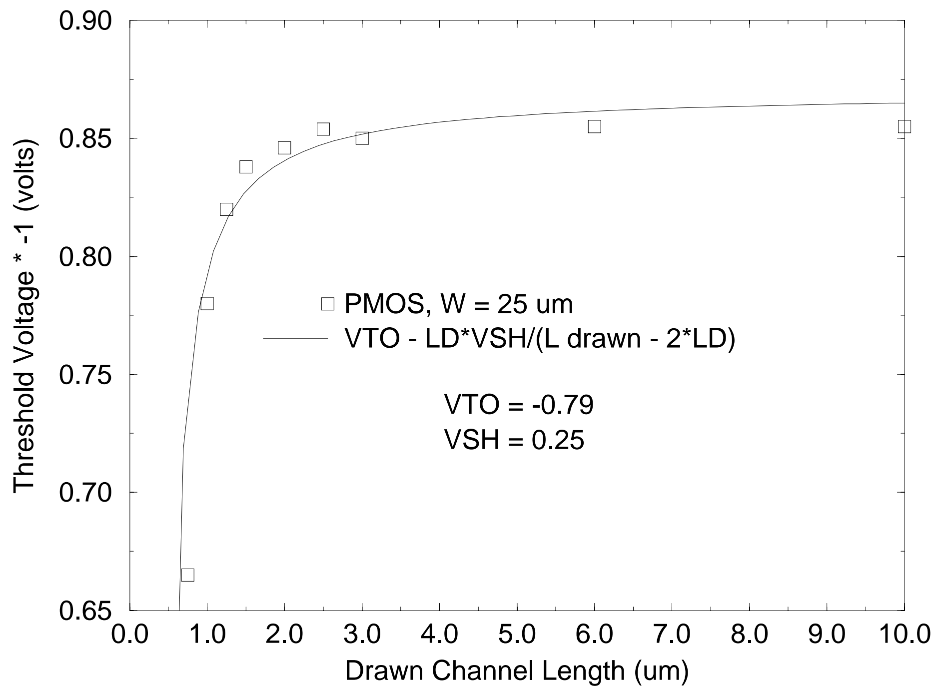

Figure 2.3: Threshold voltage versus drawn channel length for PMOS devices at 300 K. Channel width of all the devices is 25 μm. The HSPICE parameters VTO and VSH are extracted from fitting (2.3) to the experimental data.

current is used to define V_{th}. This definition, rather than extrapolating back from the peak transconductance, fits to HSPICE better.

V_{th} Roll-Off with Drain Bias

The next parameter to be obtained is FDS, which models the threshold voltage shift due to the drain bias. Like threshold voltage roll-off, this effect can be attributed to drain induced barrier lowering (DIBL) [12]. By using threshold voltages from a short-channel length device, the decrease of the threshold voltage with drain bias is clearly apparent.

Assuming no substrate bias and a long channel width, (2.1) and (2.2) reduce to

$$V_{th} = VTO - \frac{LD}{L_{eff}}\, VSH - \frac{\epsilon_{si}}{C_{ox} L_{eff}} FDS\, V_{ds} \tag{2.4}$$

The only new parameter is FDS. Therefore, by plotting threshold voltage versus drain bias for a single short-channel transistor (see Figure 2.4), FDS can be easily obtained by from the slope.

The $I_{ds} - V_{gs}$ curves with varying V_{ds} have been used to get the threshold voltages here. C_{ox}, the oxide capacitance, is obtained by dividing the oxide thickness (TOX) into the oxide permittivity. This value can be verified by measuring the gate capacitance in strong accumulation (large positive V_{gs} for PMOS, large negative V_{gs} for NMOS).

(2.4) may need to be shifted vertically in order to fit the threshold voltages in Figure 2.4, especially if (2.3) did not fit very well to the short channel threshold voltages. The amount of the shift can be neglected, as some of these extracted parameters may need to be adjusted when fitting the I-V characteristics. If there

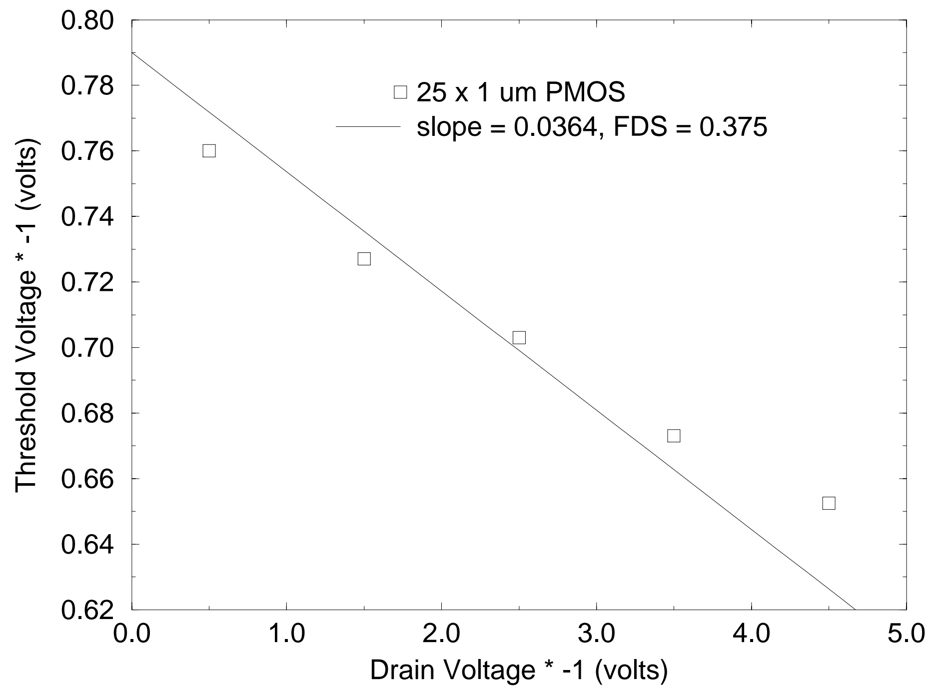

Figure 2.4: Threshold voltage versus drain bias for a 25 x 1 μm PMOS device at 300 K. The HSPICE parameter FDS is obtained by fitting the slope of (2.4) to the experimental data.

is some doubt on the value of FDS, several short-channel transistors can be used to determine FDS, and an average value can be taken.

V_{th} versus Substrate Bias

Finally, to determine PHI and γ, the threshold voltage versus substrate bias is plotted for a long channel length, long channel width transistor. Under this condition with a low drain bias, (2.1) and (2.2) reduce to

$$\begin{aligned} V_{th} &= VTO - \frac{LD}{L_{eff}} VSH - \frac{\epsilon_{si}}{C_{ox} L_{eff}} FDS\, V_{ds} \\ &\quad + GAMMA\,(PHI + V_{sb})^{1/2} - GAMMA\;\,(PHI)^{1/2} \end{aligned} \qquad (2.5)$$

Large dimensions should be used because γ changes as both length and width decrease. The user-defined parameter GAMMA equals γ under the above conditions.

Note that the first three terms in (2.5) are independent of V_{sb}. GAMMA is the slope of V_{th} vs. $(PHI + V_{sb})^{1/2} - PHI^{1/2}$. In order to obtain GAMMA, a value for PHI is first assumed, so that the above graph can be plotted and the slope determined. The substrate doping, NSUB, is then calculated using

$$NSUB = \frac{GAMMA^2\, COX^2}{2\; q\; \epsilon_{si}} \qquad (2.6)$$

where q is the electron charge. One critical assumption in (2.6) is that the substrate doping is uniform. This is generally not true because ion-implantation is typically performed in the channel region in order to shift the threshold voltage of the device for optimized logic swing. The non-uniform doping can cause a non-linear V_{th} vs. $(PHI + V_{sb})^{1/2} - PHI^{1/2}$. However, this was not seen in these particular devices. The Level 6 HSPICE model is capable of modeling a non-uniform substrate using a "Multi-level Gamma Model", but this feature is turned off in order to reduce the complexity of the extraction.

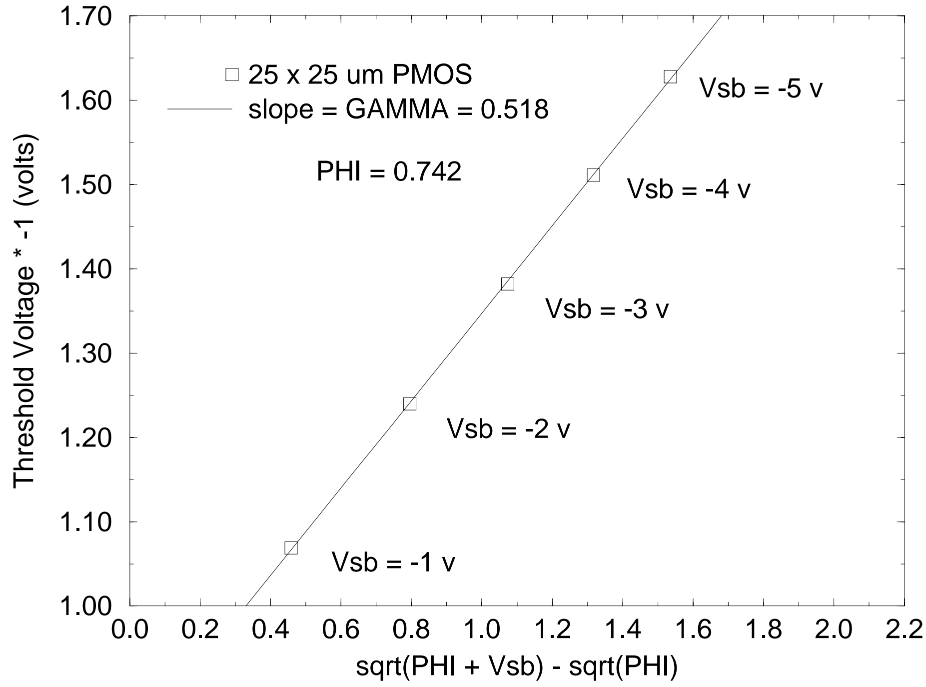

Figure 2.5: Threshold voltage versus $(PHI + V_{sb})^{1/2} - (PHI)^{1/2}$ for a 25 x 25 μm PMOS device at 300 K. An iterative process of guessing PHI, determining GAMMA, and calculating NSUB and PHI is used to determine the HSPICE parameters.

From the substrate doping, PHI is determined using

$$PHI = \frac{2kT}{q} \ln \frac{NSUB}{n_i} \tag{2.7}$$

where k is the Boltzmann constant, T is the temperature, and n_i is the intrinsic carrier concentration (1.45×10^{10} cm^3 at 300 K).

If the PHI calculated in (2.7) does not match the initially assumed PHI used to obtain GAMMA, the new value for PHI should be used to redetermine GAMMA. This process of guessing PHI, calculating GAMMA and NSUB, and recalculating PHI, should be iterated over several cycles until the calculated value of PHI agrees with the initial assumed value. The final result of this iteration process is shown in Figure 2.5.

2.2.5 Effective Mobility

The effective mobility versus gate bias can calculated from the I_{ds} vs. V_{gs} curve at low drain bias of a transistor of large dimensions. Solving the linear I_{ds}-V_{gs} equation for μ_{eff} results in

$$\mu_{eff} = \frac{I_{ds}\, L_{eff}}{W_{eff}\, COX\, (V_{gs} - VTO - \frac{V_{ds}}{2})V_{ds}} \tag{2.8}$$

Note that the above equation only applies for transistors of large dimensions, since the devices are not saturation velocity limited and not subject to short-channel effects.

In the Level 6 HSPICE model, several different functions can be used to fit the effective mobility versus gate bias. The MOB=1 model is used here due to its simplistic form and good fit with the data.

$$\mu_{eff} = \frac{U0}{1 + F1(V_{gs} - V_{bi} - F3\, V_{ds})} \tag{2.9}$$

The MOS mobility is inherently lower than the bulk mobility, U0, due to scattering along the rough Si-SiO_2 interface. High doping in the channel will also decrease mobility due to coulombic scattering. An increase in the gate bias will increase the vertical electric field, confining the carrier flow even closer to the interface. As a result, the effective mobility will decrease even further [13]. However, an increase in the drain bias will actually improve the mobility because the carriers will be accelerated faster due to the larger horizontal electric field. The faster carriers will have less probability of being coulombically scattered with the channel dopants [14].

U0 and F1 are obtained by fitting (2.9) to the μ_{eff} vs. V_{gs} curve (see Figure 2.6). V_{bi} is calculated using (2.2). A small value or zero can be assumed for F3, since V_{ds}

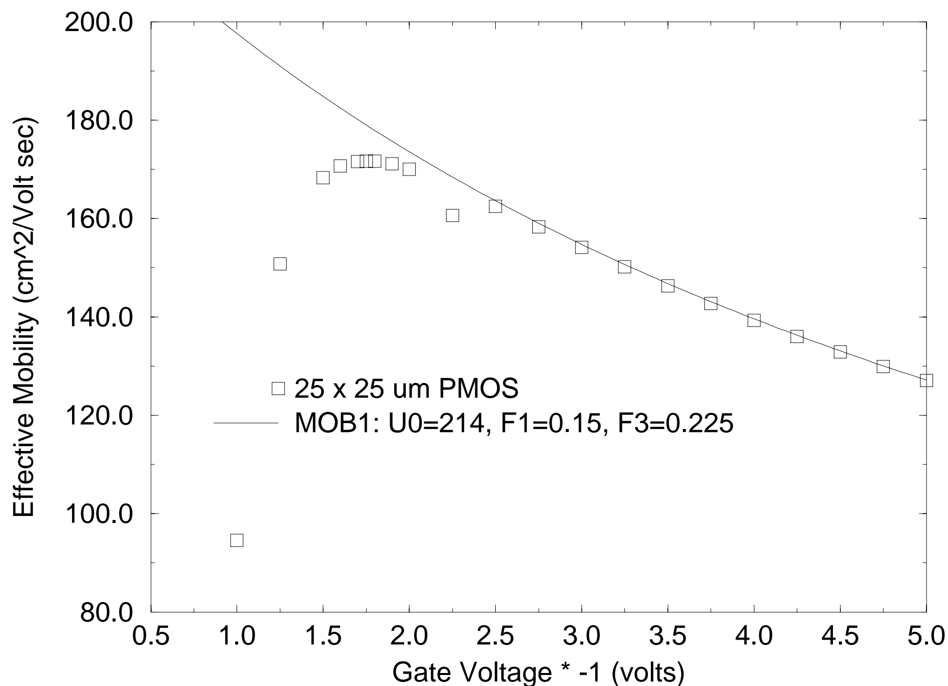

Figure 2.6: Effective mobility versus gate bias for a 25 x 25 μm PMOS device at 300 K. The HSPICE parameters U0 and F1 are extracted from fitting (2.9) to the experimental data.

is small in this case. F3 can be adjusted to fit the I_{ds} vs. V_{ds} curves later. As (2.9) predicts, the mobility decreases with increasing gate bias, due to the increase in the vertical electric field. The fit is excellent for large gate biases, but worsens for low to moderate V_{gs}. The other Level 6 mobility models have a similar flaw.

2.3 PMOS Fit

The above set of extracted parameters are used as a starting point to fit the HSPICE simulated I-V curves to the measurement results. Adjustments to the already extracted parameters may have to be made, and additional terms will be obtained during the I-V fitting. Large dimension devices should be fitted first. Parameters which model short-channel effects can then be obtained or adjusted by inspecting

the next smaller channel length device. Finally, short-channel width parameters can be set (if necessary) by shrinking the channel widths and fitting the I-V curves.

2.3.1 I_{ds} vs. V_{gs} At Low V_{ds}

The first set of curves to fit are the drain current vs. gate voltage curves at low drain bias. Figure 2.7 shows the linear I_{ds}-V_{gs} characteristics for different channel lengths. The 25 x 25 μm curve can be used to verify the accuracy of the mobility model parameters since the dimensions are so large that short channel effects do not apply. Adjustments to U0 and F1 can be made to produce a better fit. For example, F1 should be decreased if the simulated I-V curve is lower than the measurement results at higher gate biases. U0 will shift the entire curve up or down. VTO may also need to be adjusted so that the device turns on at the right time.

To fit the shorter channel lengths better, RSD, RSC, and LD can be modified. Increasing RSD and RSC will decrease the simulated current, especially at high gate biases. RSD and RSC should remain equal to each other, since the source and drain are symmetric. VSH may also need to be changed so that these devices turn on correctly with the measurements.

Once the linear I_{ds}- V_{gs} characteristics look reasonable, the subthreshold characteristics can be fitted. Using the WIC parameter, one of three possible subthreshold models can be chosen. WIC=1 was used here. Figure 2.8 shows the same I-V curves as in Figure 2.7, but on a logarithmic scale. The subthreshold slope can be adjusted through NFS, the number of fast interface states per cm^2. This value can be compared to the interface state density obtained from a high-low C-V technique [15]. VTO and VSH may need to be changed to improve the fit in the subthreshold

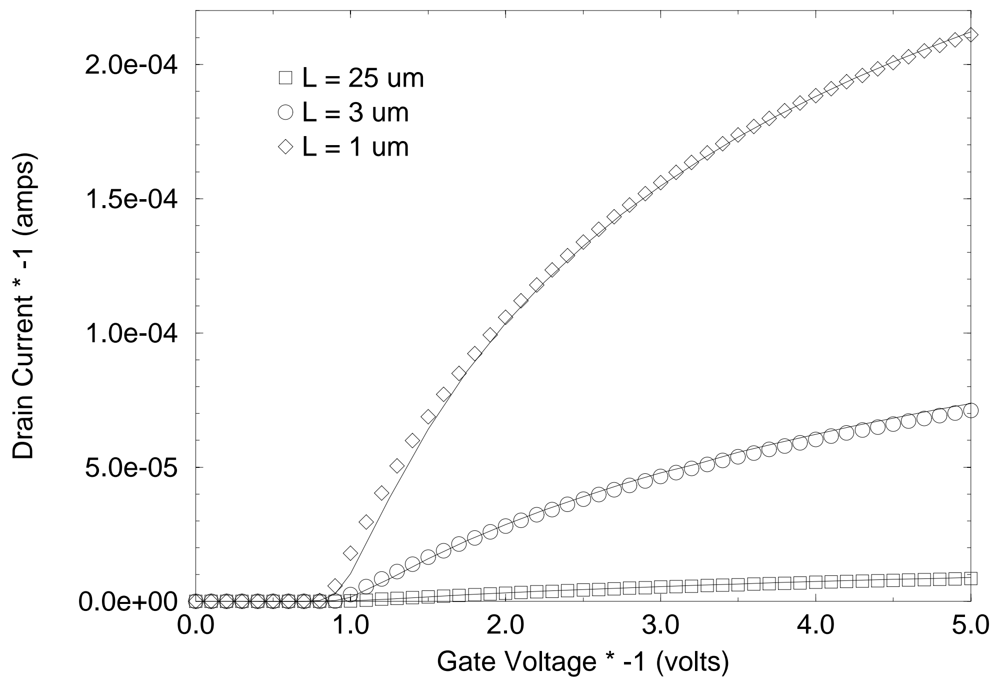

Figure 2.7: I_{ds}-V_{gs} curves (linear scale) for PMOS devices at 300 K. The channel width of all of the devices is 25 μm. Points indicate measurement data. Solid lines indicate HSPICE simulation data.

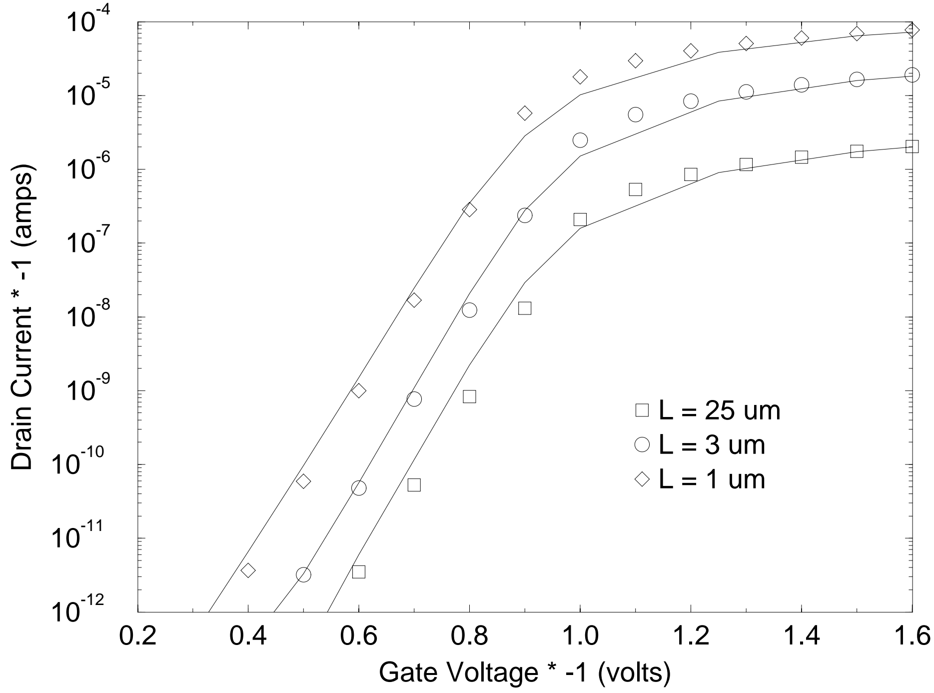

Figure 2.8: I_{ds}-V_{gs} curves (logarithmic scale) for PMOS devices at 300 K. The channel width of all of the devices is 25 μm.

regime. However, if this is done, the linear I_{ds}- V_{gs} curves should be reexamined to ensure that the simulated curves still match the measurements.

2.3.2 I_{ds} vs. V_{ds} With V_{gs} Varied

Since the I_{ds}- V_{ds} curves cover a large range of voltages, it is essential to obtain a good fit for these curves. As above, the 25 x 25 μm device is fitted first. Figure 2.9 shows the simulation and measurement results. U0 and F1 in (2.9) can again be verified and adjusted if necessary. F1 can be decreased if the simulated I-V is too low at high gate biases. In addition, F3 can be altered if the I-V fit worsens for higher drain biases. If the drain current does not saturate at the right point, VMAX (generally in the 10^6 range) should be adjusted.

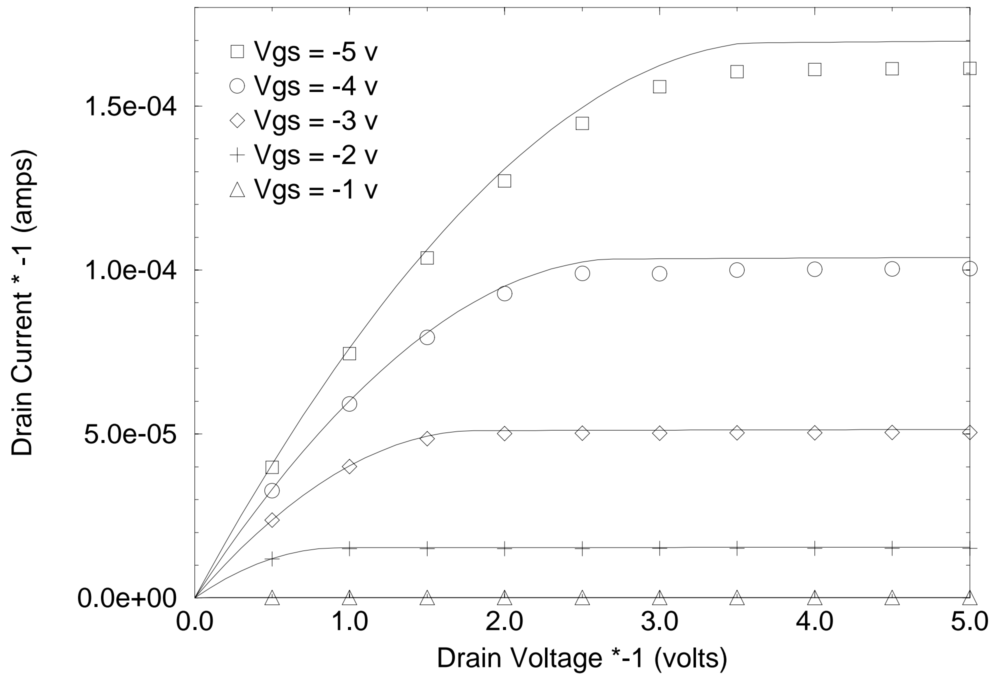

Figure 2.9: I_{ds}-V_{ds} curve for a 25 x 25 μm PMOS device at 300 K. Points indicate measurement data. Solid lines indicate HSPICE simulation data.

The I_{ds}-V_{ds} curves for shorter and shorter channel lengths can be matched after the 25 x 25 μm is fitted successfully. As the channel length decreases, the output conductance will increase, resulting in a non-zero slope in I_{ds} at drain biases above the saturation point. To model this behavior, the parameter LAMBDA should be used. Values in the 10^{-6} range are reasonable. A channel length modulation model of 1 (CLM=1) has been used, although several, more empirical models can be used.

VMAX, LAMBDA, and the mobility parameters should be adjusted such that the best I_{ds}- V_{ds} fit is obtained for the full range of channel lengths. This will often require several iterations, since a perfect fit at short channel lengths may cause changes and deviations in the long channel data. Figures 2.10 and 2.11 show the final I_{ds}- V_{ds} curves for channel lengths of 3 μm and 1 μm, respectively.

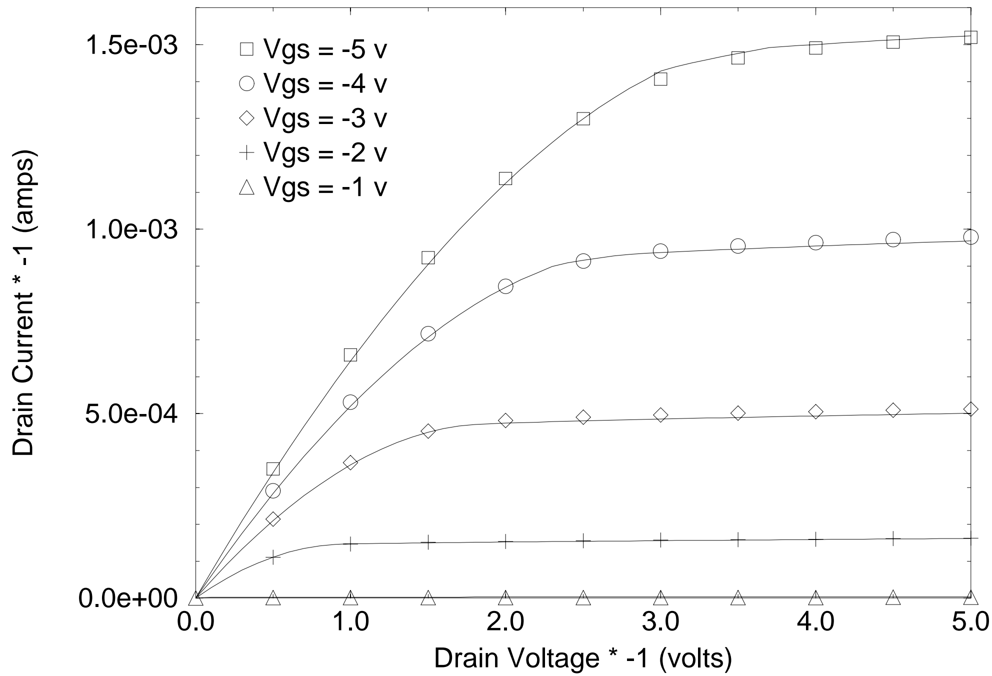

Figure 2.10: I_{ds}-V_{ds} curve for a 25 x 3 μm PMOS device at 300 K. Points indicate measurement data. Solid lines indicate HSPICE simulation data.

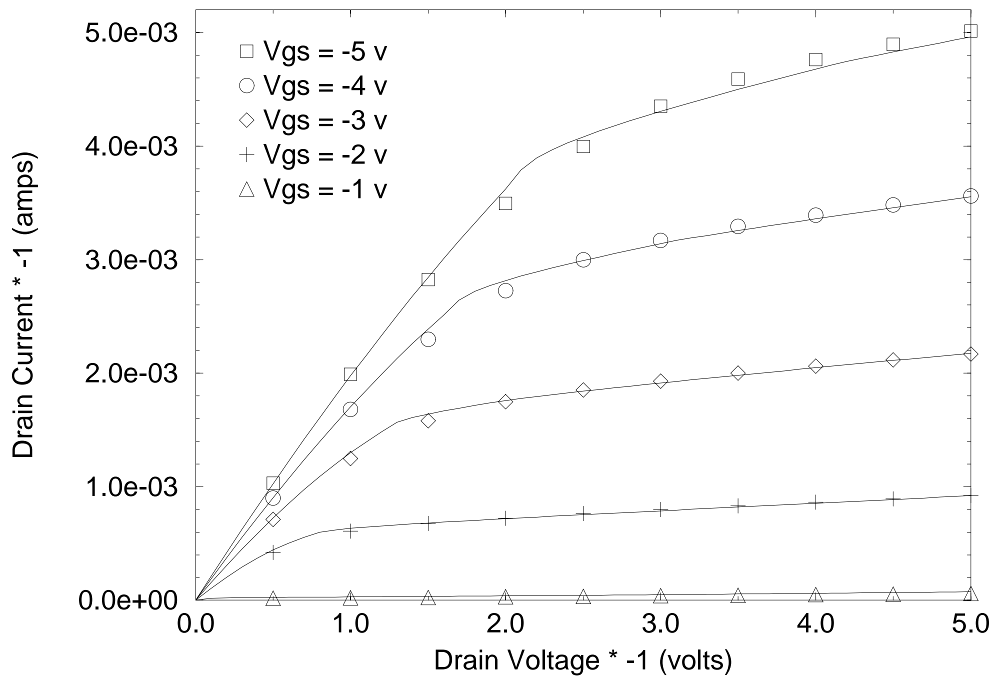

Figure 2.11: I_{ds}-V_{ds} curve for a 25 x 1 μm PMOS device at 300 K. Points indicate measurement data. Solid lines indicate HSPICE simulation data.

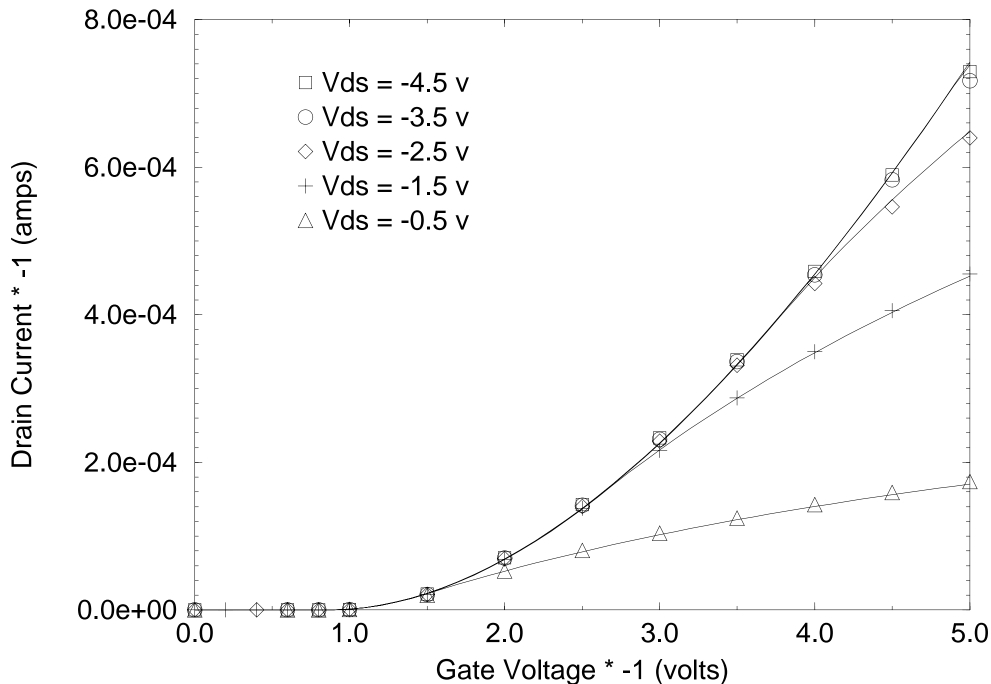

Figure 2.12: I_{ds}-V_{gs} curve with variable V_{ds} for a 25 x 25 μm PMOS device at 300 K. Points indicate measurement data. Solid lines indicate HSPICE simulation data. This method of fitting should be employed if there is trouble fitting the I_{ds}-V_{ds} curves.

If there are problems fitting the I_{ds}-V_{ds} data, a plot of I_{ds} vs. V_{gs} with V_{ds} as a parameter can be generated and fitted first. Figure 2.12 shows such a plot for a 25 x 25 μm PMOS. This is essentially the same data as the I_{ds}-V_{ds} curve, but the x-axis is V_{gs} instead of V_{ds}. The effects of changing FDS, VMAX, and the mobility parameters will be more apparent in this plot than in the I_{ds}-V_{ds} curves.

After the I_{ds}-V_{ds} data fits well, the I_{ds}-V_{gs} curves should be resimulated to ensure that there is still a good match. Changing the parameters, especially those associated with the mobility, to obtain a good I_{ds}-V_{ds} fit may worsen the I_{ds}-V_{gs} curves.

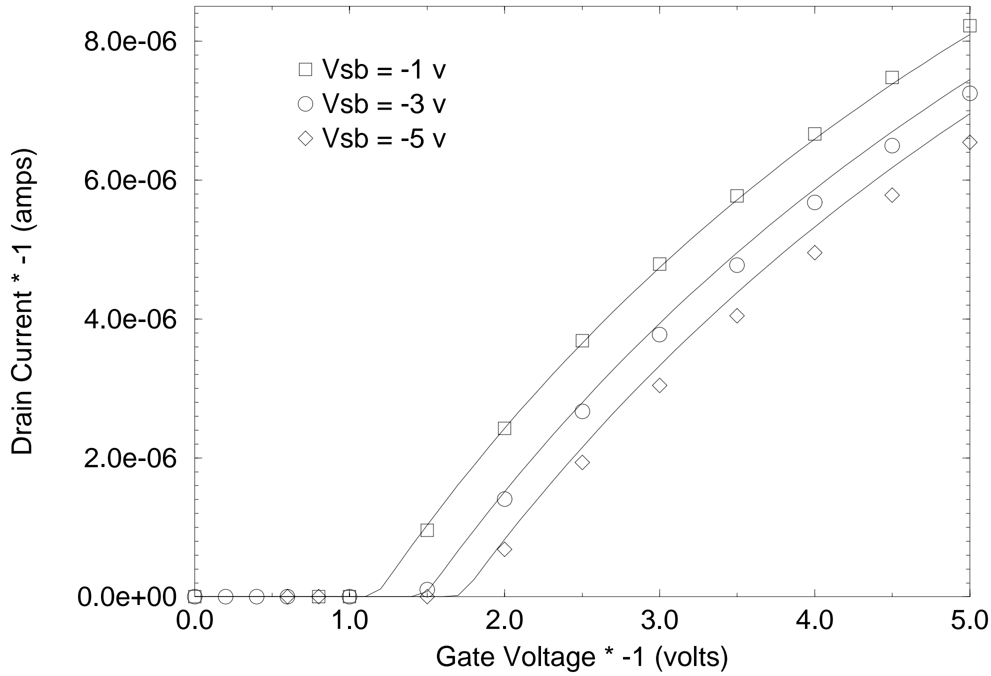

Figure 2.13: I_{ds}-V_{gs} curve with variable V_{sb} for a 25 x 25 μm PMOS device at 300 K. Points indicate measurement data. Solid lines indicate HSPICE simulation data.

2.3.3 I_{ds} vs. V_{gs} With V_{sb} Varied

I_{ds}-V_{gs} curves at low drain bias with varying substrate bias are shown in Figures 2.13, 2.14, and 2.15, for channel lengths of 25, 3, and 1 μm, respectively. To obtain a better fit, GAMMA and PHI can be changed. However, these values are used to calculate the current even with zero substrate bias. So any changes to these values will shift all of the previous I-V curves, and may result in poorer matching. Since the agreement for most of the data here was already within ten percent, no additional adjustments were made. If changes are to be made, the complexity of the fitting increases dramatically since both the I_{ds}-V_{ds} and I_{ds}-V_{gs} curves will shift. Several iterations between all the different I-V curves will be required to obtain the most optimized fit.

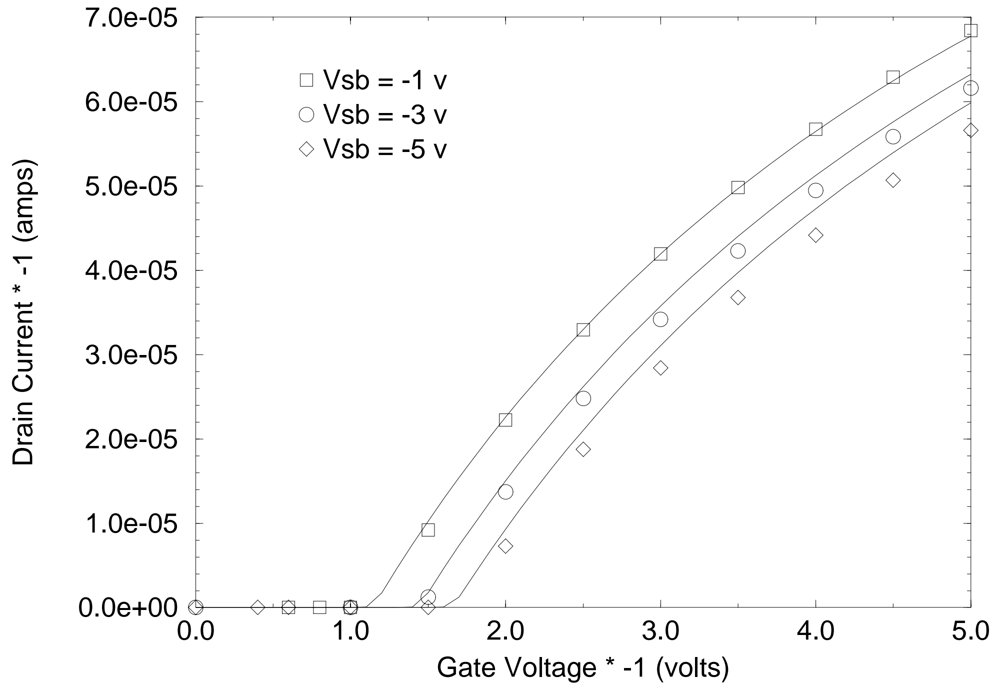

Figure 2.14: I_{ds}-V_{gs} curve with variable V_{sb} for a 25 x 3 μm PMOS device at 300 K. Points indicate measurement data. Solid lines indicate simulation data.

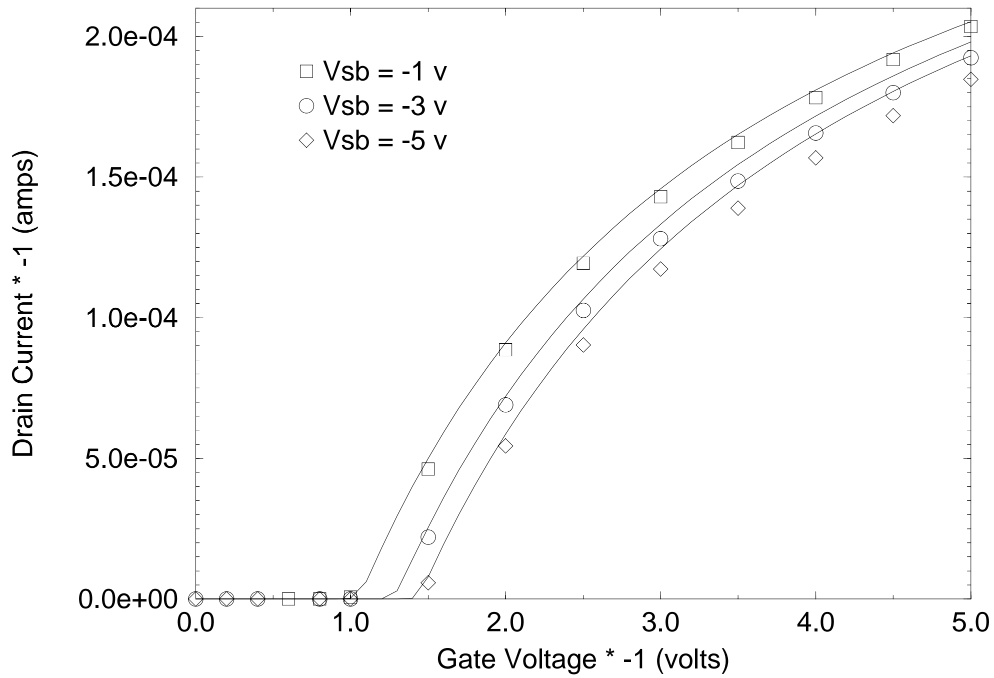

Figure 2.15: I_{ds}-V_{gs} curve with variable V_{sb} for a 25 x 1 μm PMOS device at 300 K. Points indicate measurement data. Solid lines indicate simulation data.

Since there is no V_{sb} dependence in the MOB=1 model, it is expected that the I_{ds} vs. V_{gs} curves with non-zero V_{sb} will not fit as well as the other curves. In addition, there is no Level 6 parameter which is applied only in the case of a non-zero substrate bias. As a result, it is difficult to make any adjustments to just the I_{ds}-V_{gs} curves with non-zero V_{sb}. Adjustments to PHI, GAMMA, NWE, and WD appear to have shift these curves the most.

2.3.4 Short Channel Width Fit

Once the long channel width devices have been fitted, the I-V curves of devices with shorter channel widths can be examined. Figure 2.16 shows the I_{ds}- V_{gs} curves at low drain bias for transistor widths of 10 μm and 6 μm. Ideally, these devices should fit reasonably well. However, the NWE and NWM parameters can be used to improve the fit. Increasing NWE will increase the threshold voltage. Increasing NWM will decrease the current drive, although a high NWM will cause poor subthreshold behavior. WD can also be adjusted to provide a better fit. Changing any other parameters will probably cause a significant shift the long channel width results. Nevertheless, if any changes are made, the long channel width I-V curves should be regenerated to ensure that no significant deviations have occurred.

In the PMOS devices here, no additional modification or additions to the parameters were necessary. Figures 2.17 and 2.18 show the I_{ds}-V_{ds} curves for the 10 x 6 μm and 6 x 2 μm PMOS devices. These devices are the closest dimensions to those used in the ring oscillator circuits. The I_{ds} vs. V_{gs} curves with non-zero V_{sb} also fitted reasonably well.

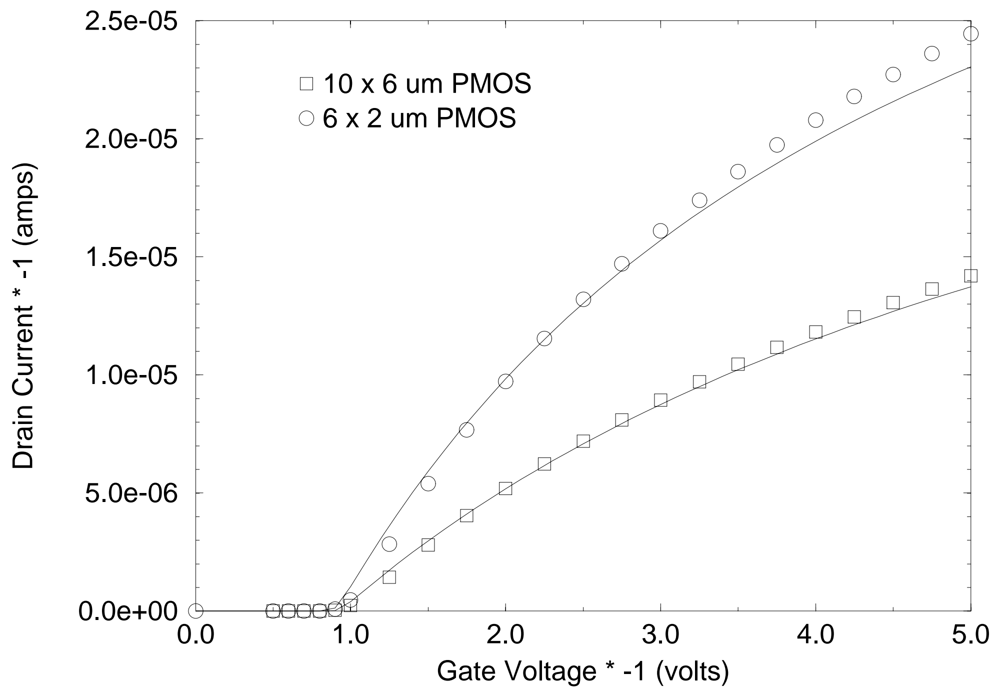

Figure 2.16: I_{ds}-V_{gs} curves for a 10 x 6 μm and a 6 x 1 μm PMOS device at 300 K. Points indicate measurement data. Solid lines indicate HSPICE simulation data.

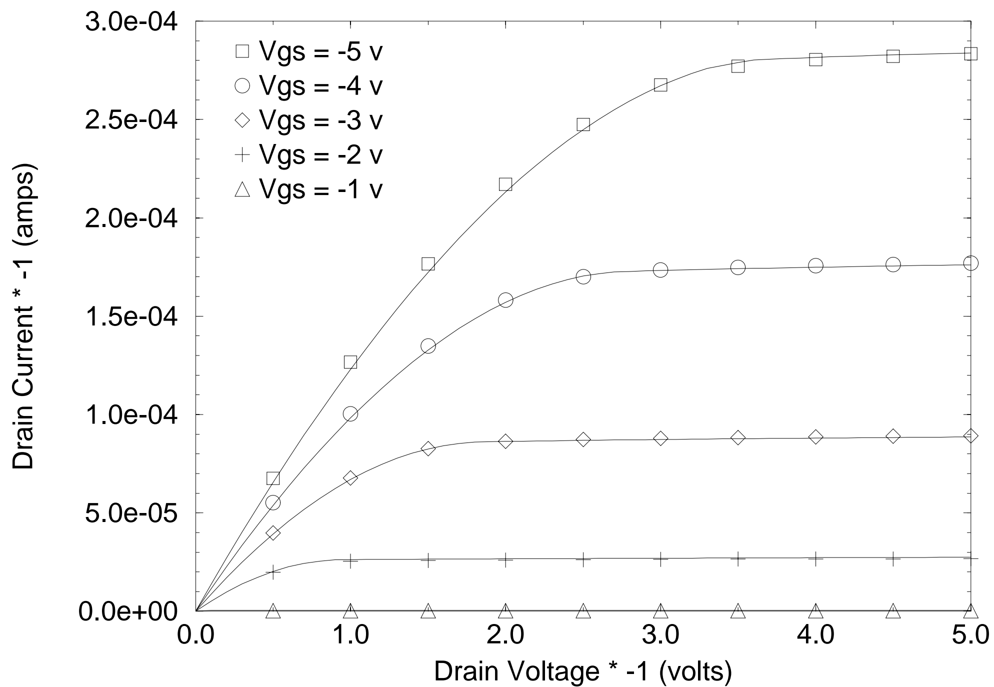

Figure 2.17: I_{ds}-V_{ds} curve for a 10 x 6 μm PMOS device at 300 K. Points indicate measurement data. Solid lines indicate simulation HSPICE data.

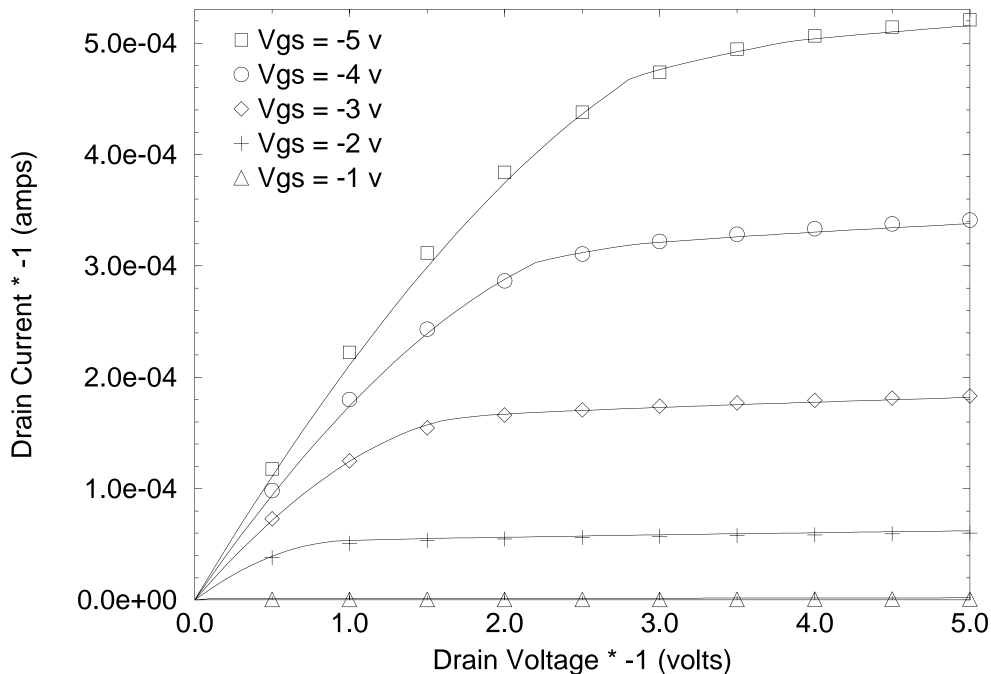

Figure 2.18: I_{ds}-V_{ds} curve for a 6 x 2 μm PMOS device at 300 K. Points indicate measurement data. Solid lines indicate HSPICE simulation data.

2.4 NMOS Fit

The extraction technique described in this chapter has also been performed on the HP-MOSIS NMOS devices. I_{ds}-V_{gs} curves with low drain bias are shown in Figure 2.19. The drain current at high gate biases is underapproximated by the simulation. However, the I_{ds}-V_{ds} curves (shown next) match with the measurements better under this condition.

I_{ds}-V_{ds} curves for the 25 x 3 μm and 25 x 2 μm NMOS devices are shown in Figures 2.20 and 2.21. One of the less desirable features of the NMOS fit is the sharp "kink" at the saturation point. This effect is only seen in the short channel devices and is the result of a poor mobility fit. Figure 2.22 shows the effective electron mobility and its associated fit. The measured electron mobility is concave

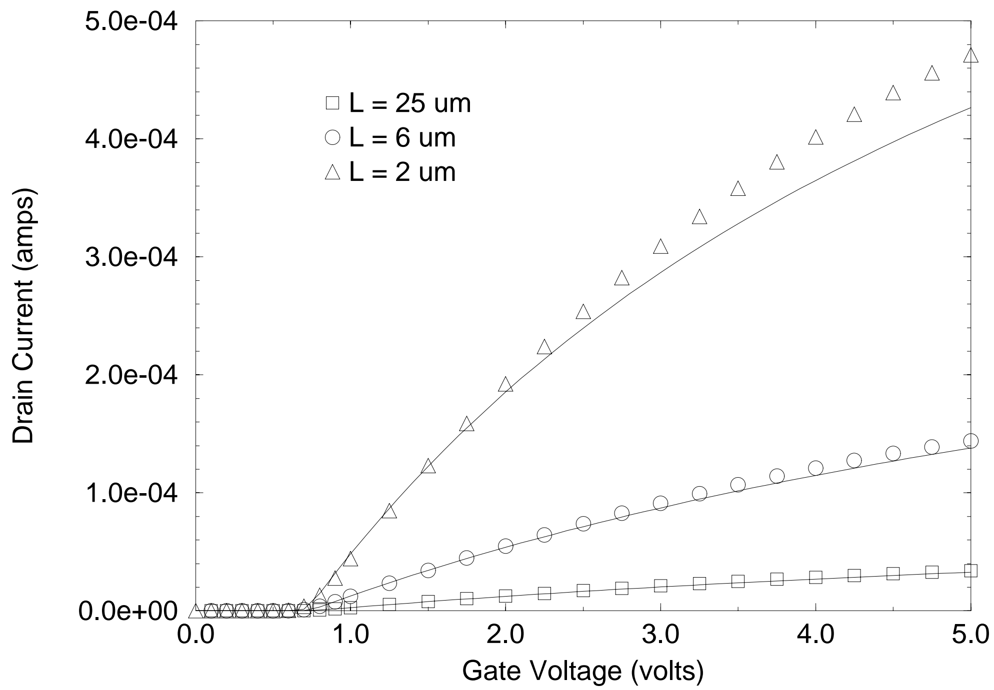

Figure 2.19: Linear I_{ds}-V_{gs} curves for NMOS devices at 300 K. The channel width of all the devices is 25 μm. Points indicate measurement data. Solid lines indicate HSPICE simulation data.

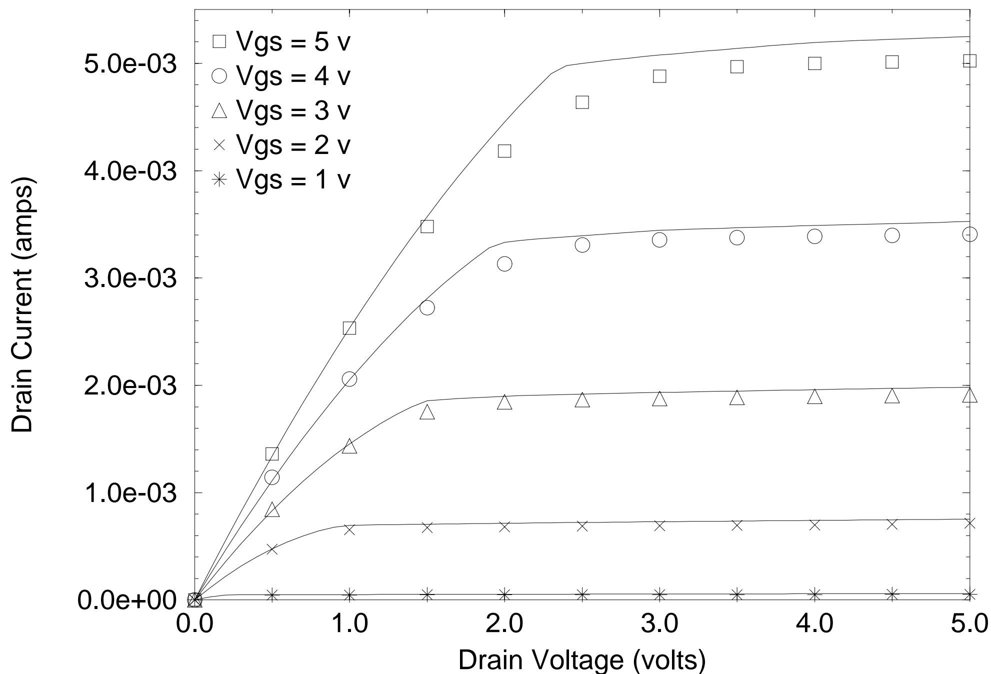

Figure 2.20: I_{ds}-V_{ds} curve for a 25 x 3 μm NMOS device at 300 K. Points indicate measurement data. Solid lines indicate HSPICE simulation data.

down versus gate bias. Since all of the mobility models are modeled using concave up functions (1/x dependencies), it is extremely difficult to obtain a reasonable fit to the mobility. As a result, it becomes more difficult to fit the I-V curves. The PMOS I_{ds}-V_{ds} curves show a less severe kink, due to the better mobility fit.

The saturation kink may also be the result of a discontinuity in modeling the saturation velocity. As a result, the linear and saturation drain currents will not match up well. Using the multi-level gamma option in the Level 6 model can prevent such a discontinuity, although the complexity of this fitting will increase.

Figures 2.23 and 2.24 show the I_{ds}-V_{ds} curves for a 6 x 2 μm and 6 x 1 μm NMOS, respectively. The fit is a little bit better than the long channel width, short channel length results, although the saturation kink is still evident. Adjustments

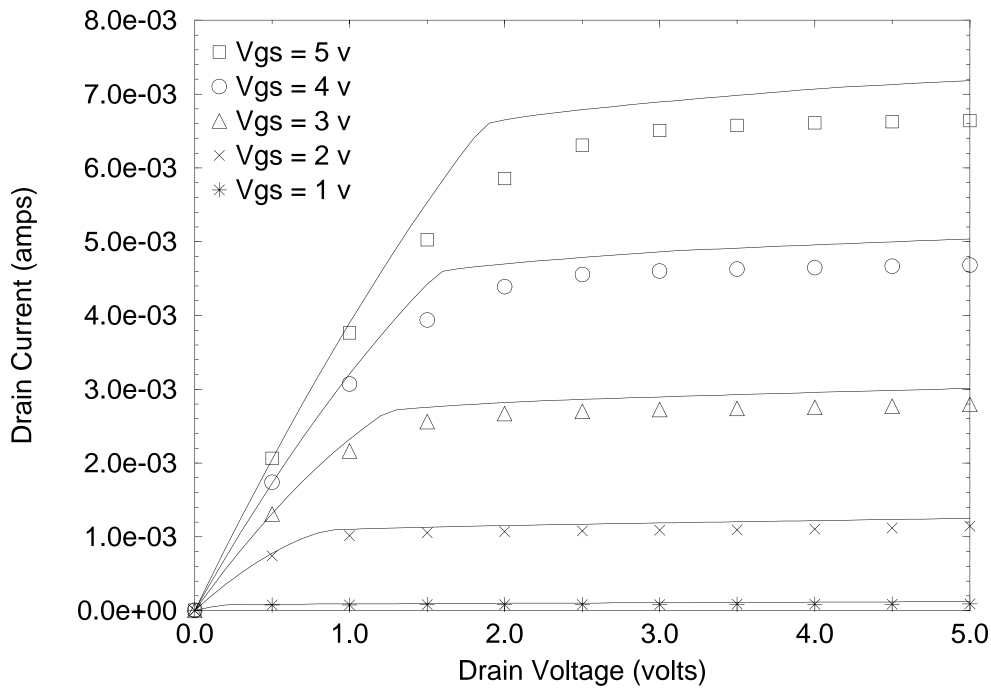

Figure 2.21: I_{ds}-V_{ds} curve for a 25 x 2 μm NMOS device at 300 K. A severe kink in the drain current near the saturation point can be seen at high V_{gs}.

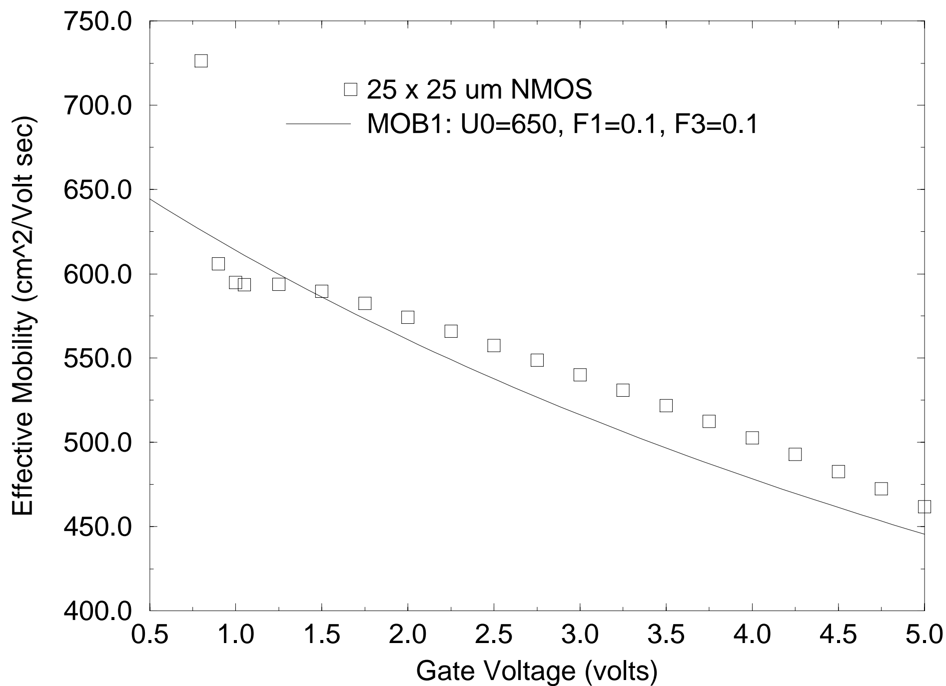

Figure 2.22: Effective mobility versus gate bias for a 25 x 25 μm NMOS device at 300 K. The electron mobility does not fit as well as the hole mobility (see Figure 2.6).

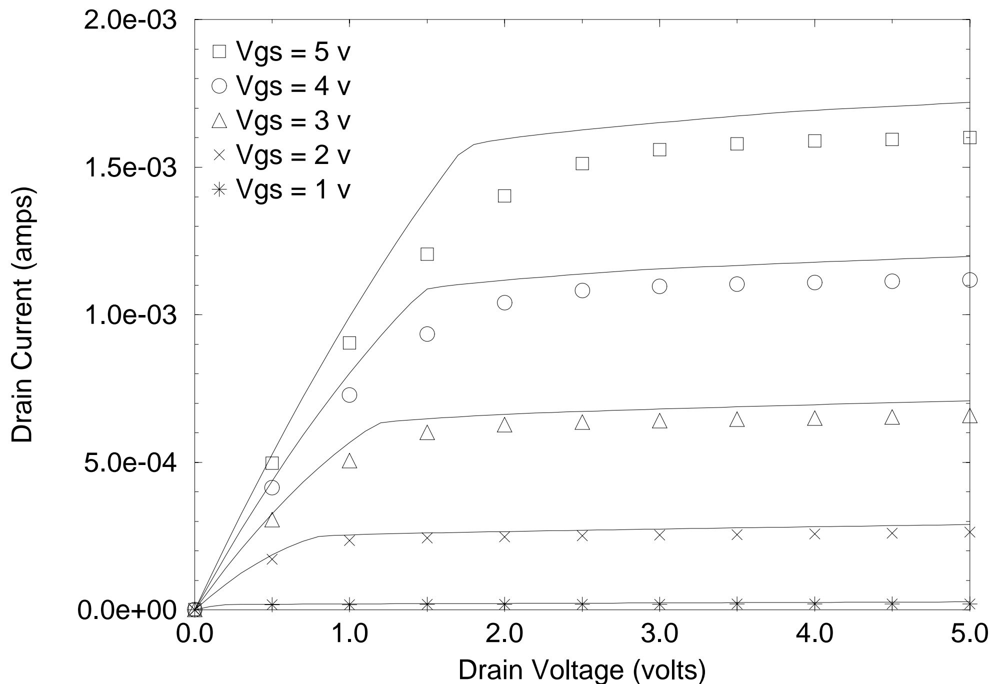

Figure 2.23: I_{ds}-V_{ds} curve for a 6 x 2 μm NMOS device at 300 K. Points indicate measurement data. Solid lines indicate HSPICE simulation data.

to FDS, VMAX, LAMBDA, and the mobility parameters may result in a better fit, although all of the previous I-V curves may shift as well.

2.5 Ring Oscillator Fit

To demonstrate the accuracy and usefulness of the extracted HSPICE parameters, several ring oscillators have been measured. The structures vary in the number of stages, but the output signals are buffered before they are sent to a two transistor load. Table 2.1 lists the three ring oscillators that were tested at 300 K.

In order to model circuit performance, the parasitic capacitances have been measured, since they will contribute to the circuit delay. The junction capacitance (CJ:

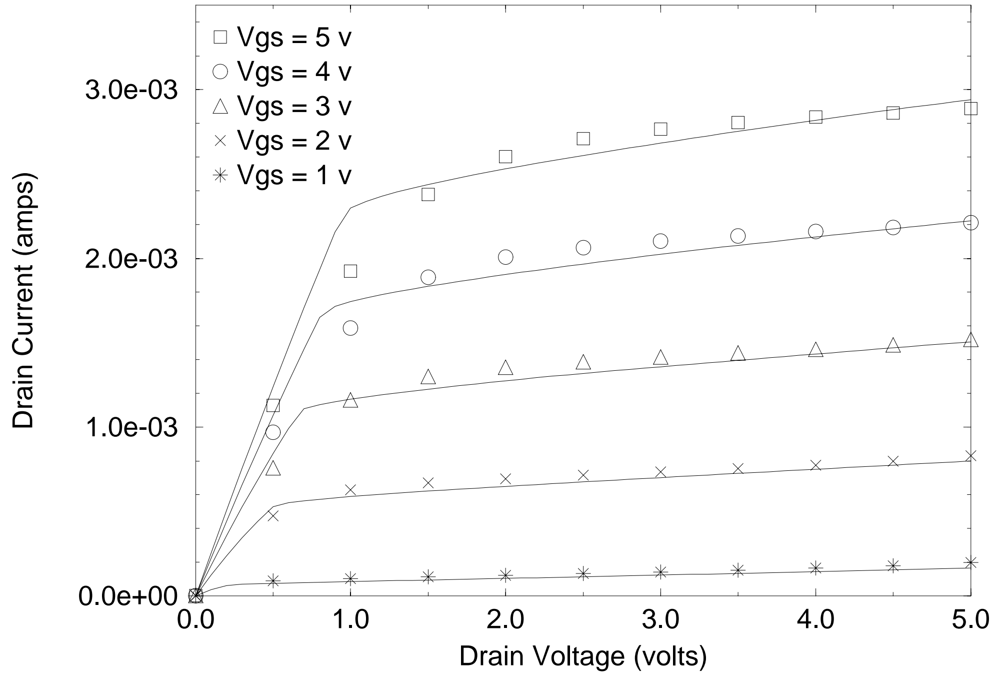

Figure 2.24: I_{ds}-V_{ds} curve for a 6 x 1 μm NMOS device at 300 K. Points indicate measurement data. Solid lines indicate HSPICE simulation data.

Number of Stages	PMOS W/L	NMOS W/L
13	6/2	6/2
17	6/2	6/2
41	6/1	6/1

Table 2.1: Ring Oscillators Measured at T = 300 K

between the source/drain and the substrate), the sidewall capacitance (CJSW: between the sides of the diffused source/drain and the substrate), and the overlap capacitances (CJSO, CJDO, CJBO: between the gate and the lateral diffusion of the source/drain regions) have all been measured using several specialized structures on the HP-MOSIS chip. These values are automatically calculated by HSPICE if they are not given, but it is better to measure a real value for these capacitances if possible.

Propagation delay per stage versus power supply voltage has been plotted for the three different ring oscillators of Table 2.1 in Figure 2.25. Propagation delay is the period of the output waveform divided by two times the number of stages. The same power supply voltage was applied on both the ring oscillators and the buffer. The load transistors were left floating, and the output pad was connected directly to the 50 Ω input of a Tektronix 11301 Programmable Oscilloscope. Simulation results match the measurements well. The parasitic capacitances can be increased slightly to obtain a closer fit. The delay per stage of the two different 2 μm ring oscillators line up with each other. The scaled (1 μm) channel length oscillator has three times lower propagation delay, primarily due to its larger current drive.

2.6 Conclusion

Table 2.2 summarizes the steps in extracting the Level 6 HSPICE parameters for an MOS device. The effective dimensions, threshold voltage, and mobility are modeled first. These form an initial foundation for running simulations. Additional parameters are determined by fitting the simulation data to the actual I-V measurements. Some of the initial values may also have to be modified in the process of the fitting.

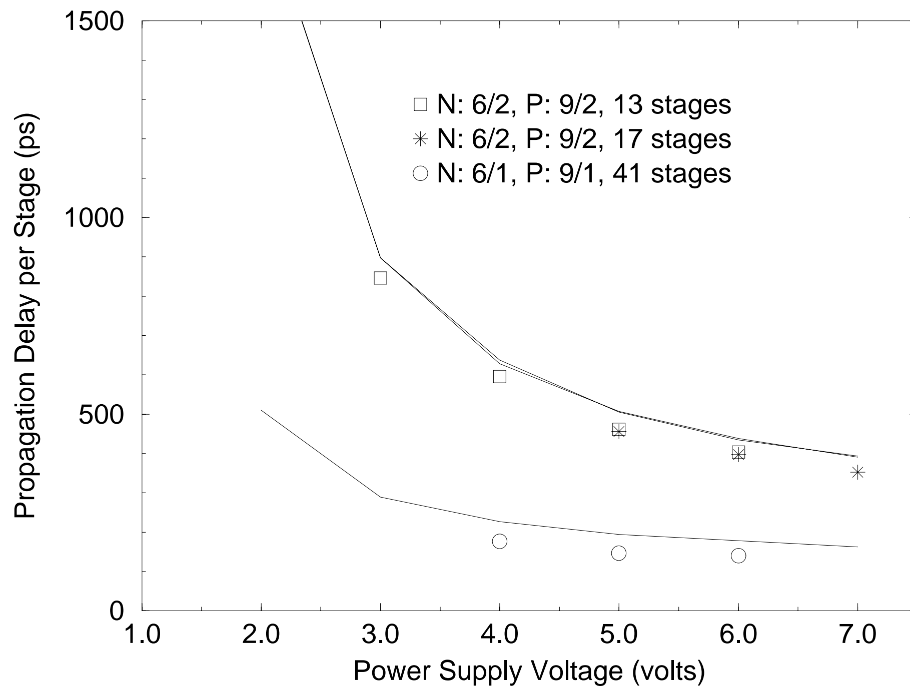

Figure 2.25: Propagation delay per stage versus power supply voltage of ring oscillators at 300 K. Points indicate measurement results. Lines indicate HSPICE simulation results.

Step	HSPICE Parameters Obtained
Extract R_{sd} and ΔL	RSD, RSC, LD
Extract ΔW	WD
Fit V_{th} vs. L_{drawn}	VTO, VSH
Fit V_{th} vs. V_{ds}	FDS
Fit V_{th} vs. V_{sb}	GAMMA, PHI, NSUB
Fit μ_{eff} vs. V_{gs}	MOB, U0, F1, F3
Fit I_{ds} vs. V_{gs}	WIC, NFS
Fit I_{ds} vs. V_{ds}	CLM, LAMBDA
Fit I_{ds} vs. V_{gs} (back-gate biased)	
Fit I-V curves for shorter channel widths	NWE, NWM, WD

Table 2.2: Extraction procedure for obtaining Level 6 HSPICE parameters.

However, changes to the parameters in the middle of the I-V fitting may significantly alter the previously fitted I-V curves.

Good results have been obtained over a large range of channel lengths and channel widths for an HP-MOSIS technology. With improvements in the mobility modeling, an even better fit can be obtained. However, if a single set of parameters cannot be used to model the entire gamut of dimensions, "domains" can be created. For example, if there are problems fitting across channel lengths, one set of parameters can be used to fit the long channel lengths, and another set with slightly different values can be used to fit short channel lengths. Care must be taken to ensure that both models fit intermediate channel lengths. If domains are not desired, then one will have to consider giving up a good fit in one regime for a better fit in another. If digital circuits are to be simulated, then the fit to long dimensions (especially channel length) will be less critical.

The extracted parameters, along with the parasitic capacitances, can be used for circuit modeling as well as I-V modeling. The simulated propagation delay of the HP-MOSIS ring oscillators has been shown to match the measurements well. This

step-by-step method for extracting SPICE parameters is not limited to the Level 6 HSPICE model and can be applied to fit data to any SPICE circuit model.

Chapter 3

Extraction Results at 77 K

3.1 Introduction

The basic principles shown in the extraction technique of Chapter 2 can be applied at any temperature to any arbitrary SPICE model. Therefore, the tradeoffs in device performance between operating at 300 K versus 77 K can be understood by examining how the SPICE parameters change. In this chapter, the Level 6 HSPICE parameters for the HP-MOSIS devices of Chapter 2 are obtained at 77 K. Again, a reasonable fit is obtained with a single set of parameters for both the NMOS and PMOS devices. However, a few problems that did not occur at 300 K slightly complicate the extraction procedure. Nevertheless, the model parameters accurately predict circuit behavior at 77 K. Finally, the resulting HSPICE parameters at 77 K are compared with those at 300 K and some conclusions are drawn.

3.2 Extraction Problems at 77 K

The same procedure in extracting the HSPICE parameters at 300 K has been applied at 77 K for the HP-MOSIS devices of Chapter 2. A Lakeshore Cryotronics dewar with temperature control was used to cool the devices down to 77 K for the I-V and circuit measurements.

3.2.1 Effective Channel Dimensions and Source/Drain Resistance

Figure 3.1 shows the results of applying the method of [11] to obtain the source/drain resistance and effective channel length. Although the method results in a good intersection with positive results at 300 K, a negative ΔL and poor intersection are obtained. A negative ΔL is not physical and will result in a simulation error if it is applied to HSPICE. As a result, the 300 K values for LD, RSC, and RDC have been used as a starting point for the 77 K parameters. The values have been adjusted to fit the I_{ds}-V_{gs} curves.

Similarly, the WD value at 300 K has also been used at 77 K, since the plot of total conductance versus effective channel width also intersects at a negative value as well. It is possible to get positive values for R_{sd}, ΔL, and ΔW if all of the parameters are given a gate-bias dependence. This will be elaborated in Chapter 4.

3.2.2 Threshold Voltage Fluctuations

One problem with the low temperature measurements that is immediately apparent is the threshold voltage. Figure 3.2 shows the threshold voltage versus channel

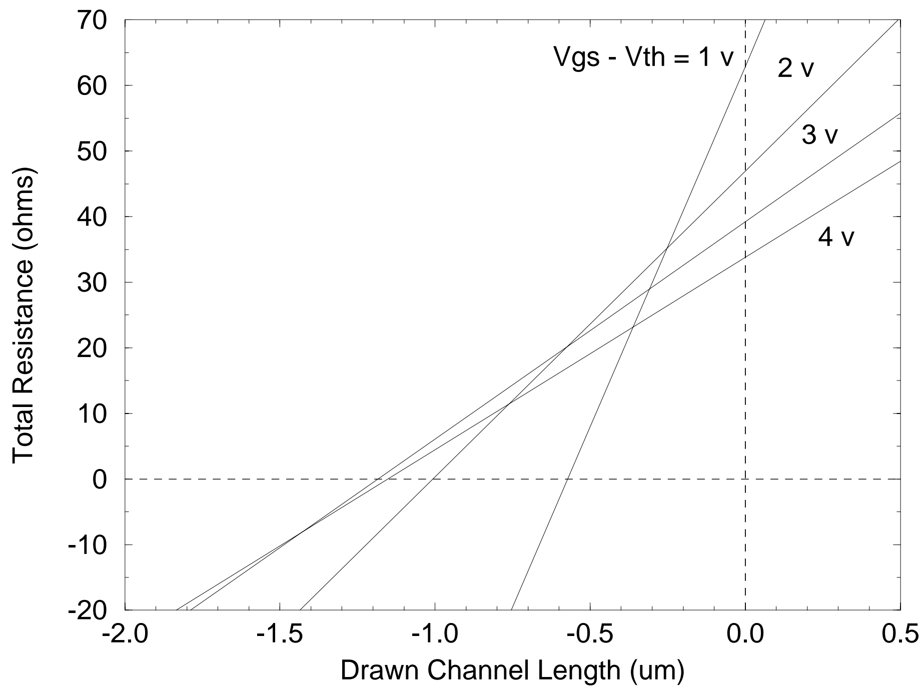

Figure 3.1: Total resistance versus drawn channel length for NMOS devices at 77 K. Channel width of all the devices is 25 μm. Gate biases for each line are indicated on the figure. The intersection of the lines of constant gate drive above the threshold voltage give R_{sd} and ΔL. However, the lines do not intersect together at a single point. In addition, ΔL is negative, which is not physically possible.

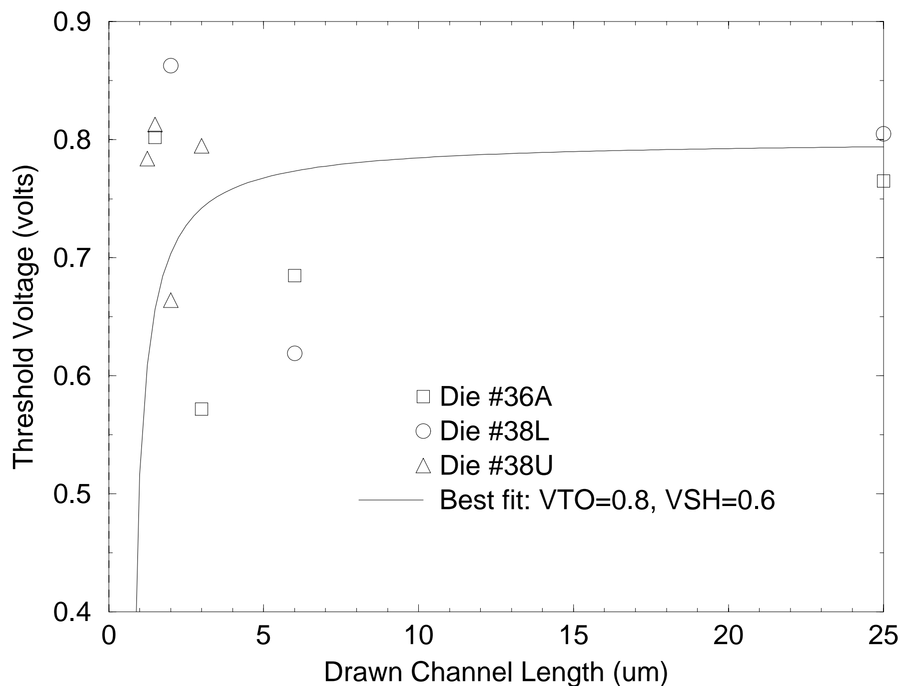

Figure 3.2: Threshold voltage versus drawn channel length for NMOS devices at 77 K. Channel width of all the devices is 25 μm. The roll-off is not clear at all. A best fit was performed, nonetheless, to obtain VTO and VSH.

length for the NMOS devices at 77 K. The roll-off in V_{th} is not clear, neither within nor across dies. The variation in the threshold voltage may have resulted from accidental stress during the bonding and packaging of the device or from cooling down the device to 77 K. After the low temperature measurements, the threshold voltage did not recover to the original 300 K values. This indicates that some form of stress had occurred. When the devices were cooled back down to 77 K, similar threshold voltages to the original results were obtained, even after holding at 77 K for a longer period of time.

The devices may have even been stressed during the measurements. Since current drive and electric fields increase at lower temperatures, device reliability becomes more questionable. In fact, it has been shown that the same amount of stress at

lower temperatures results in a greater amount of damage to a device [16]. As a result, the 77 K I-V measurement results shown later in this chapter were performed only up to 3 volts instead of 5 volts. In addition, I_{ds}-V_{gs} sweeps at low drain bias were performed at three different phases of the low-temperature measurement: after bonding and packaging the device for dewar measurements, before cooling down the device, and after cooling down the device. In all of the $I_{ds} - V_{gs}$ measurements, the curves did not change very much, indicating that the lower voltage measurements at 77 K were accurate.

The poor roll-off of V_{th} with channel length may also be a result of edge effects. The carrier concentration on the edge of the transistor along the length of the channel is typically different from the concentration in the center of the transistor. A "field-implant" is typically used outside of the active region of the transistor for isolation purposes, but the doping does not change abruptly from the edge of the isolated region to the edge of the transistor. As a result, the edges of the device may turn on sooner than the middle, especially at low temperatures, since the threshold voltage and current drive increase. Freeze-out near the edges [1] may also contribute to this threshold voltage problem. Implant recipes may need to be adjusted to prevent edge effects from affecting the I-V curves at 77 K. Threshold voltage instability is ultimately process dependent. Measurements performed at 77 K on NMOS and PMOS transistors manufactured from a different technology show a well behaved roll-off, and very little fluctuation between dies.

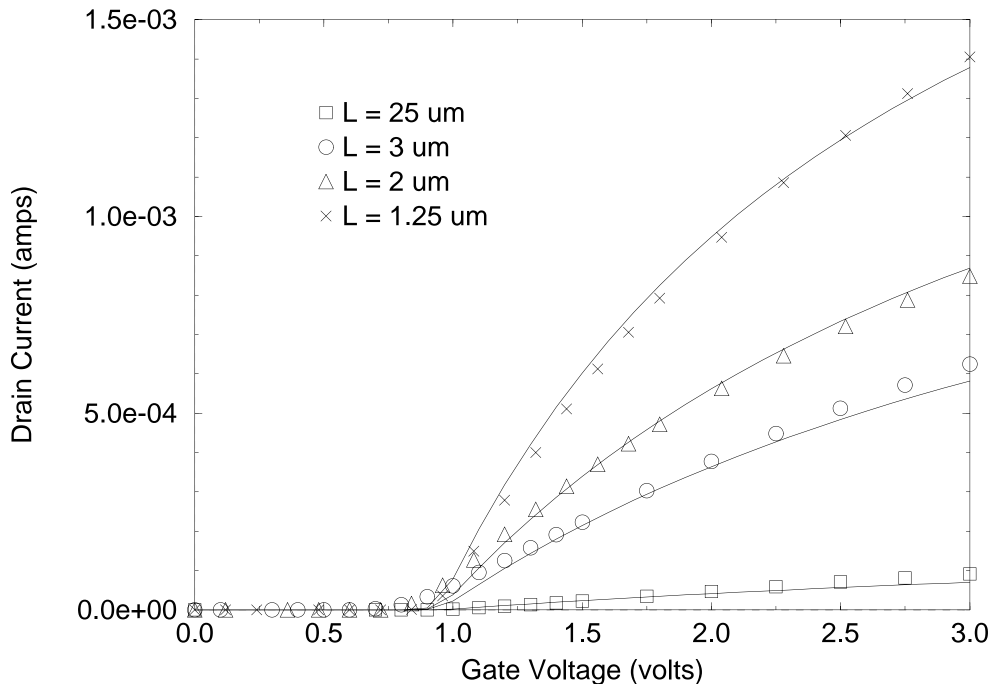

Figure 3.3: I_{ds}-V_{gs} curves (linear scale) for NMOS devices at 77 K. Channel width of all the devices is 25 μm. Points indicate measurement data. Solid lines indicate HSPICE simulation results.

3.3 I-V Fit at 77 K

3.3.1 I_{ds} vs. V_{gs} Curves

The I_{ds}-V_{gs} curves at low drain bias for the NMOS devices are shown in Figure 3.3. The overall fit of the curves is acceptable and not as difficult as the threshold voltage fluctuations would suggest.

The subthreshold characteristics for the 25 x 25 μm and the 25 x 3 μm devices are shown in Figure 3.4. NFS had to be reduced to 5.0e10, which is a fairly small interface state density. However, the simulated subthreshold slope is still too high. The subthreshold characteristics can be fitted better by changing the simulation temperature. For all of the 77 K HSPICE simulations here, the temperature was

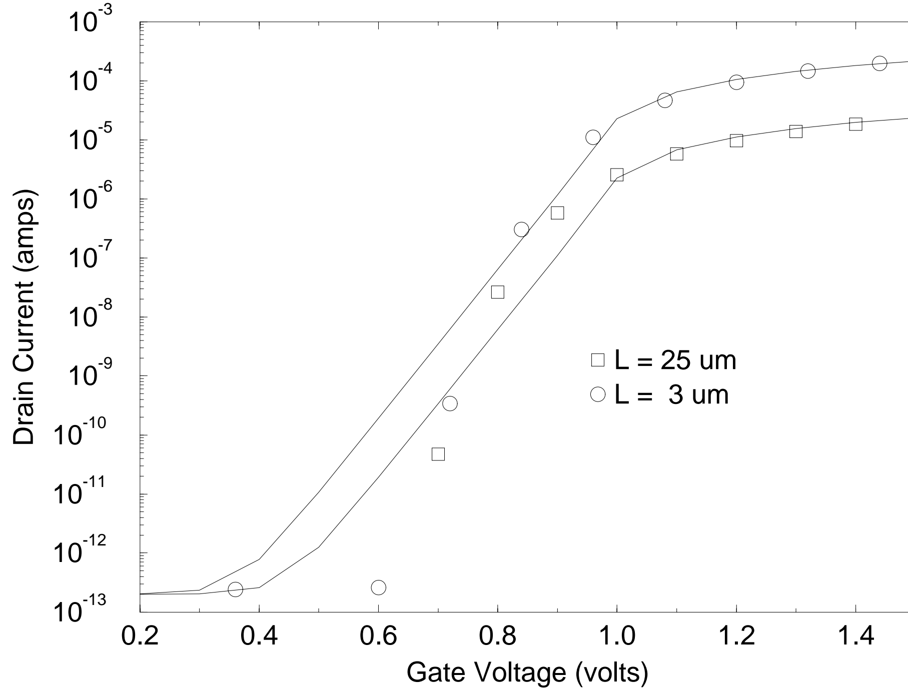

Figure 3.4: I_{ds}-V_{gs} curves (logarithmic scale) for NMOS devices at 77 K. Channel width of all the devices is 25 μm. Points indicate measurement data. Solid lines indicate HSPICE simulation results.

left at 300 K. By changing the simulation and model reference temperature to 77 K, a better subthreshold fit can be obtained, since the subthreshold slope is proportional to kT/q. A 77 K HSPICE simulation can be performed by adding TREF=-196.15 in the .model card, TNOM=-196.15 in the .option card, and "temp -196.15" at the bottom of the input file. Since the only significant problem with the fitting lied in the subthreshold behavior, the 77 K simulations were run at 300 K. Most of the extracted SPICE parameters are not expected to change very much since they do not dependent on the TNOM, TREF, or .temp statements.

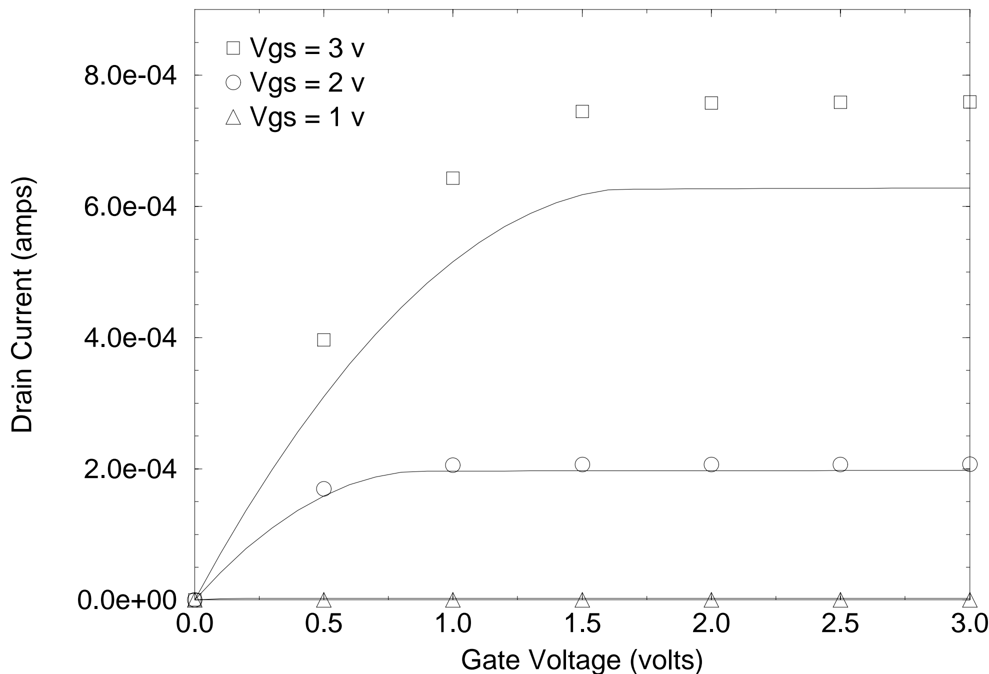

Figure 3.5: I_{ds}-V_{ds} curve for a 25 x 25 μm NMOS device at 77 K. Points indicate measurement data. Solid lines indicate HSPICE simulation results.

3.3.2 I_{ds} vs. V_{ds} Curves

Figures 3.5, 3.6, and 3.7 show the simulated and measured I_{ds}-V_{ds} curves for a 25 x 25 μm, a 25 x 3 μm, and a 25 x 1.5 μm NMOS device, respectively. Just as at 300 K, a "kink" near the saturation point is evident in the simulation curves. Although the simulated current is well under the measured current for the long channel device, the remaining devices fit reasonably well. Using a "domain", a set of slightly different parameters, for the long channel device, a better fit can be achieved. However, most circuit applications will not call for the use of such large dimensions, especially in the length.

For the short channel devices, the simulated current overapproximated the measurements for gate biases above 3 volts. However, if the simulation curves are shifted

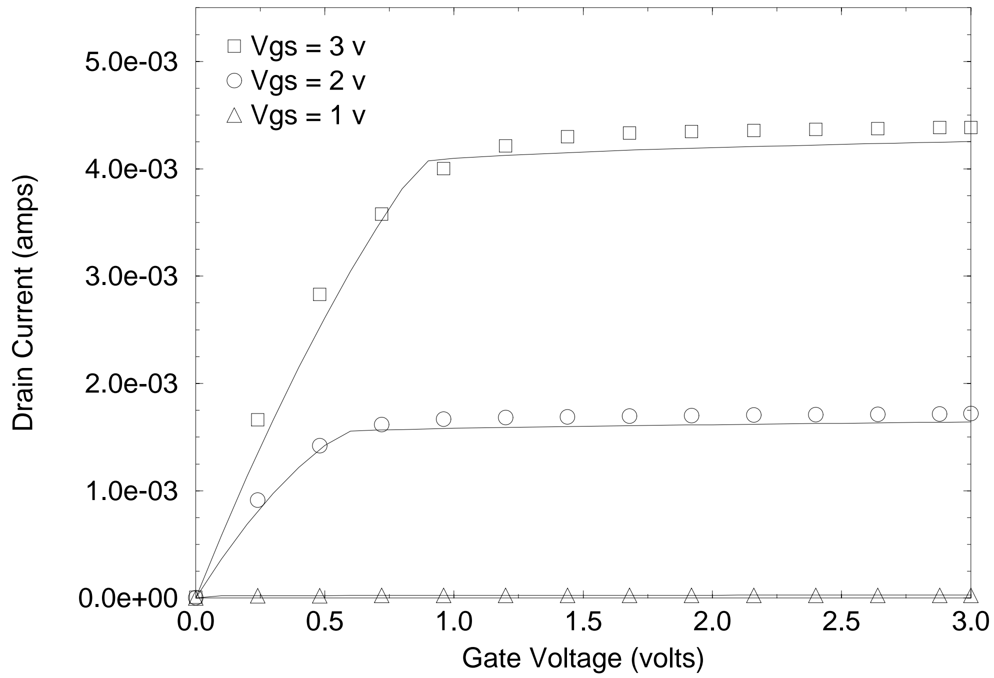

Figure 3.6: I_{ds}-V_{ds} curve for a 25 x 3 μm NMOS device at 77 K. Points indicate measurement data. Solid lines indicate HSPICE simulation results.

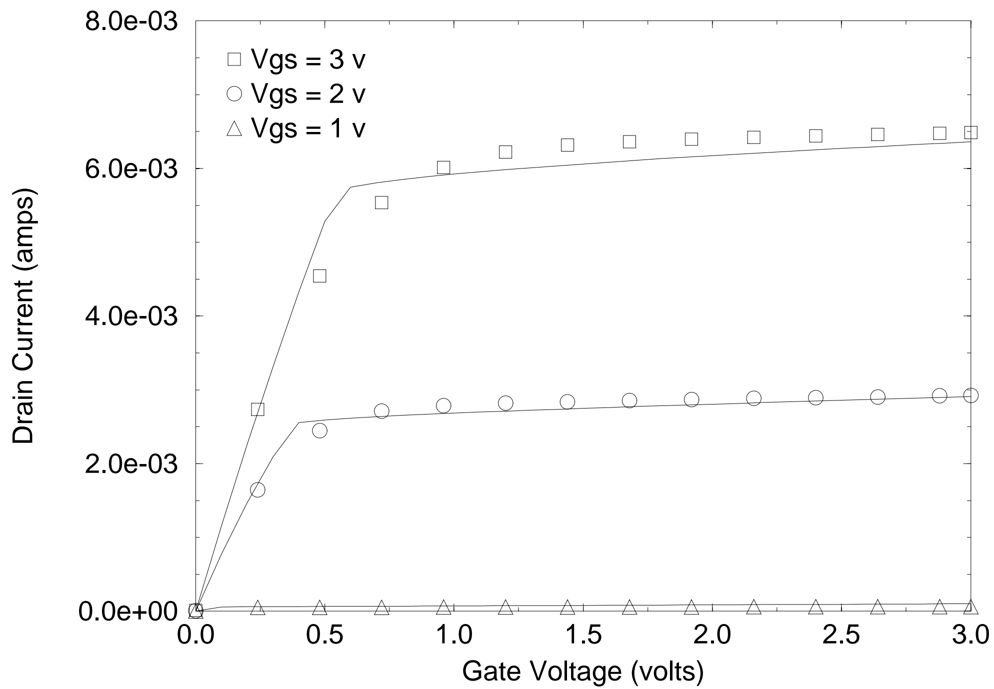

Figure 3.7: I_{ds}-V_{ds} curve for a 25 x 1.5 μm NMOS device at 77 K. Points indicate measurement data. Solid lines indicate HSPICE simulation results.

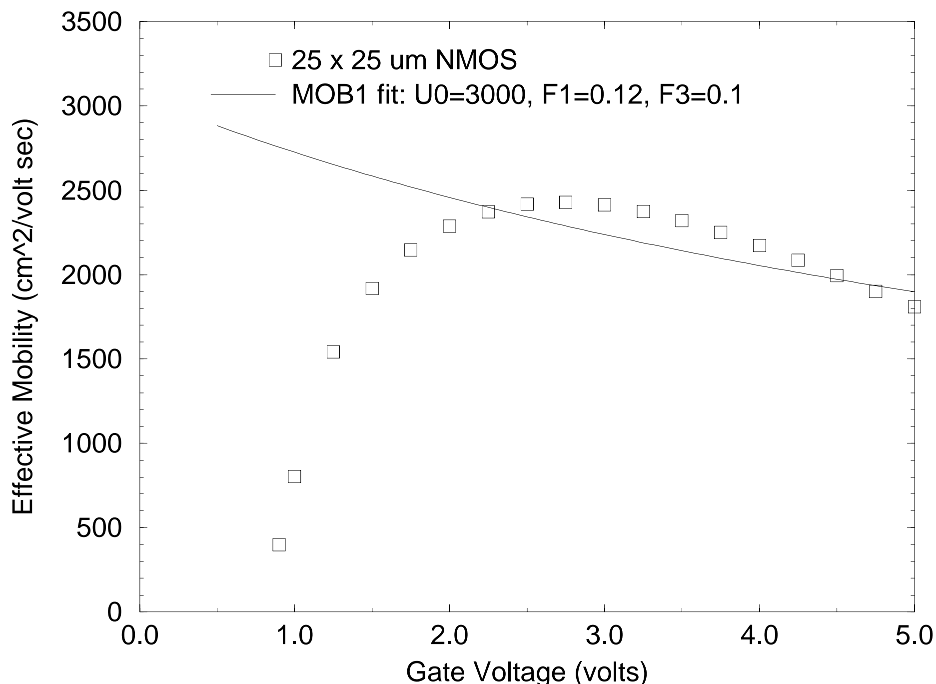

Figure 3.8: Effective mobility versus gate bias for a 25 x 25 μm NMOS device at 77 K. The 77 K electron mobility does not fit as well as at 300 K (see Figure 2.22).

down for better high gate bias fit, the current at lower gate biases will underapproximate the measurement results. Accidental stress during the 77 K measurements at high voltages and poor mobility modeling can be attributed to the poor fit at high V_{gs}. Figure 3.8 shows that the mobility does not fit well over the entire range of gate biases, just as at 300 K.

A poor fit at high gate biases in the I_{ds}-V_{ds} curves may not be a concern in the long run. Domains can be used to deal with the high gate biases, but due to the already high drive current at lower gate biases and the poorer reliability at low temperature, the power supply voltage at 77 K will most likely need to be scaled down to values well below 5 volts.

The I-V curves fit well near the target ring oscillator dimensions. Figure 3.9 shows the results for a 6 x 6 μm NMOS. I_{ds}-V_{ds} characteristics for the PMOS devices

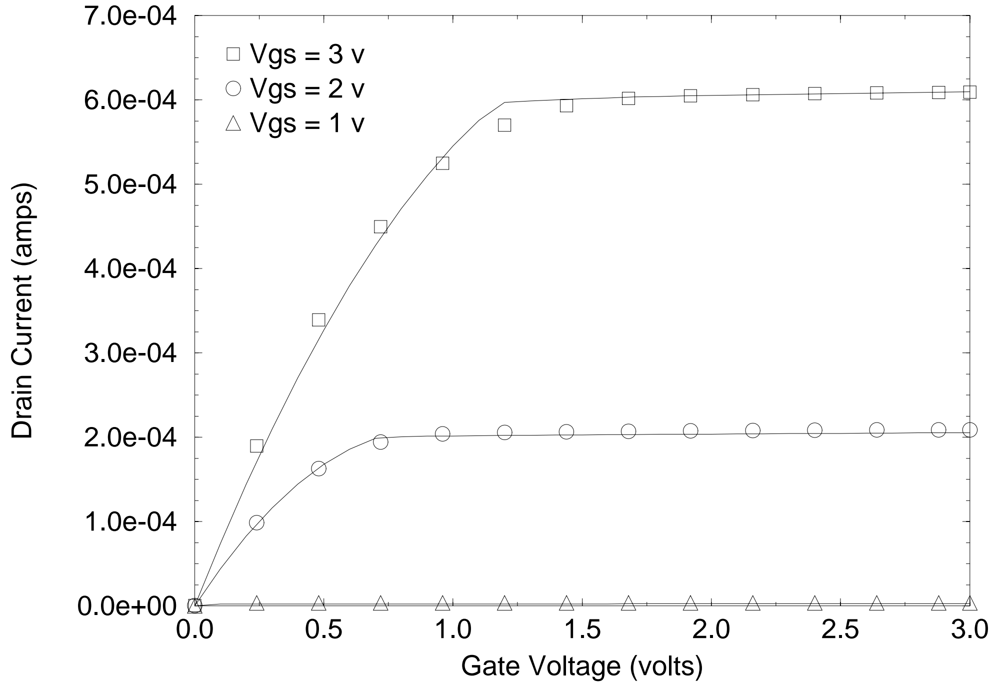

Figure 3.9: I_{ds}-V_{ds} curve for a 6 x 6 μm NMOS device at 77 K. Points indicate measurement data. Solid lines indicate HSPICE simulation results.

fitted well over all channel lengths and widths, showing much less of a saturation kink (due to the improved fit of μ_{eff} vs. V_{gs}).

3.3.3 Ring Oscillator Performance

Table 3.1 summarizes the ring oscillator structures which were measured at 77 K. The parasitic capacitances used in the simulation at 77 K were assumed to be the same as those at 300 K. The decrease in the capacitance at 77 K can be calculated using a parallel plate approximation.

$$C_{parasitic} = \frac{\epsilon_{si}}{W_{depl}} \tag{3.1}$$

Assuming that one side of the junction is heavily doped (and therefore has a negligible depletion width), W_{depl} is equal to the depletion width of the lighter

Number of Stages	PMOS W/L	NMOS W/L
41	6/2	6/2
23	6/1	6/1

Table 3.1: Ring Oscillators Measured at T = 77 K

doped junction.

$$W_{depl} = \sqrt{\frac{2\epsilon_{si} V_{bi}}{q N_{eff}}} \tag{3.2}$$

N_{eff} is the doping concentration (assumed to be uniform) and

$$V_{bi} = E_g/2 + \frac{kT}{q} \ln \frac{N_{eff}}{n_i} \tag{3.3}$$

where E_g is the energy gap and n_i is the intrinsic carrier concentration, both of which are temperature dependent.

W_{depl} at 300 K can be determined by plugging the 300 K parasitic capacitance into (3.1). N_{eff} can then be calculated analytically by substituting W_{depl} and (3.3) into (3.2). Then neglecting freeze-out effects, the same value of N_{eff} can be used to calculate $C_{parasitic}$ at 77 K. Since n_i decreases from 1.45 x 10^{-10} cm^3 at 300 K to about 6.8 x 10^{-21} cm^3 at 77 K, the capacitance is expected to decrease at lower temperatures. The change, however, has been calculated to be less than fifteen percent for the HP-MOSIS devices. Therefore, the 300 K parasitic capacitances were still used in the 77 K ring oscillator simulations.

Figure 3.10 shows the propagation delay versus power supply voltage for the 2 μm and 1 μm channel length ring oscillators. A very good fit has been obtained, even though the parasitic capacitances were not adjusted.

The improvement in ring oscillator performance at low temperature is only marginal. The 2 μm channel lengths have 2.3 times lower propagation delay, while

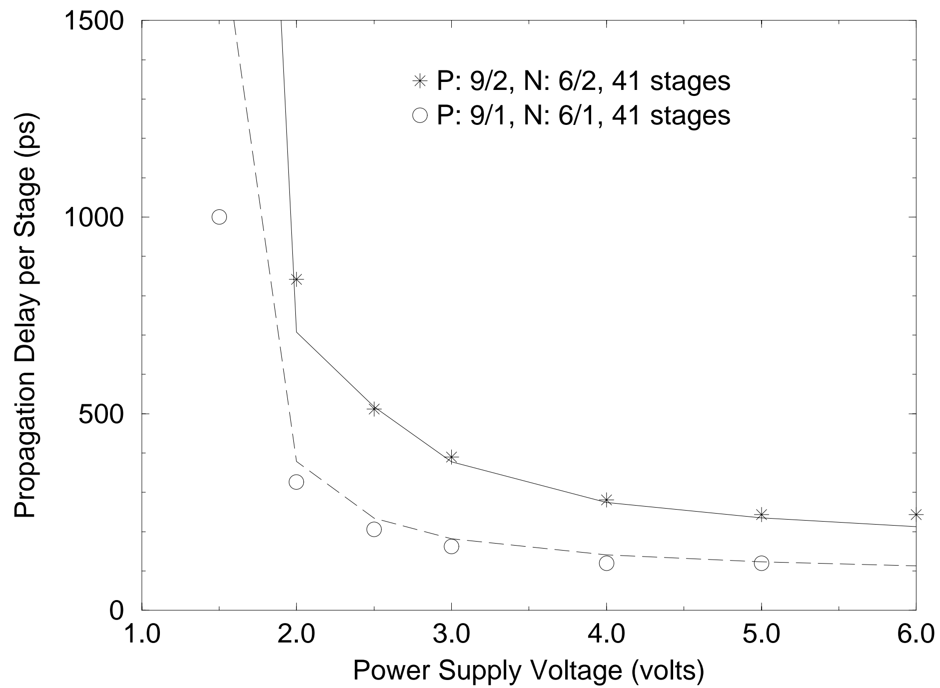

Figure 3.10: Propagation delay per stage versus power supply voltage of ring oscillators at 77 K. Points indicate measurement results. Lines indicate HSPICE simulation results (solid: 2 μm, dashed: 1 μm).

the 1 μm oscillators improve by a factor of only 1.5. Since the turn-on and turn-off times of an inverter are inversely proportional to the saturation current, the change in the maximum current drive, $I_{ds\,sat}$, from 300 K to 77 K can be attributed to the minor improvement. At 2 μm channel lengths, the saturation current increases by a factor of 2 at 77 K, but at 1 μm, the improvement is only 1.5. The increase in threshold voltage at 77 K limits the maximum current and improvement that can be obtained at low temperature.

3.4 Comparison with 300 K HSPICE Parameters

Table 3.2 summarizes the HSPICE parameters used for 300 K and 77 K simulations. Scaling factors of 1 μm were added using the .Option card (ScalM=1U, Scale=1U). Since the source/drain resistance changes with channel width, RSD and RSC must be adjusted for different channel widths. An approximate value can be obtained as follows.

$$R_{sd\,new} = R_{sd\,old}\frac{W_{eff\,old}}{W_{eff\,new}} \tag{3.4}$$

If transistors of those width dimensions are available, the I_{ds}-V_{gs} curves should be measured and compared with the simulation results to ensure that the values calculated in (3.4) are correct. This adjustment is not necessary if the number of "squares" that cover the source/drain area can be determined. However, the transistor layout must be inspected in order to determine this value.

Based on the changes in the HSPICE parameters from 300 K to 77 K, the following observations can be made regarding low temperature operation.

Parameter	NMOS 300 K	NMOS 77 K	PMOS 300 K	PMOS 77 K
LD	0.243	0.2	0.19	0.095
RSC	65	12.5	300	300
RDC	65	12.5	160	160
WD	0	0	0.25	0.25
VTO	0.68	0.89	-0.875	-1.33
VSH	0.15	0.05	0.25	0.3
FDS	0.275	0.2	0.25	0.06
GAMMA	0.35	0.62	0.518	0.51
PHI	0.352	0.62	0.371	0.55
NSUB	1.10e16	3.48e16	2.41e16	2.34e16
XJ	0.5	0.324	0.253	0.253
MOB	1	1	1	1
U0	650	3100	210	2000
F1	0.10	0.20	0.15	0.9
F3	0.225	0.05	0.35	0.4
WIC	1	1	1	1
NFS	3.3e11	5.0e10	1.0e11	1.0e11
CLM	1	1	1	1
LAMBDA	5.25e-6	7.00e-6	9.00e-6	1.30e-5
VMAX	6.25e6	8.50e6	4.00e6	4.80e6
TOX	200e-10	200e-10	200e-10	200e-10
CJBO	1.70e-15	1.70e-15	1.53e-15	1.53e-15
CJDO	1.74e-15	1.74e-15	1.23e-15	1.23e-15
CJSO	1.79e-15	1.79e-15	1.29e-15	1.29e-15
CJ	2.29e-16	2.29e-16	4.58e-16	4.58e-16
CJSW	7.57e-16	7.57e-16	1.16e-15	1.16e-15
SCM	5	0	0	0
NWE	0	0	0	0
NWM	0	0	0	0
TREF	27	27	27	27
TNOM (in .Option card)	27	27	27	27
.TEMP card	27	27	27	27

Table 3.2: Level 6 HSPICE parameters at 300 K and 77 K. NMOS channel width is 6 μm, and PMOS channel width is 9 μm.

- The effective channel length increases at lower temperatures. This effect may be attributed to the higher electric fields and therefore greater gate control near the edges of the channel region. Consequently, the source/drain resistance decreases at 77 K since more of the transistor is considered to be part of the channel.

- Threshold voltage (VTO) increases at lower temperature. This effect results primarily from the decrease in n_i [2]. Lighter channel implants can be used to readjust the threshold voltage. Lower doping levels in the channel will further improve the mobility.

- Mobility (UO) increases dramatically at 77 K, both for electrons (NMOS) and holes (PMOS). This is one of the most advantageous improvements of low temperature operation. Current drive increases as a result of the mobility enhancement.

- The saturation output conductance (LAMBDA) increases. Potentially higher current drive can be obtained as a result, although output resistance will decrease.

- Subthreshold current swing decreases. As a result, it is easier to turn the device off. Lower, more aggressive, threshold voltages can be used, allowing for higher current drive and possibly lower power supply voltages.

- Saturation velocity (VMAX) increases, which results in higher saturation currents.

3.5 Conclusion

The Level 6 HSPICE parameters have been extracted at 77 K. The same technique shown in Chapter 2 has been used, resulting in a reasonable fit in the I-V and circuit characteristics. Even though only the NMOS I-V curves have been shown here, the PMOS devices also exhibited a good fit.

The results presented for the HP-MOSIS devices demonstrate that simply cooling a device from 300 K down to 77 K will improve, but not maximize performance. Although mobility increases dramatically, allowing for higher current drive, the increase and instability of threshold voltage, and the lack of improvement in current drive are significant problems, especially at short channel lengths. Careful redesigning of the transistor profile, to correct for the increase in threshold voltage, to increase the mobility even further, and to prevent threshold voltage fluctuations, should help to further improve device performance at 77 K. However, power supply voltages will probably need to be reduced due to enhanced hot carrier degradation at low temperature.

Chapter 4

Extraction of the ate Dependent Source/Drain Resistance and Effective Channel Length

4.1 Introduction

As the channel length of MOSFETs decrease into the sub-micron range, the parasitic resistance of the source and drain regions becomes a greater limiting factor on device characteristics. Although current drive increases by scaling down to smaller channel lengths, the resistance outside of the channel does not scale down accordingly. The source-drain resistance will ultimiately limit the maximum current drive in a MOSFET. Therefore, it is important to accurately determine this value.

Numerous techniques have been presented on extracting the source/drain resistance, R_{sd}, along with the difference between the drawn channel length and the effective channel length, ΔL [10], [11], [17], [18]. The two quantities are coupled.

Increasing ΔL will increase R_{sd} since less of the entire MOS device is considered to be part of the channel. The extraction method in [11] was used in Chapters 2 and 3 to obtain R_{sd} and ΔL. Although good results were obtained for both parameters at 300 K, an effective channel length greater than the drawn length resulted at 77 K, as shown in Figure 3.1 of Chapter 3. Recently, several new extraction methods have been proposed which yield a positive ΔL's as well as a positive R_{sd} at 77 K [19], [20]. However, these methods are not very clear and do not consider the fact that both parameters are dependent on the gate bias.

The gate-dependence of R_{sd} and ΔL has been discussed in several papers [21], [22]. A $1/V_{gs}$ dependence is assumed, although in [22], ΔL was set to be constant. Both papers demonstrated a significant gate-depedence only in LDD devices. However, at low temperatures, a negative R_{sd} and ΔL are still obtained.

This chapter will demonstrate an inherent gate dependence in R_{sd} and ΔL through simulations on non-LDD devices. A current, commonly used extraction technique has been improved by assuming that both the source/drain resistance and the effective channel length vary with the gate bias. Simulation results on a variety of different doping profiles indicate the validity and usefulness of this method. A positive source/drain resistance and an effective channel length less than the drawn channel length are obtained at both room temperature and low temperature. More accurate extraction and HSPICE modeling of R_{sd} and ΔL is possible by including this gate dependence.

4.2 Extraction Technique

In the extraction method of [11], the total resistance of a MOSFET operating in the linear region at low drain bias is modeled as three resistors in series.

$$R_{tot} = R_{source} + R_{channel} + R_{drain} = R_{sd} + R_{channel} \tag{4.1}$$

R_{source} and R_{drain} are the external, parasitic resistances on each side of the MOSFET channel. $R_{channel}$ can be obtained by rearranging the I-V equation for the MOSFET in the linear regime.

$$R_{channel} = \frac{V_{ds}}{I_{ds}} = \frac{L_{eff}}{W_{eff}\mu_{eff}C_{ox}(V_{gs} - V_{th})} \tag{4.2}$$

The drain bias, V_{ds}, is assumed to be small. L_{eff} is the effective channel length and is equal to

$$L_{eff} = L_{drawn} - \Delta L \tag{4.3}$$

Based on the above equations, the source/drain resistance, R_{sd}, and ΔL can be obtained by plotting $1/g_d$ ($= V_{ds}/I_{ds}$) versus the drawn mask length for different gate biases above the threshold voltage, V_{th}. I_{ds}-V_{gs} characteristics at low drain bias of several transistors with equal width and varying length are used as data. Extrapolating the lines of constant $V_{gs}-V_{th}$ back, the x-coordinate of the intersection gives ΔL, and the y-coordinate is R_{sd}.

Figure 4.1 shows the results of applying this technique on an n-channel MOSFET at 300 K. A two dimensional device simulator, MEDICI [23], was used to simulate the I_{ds}-V_{gs} characteristics for channel lengths of 2, 3, 4, and 5 μm. Upon close inspection of the region near the intersection, it can be seen that the lines of constant $V_{gs} - V_{th}$ do not meet together at one point. This spreading results from the technique's

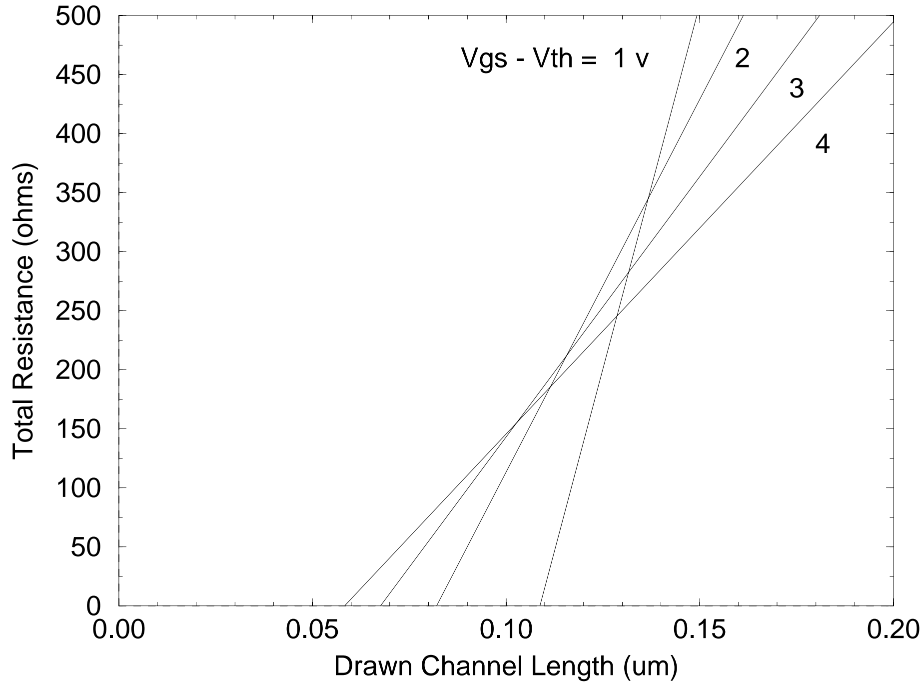

Figure 4.1: Total resistance versus drawn channel length for simulated NMOS devices at 300 K. Gate biases for each line are indicated on the figure. The lines of constant gate drive above the threshold voltage do not intersect together at a single point.

assumption that both R_{sd} and ΔL are constant and independent of gate bias. In actuality, as V_{gs} increases, a greater portion of the MOSFET will be inverted due to the higher electric fields near the edges of the channel region. As a result, ΔL and R_{sd} should decrease with increasing V_{gs}. This is verified in Figure 4.1 since the higher gate biases intersect at lower values of R_{sd} and ΔL.

For the same device at 77 K, the spreading of the intersection is similarly poor (see Figure 4.2). Due to the larger range of electric fields at low temperature, the gate has more control over the channel region, resulting in a lower R_{sd} and ΔL. However, ΔL is less than zero, which would seem to indicate that the effective channel length is longer than the drawn channel length! R_{sd} is near zero as well. Both of these values are physically impossible.

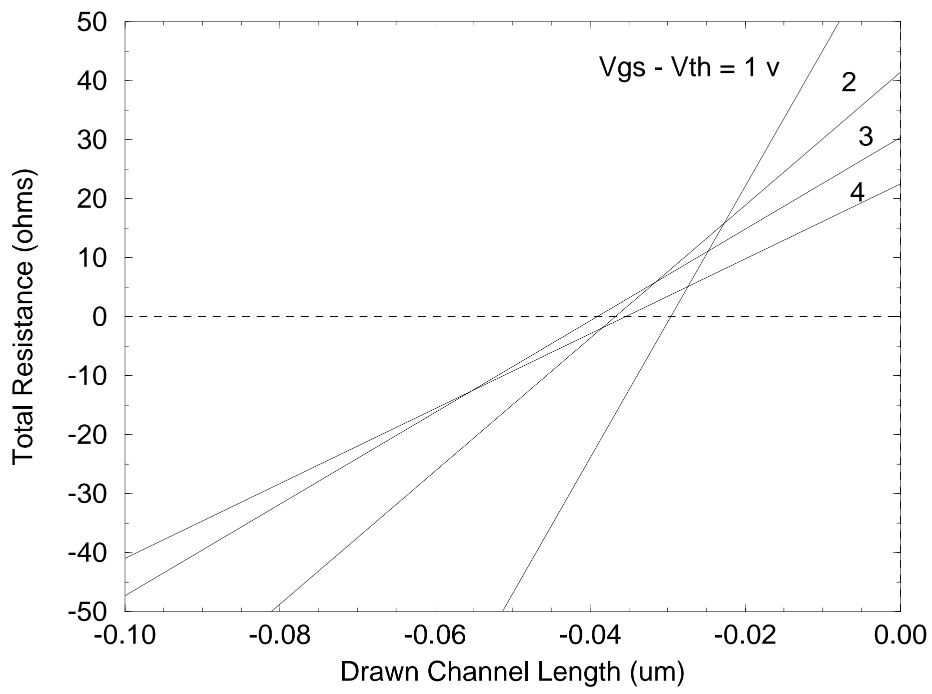

Figure 4.2: Total resistance versus drawn channel length for simulated NMOS devices at 77 K. Gate biases for each line are indicated on the figure. Just as at 300 K, the intersection is poor.

To incorporate a gate dependent R_{sd} and ΔL, a few modifications can be made in the extraction technique of [11]. Defining V'_{gs1} and V'_{gs2} as two different, but relatively close gate biases above the threshold voltage, equation (4.1) becomes

$$R_{tot} = R_{sd1} + \frac{L_{drawn} - \Delta L_1}{\mu_{eff} W C_{ox} V'_{gs1}} \tag{4.4}$$

$$R_{tot} = R_{sd2} + \frac{L_{drawn} - \Delta L_2}{\mu_{eff} W C_{ox} V'_{gs2}} \tag{4.5}$$

where $R_{sd1} = R_{sd}(V'_{gs1})$, $R_{sd2} = R_{sd}(V'_{gs2})$, $\Delta L_1 = \Delta L(V'_{gs1})$, $\Delta L_2 = \Delta L(V'_{gs2})$, $V'_{gs1} = V_{gs1} - V_{th}$, and $V'_{gs2} = V_{gs2} - V_{th}$. W_{eff} is approximately equal to W if long channel width devices are used.

The original extraction technique plots lines of constant V'_{gs} in a R_{tot} versus L_{drawn} plane. The intersection of any these lines gives R_{sd} (y-coordinate) and ΔL (x-coordinate). (4.4) and (4.5) each describe one of these lines. So defining the intersection point as (ΔL_{locus}, R_{locus}) and solving simultaneously, the results are

$$R_{locus} = R_{sd1} + V'_{gs2} \frac{R_{sd2} - R_{sd1}}{V'_{gs2} - V'_{gs1}} - \frac{1}{\mu_{eff} W C_{ox}} \frac{\Delta L_2 - \Delta L_1}{V'_{gs2} - V'_{gs1}} \tag{4.6}$$

$$\Delta L_{locus} = \Delta L_1 + \mu_{eff} W C_{ox} V'_{gs1} V'_{gs2} \frac{R_{sd2} - R_{sd1}}{V'_{gs2} - V'_{gs1}} - V'_{gs1} \frac{\Delta L_2 - \Delta L_1}{V'_{gs2} - V'_{gs1}} \tag{4.7}$$

It can be seen from Figures 4.1 and 4.2 that the values for R_{locus} and ΔL_{locus} will depend on which two lines are intersected. If V'_{gs1} is close enough to V'_{gs2}, the differences in R_{sd}, ΔL, and V'_{gs} can be replaced with differentials.

$$R_{locus} = R_{sd}(V'_{gs}) + V'_{gs} \frac{\partial R_{sd}}{\partial V_{gs}} - \frac{1}{\mu_{eff} W C_{ox}} \frac{\partial \Delta L}{\partial V_{gs}} \tag{4.8}$$

$$\Delta L_{locus} = \Delta L(V'_{gs}) + \mu_{eff} W C_{ox} V'^{2}_{gs} \frac{\partial R_{sd}}{\partial V_{gs}} - V'_{gs} \frac{\partial \Delta L}{\partial V_{gs}} \tag{4.9}$$

Assuming no gate dependence in R_{sd} or ΔL, the differentials in the above equations would drop out, yielding $R_{locus} = R_{sd}$ and $\Delta L_{locus} = \Delta L$, both of which are constant, as expected from [11].

$R_{sd}(V'_{gs})$ and $\Delta L(V'_{gs})$ can be obtained from equations (4.8) and (4.9) by curve fitting. This is done by first guessing what the gate dependency of R_{sd} and ΔL is (for example a $1/V_{gs}$ form as in [22] could be assumed). Then the right hand side of equations (4.8) and (4.9) can be evaluated and fitted to the R_{locus} and ΔL_{locus}.

To obtain R_{locus} and ΔL_{locus}, the "paried V_{gs}" method of [21] is used. Instead of intersecting all of the lines obtained from [11] together and obtaining a single R_{sd} and ΔL, adjacent lines of constant V'_{gs} $(= V_{gs} - V_{th})$ are intersected. The y-coordinate of each intersection point is R_{locus}, and the x-coordinate is ΔL_{locus}. Thus, a family of $R_{locus}(V_{gs})$ and $\Delta L_{locus}(V_{gs})$ points can be obtained. This technique should be reasonably accurate as long as the spacing between adjacent V'_{gs}'s is not large.

Equations (4.8) and (4.9) will remain valid as long as there is no variation of the mobility with gate bias. Otherwise, the independent variable V'_{gs} should be replaced by $\mu_{eff}V'_{gs}$ in equations (4.8) and (4.9) yielding

$$R_{locus} = R_{sd}(x) + x\frac{\partial R_{sd}}{\partial x} - \frac{1}{WC_{ox}}\frac{\partial \Delta L}{\partial x} \qquad (4.10)$$

$$\Delta L_{locus} = \Delta L(x) + WC_{ox}x^2\frac{\partial R_{sd}}{\partial x} - x\frac{\partial \Delta L}{\partial x} \qquad (4.11)$$

where $x = \mu_{eff}V_{gs}$. The resulting R_{sd} and ΔL are now functions of $\mu_{eff}V'_{gs}$. R_{locus} and ΔL_{locus} are still obtained using the "paired V_{gs}" method described above. However, these locus points should now be plotted as a function of $\mu_{eff}V_{gs}$. Since the slope of each line of constant $V_{gs}-V_{th}$ equals $1/\mu_{eff}C_{ox}(V_{gs}-V_{th})$, $\mu_{eff}V'_{gs}$ is obtained

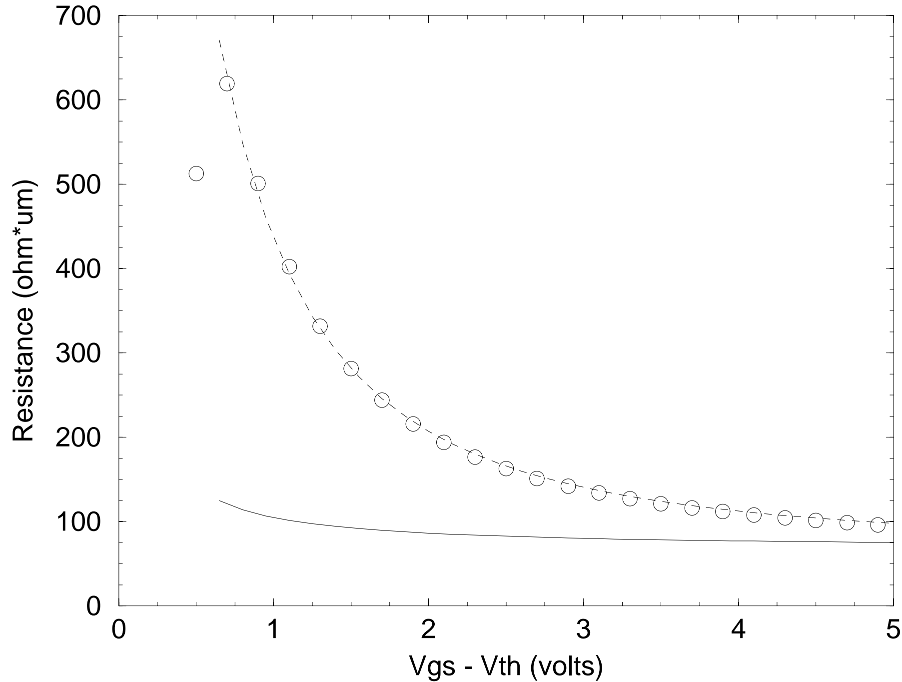

Figure 4.3: R_{locus} and R_{sd} versus $V_{gs}-V_{th}$ for an abrupt, uniform source/drain profile at 300 K. Mobility is independent of gate and drain biases. Locus points (obtained from simulation) are indicated with circles. The associate curve fit is the dotted line. The solid line is the extracted, gate dependent R_{sd}. $R_{sd} = 68 + 37/(V_{gs} - V_{th})$.

by first determining the average mobility from the slopes and then multiplying by the average gate bias.

4.3 Simulation Results and Discussion

Using MEDICI, R_{sd} and ΔL have been determined for several different transistor doping profiles. Figures 4.3 and 4.4 show the results for an abrupt, uniform source/drain profile. The source/drain junctions are located 0.2 μm underneath the gate. As a result, ΔL should be around 0.4 μm. In this particular simulation, the mobility was set to be independent of gate bias, so that equations (4.8) and (4.9) could be used.

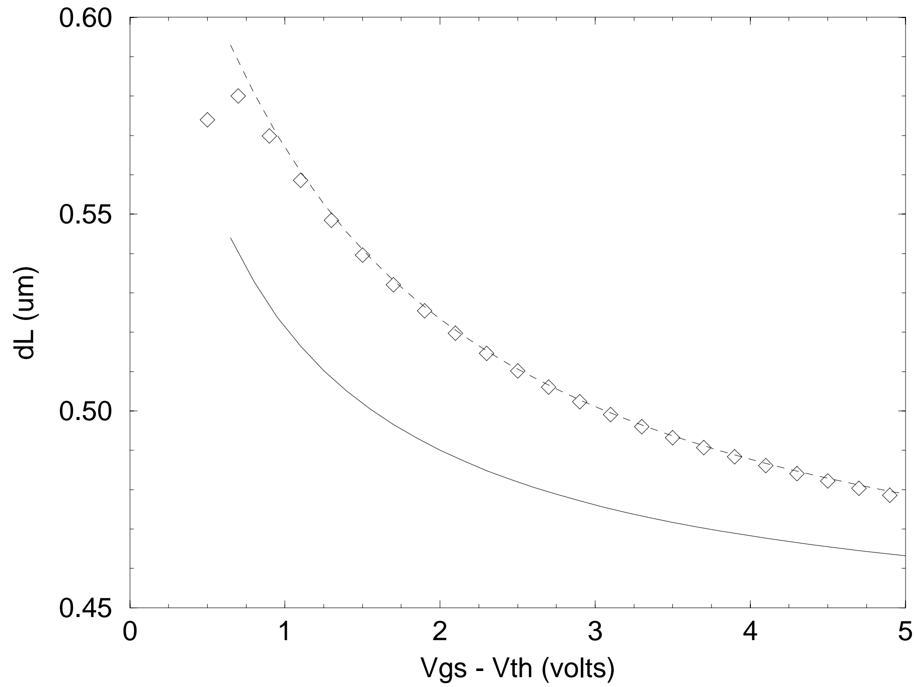

Figure 4.4: ΔL_{locus} and ΔL versus $V_{gs} - V_{th}$ for an abrupt, uniform source/drain profile at 300 K. Mobility is independent of gate and drain biases. Locus points (obtained from simulation) are indicated with diamonds. The associate curve fit is the dotted line. The solid line is the extracted, gate dependent ΔL.
$\Delta L = 0.44 + 0.13/(V_{gs} - V_{th} + 0.6)$.

A $1/V'_{gs}$ dependency in R_{sd} and ΔL [22] was used to fit the locus data. As expected, ΔL is about 0.4 μm. Both R_{sd} and ΔL remain relatively constant from moderate to high gate biases. The extremely abrupt junction between the source/drain and the channel here limits any additional inversion from occurring as the gate bias is increased. The rise in R_{sd} and ΔL at low gate biases is due to the fact that the transistor is only weakly turned on.

The results for a non-LDD, Gaussian source/drain profile at 300 K are shown in Figures 4.5 and 4.6. A lateral diffusion constant of 0.8 and an electric field dependent mobility were employed. As a result, the x-axis of both figures is now $\mu_{eff}V_{gs}$ instead of just V_{gs}. Equations (4.10) and (4.11) were used here. A $1/(x+a)$ dependency in both R_{sd} and ΔL was used to fit the locus data ($x \equiv \mu_{eff}(V_{gs}-V_{th})$). The "a" in the denominator corresponds to the point at which the locus data diverges. At 300 K, there is a greater dependence in R_{sd} than in the uniform, abrupt source/drain profile. ΔL remains about the same over the operating range of the device. Since the doping profile in the lateral direction changes more gradually here, the gate has a greater ability to invert portions of the channel near the source/drain junction. As a result, a significant gate dependence can be seen here in these non-LDD devices. Previous works have only shown gate dependencies in LDD devices [21], [22]. Simulations using an LDD profile yielded a similar, but stronger gate dependence in the locus data.

At 77 K, both R_{sd} and ΔL are lower than at room temperature, as indicated in Figures 4.7 and 4.8. This is due to the smaller source to channel potential [2], which allows the gate to have more control over a greater portion of the channel region near the source/drain edge. Both R_{sd} and ΔL are lower at 77 K for the

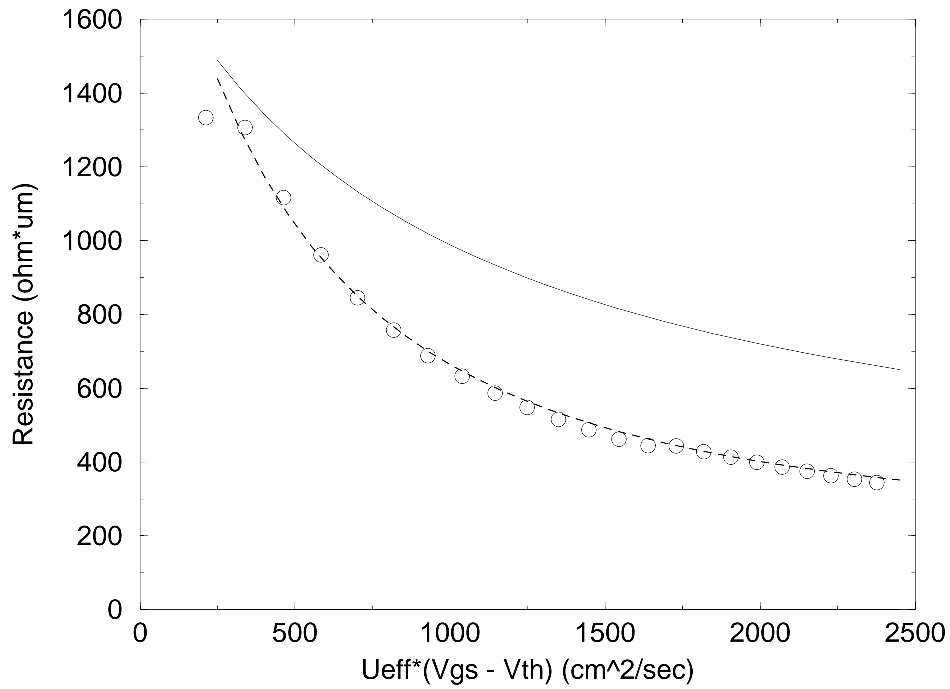

Figure 4.5: R_{locus} and R_{sd} versus $\mu_{eff}(V_{gs} - V_{th}$ for a Gaussian source/drain profile at 300 K. Locus points (obtained from simulation) are indicated with circles. The associate curve fit is the dotted line. The solid line is the extracted, gate dependent R_{sd}. $R_{sd} = 200 + 1.52e6/(x + 934)$, where $x = \mu_{eff}(V_{gs} - V_{th})$.

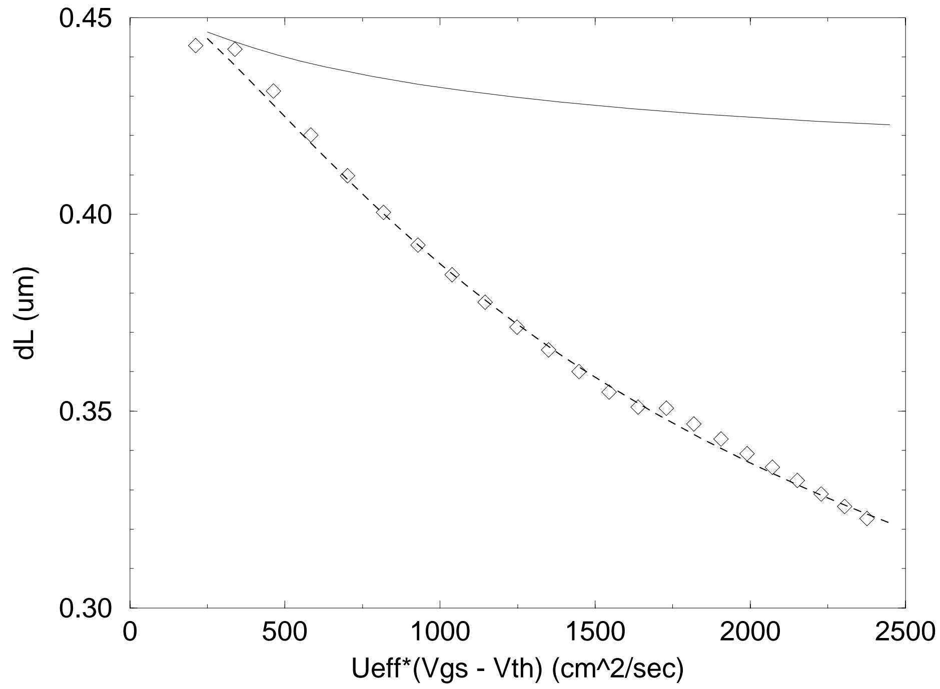

Figure 4.6: ΔL_{locus} and ΔL versus $\mu_{eff}(V_{gs}-V_{th})$ for a Gaussian source/drain profile at 300 K. Locus points (obtained from simulation) are indicated with diamonds. The associate curve fit is the dotted line. The solid line is the extracted, gate dependent ΔL. $\Delta L = 0.41 + 43/(x + 934)$, where $x = \mu_{eff}(V_{gs} - V_{th})$.

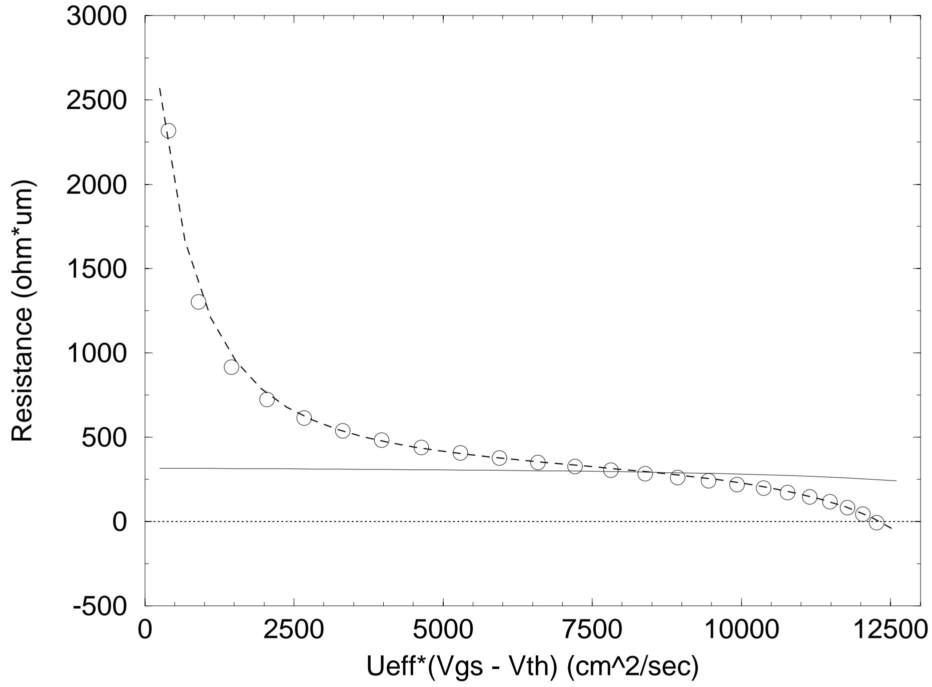

Figure 4.7: R_{locus} and R_{sd} versus $\mu_{eff}(V_{gs} - V_{th})$ for a Gaussian source/drain profile at 77 K. Locus points (obtained from simulation) are indicated with circles. The associate curve fit is the dotted line. The solid line is the extracted, gate dependent R_{sd}. $R_{sd} = 340 + 3.74e5/(x - 16400)$, where $x = \mu_{eff}(V_{gs} - V_{th})$.

uniform box profile as well. The low temperature locus data shows a greater gate dependence, which corresponds with the greater amount of spreading using the extraction of [11]. At high gate biases, the locus points are negative, but R_{sd} and ΔL remain positive using this technique. The average value for ΔL is close to the metallurgical junctions, which are located about 0.18 μm underneath the gate on each side. The overall trend of the locus data is significantly different at 77 K compared with 300 K because a greater range of $\mu_{eff} V'_{gs}$ is covered. In fact, there are singularity points near at both ends of the locus data.

Similar trends in R_{locus} and ΔL_{locus} were observed from experimental data at both 300 K and 77 K. Figures 4.9 and 4.10 show R_{locus} and ΔL_{locus} at 300 K and 77 K, respectively. Due to freezeout effects and fluctuations between devices, the

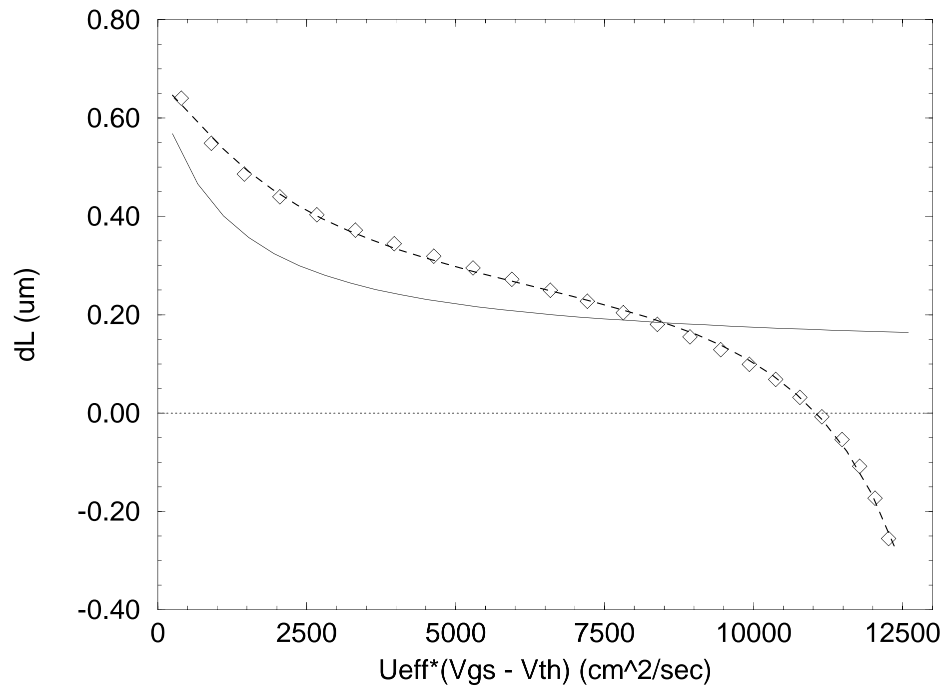

Figure 4.8: ΔL_{locus} and ΔL versus $\mu_{eff}(V_{gs} - V_{th})$ for a Gaussian source/drain profile at 77 K. Locus points (obtained from simulation) are indicated with diamonds. The associate curve fit is the dotted line. The solid line is the extracted, gate dependent ΔL. $\Delta L = 0.12 + 658/(x + 1200)$, where $x = \mu_{eff}(V_{gs} - V_{th})$.

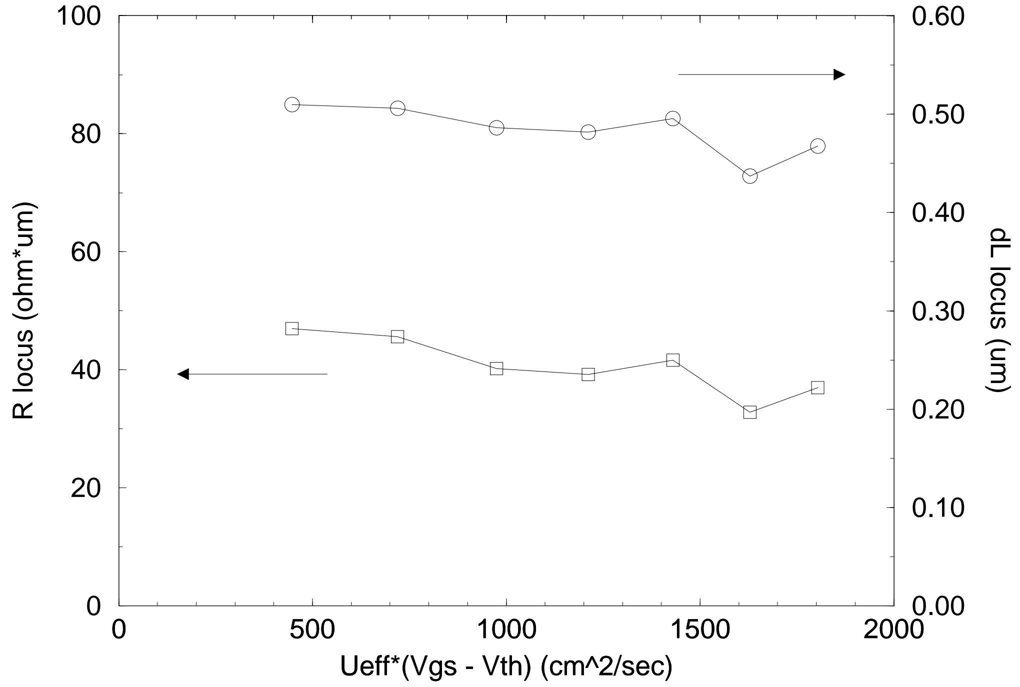

Figure 4.9: Measured R_{locus} and ΔL_{locus} versus $\mu_{eff}(V_{gs} - V_{th})$ at 300 K for the HP-MOSIS devices of Chapter 2. The locus points are not very smooth, but do exhibit a decreasing trend with gate bias.

experimental R_{locus} and ΔL_{locus} are not smooth, making it difficult to fit a curve to the data. Nevertheless, the trends are similar to the simulation results.

4.4 Conclusion

By incorporating a gate dependence in the source/drain resistance and effective channel length, a more physically meaningful extraction of these parameters in an MOS device can be performed. Both parameters have been given a gate dependence, rather than simplifying the problem by assuming that one or both of them are constant. The functional dependence for each parameter is arbitrary, although a $1/V_{gs}$ form has been commonly used. A polynomial function can be used to fit the locus data, but some of the physical meaning will be lost as a result. At low

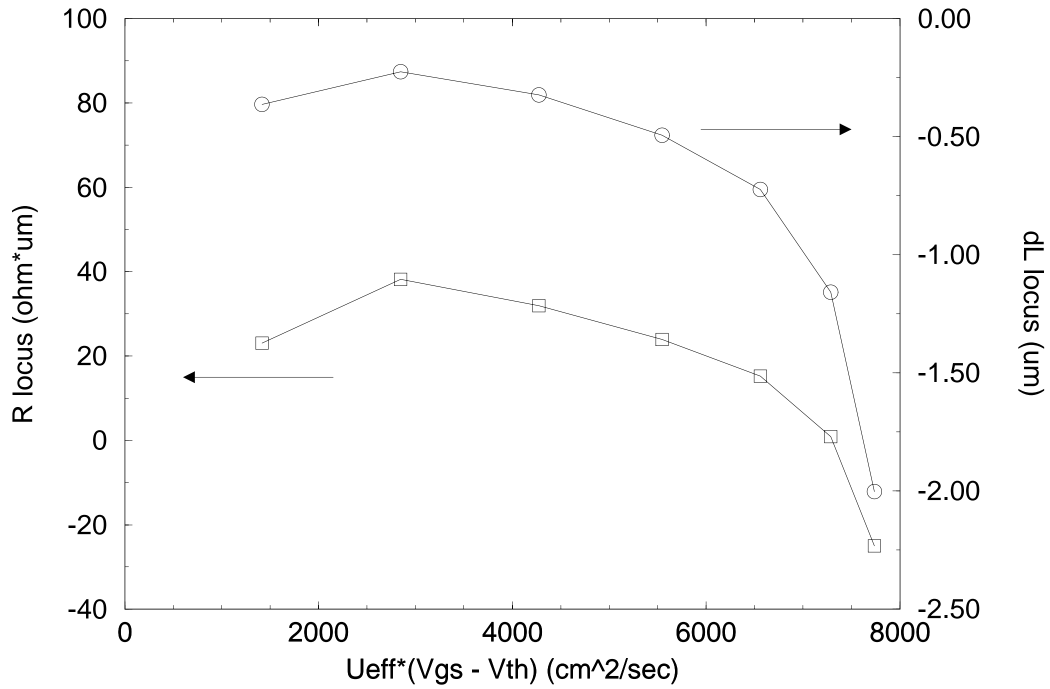

Figure 4.10: Measured R_{locus} and ΔL_{locus} versus $\mu_{eff}(V_{gs} - V_{th})$ at 77 K for the HP-MOSIS devices of Chapter 3. The locus points are not very smooth, but do exhibit a decreasing trend with gate bias, more so than at 300 K. ΔL_{locus} is negative over all gate biases here.

temperatures, this method can yield positive meaningful results for both R_{sd} and ΔL.

This technique is ultimately limited by the original modeling of the MOS device as simply three resistors in series. The transistion from the external source/drain to the channel is not completely abrupt. At the edges of the channel, the inversion charge is no longer equal to $C_{ox}(V_{gs} - V_{th})$. As a result, R_{ch}, which is based on the I_{ds}-V_{gs} equation and the assumption that the inversion charge is equal to the above relation, cannot be used to model the entire channel of an MOS device. Several papers have introduced additional resistances near the source/drain junction to account for this effect [24]-[26].

It is important to accurately determine both R_{sd} and ΔL, as these parameters will ultimately limit device performance. With some modifications of HSPICE, the gate dependence of both parameters can be included. This allows for more accurate modeling of R_{sd} and ΔL. The impact of this effect on overall circuit performance can also be evaluated.

Chapter 5

Conclusion

5.1 Summary

In order for low temperature CMOS to be applicable in the future, parameters characterizing its behavior at 77 K must be obtained. Circuits can then be designed and simulated before they are manufactured. This thesis has presented the steps required to extract the Level 6 HSPICE parameters at any given temperature. The general extraction principles and procedures shown here can be applied towards obtaining the parameters for any model of any circuit simulator. Good match to measured I-V and circuit characteristics has been demonstrated at both 300 K and 77 K.

By obtaining the HSPICE parameters at two or more different temperatures, the changes that occur in a device versus temperature can be noted. The impact on circuit performance can be clearly noted, since these are circuit level parameters. Using process simulation tools such as SUPREM [27], the transistor doping

profiles can be adjusted to compensate for the undesired changes due to temperature. Furthermore, these changes can help to optimize operation at the new target temperature. Then, plugging the profiles into two dimensional simulation programs such as MEDICI [23], I-V curves can be obtained. Thus, new HSPICE parameters can be extracted. Repeating the above steps over several cycles, one should be able to obtain an optimized CMOS device at 77 K.

Some of the problems in extracting the low temperature HSPICE parameters have been discussed. In particular, the source/drain resistance and effective channel length were dealt with at length. A new technique has been presented which assumes that both parameters are not fixed, but vary with the applied gate bias. Simulations have demonstrated the usefulness of this method, although it is more difficult to apply to measurement results.

5.2 Suggestions for Future Work

Even though this thesis can ultimately be used to obtain parameters for circuit simulation at 77 K, there are still a number of issues which need to be addressed. Below is a list of suggestions for future work.

- Device reliability at 77 K. Several papers have indicated that 77 K operation may worsen device lifetime [16], [28]-[29]. The power supply voltage may have to be scaled down to reduce the enhanced hot carrier degradation. Significant improvements in device performance will allow for this tradeoff.

- Optimized performance at 77 K. Ring oscillator results presented in this thesis indicated only a 2x improvement in circuit performance at 77 K versus 300 K.

The improvement worsens with scaling. Simply cooling an optimized 300 K device to 77 K will not better it by much. A 3x improvement is certainly possible [4]. Changes in device processing need to be determined to ensure maximum performance and also improved reliability. However, the proposed changes should remain compatible with current CMOS processing technology. Otherwise, the cost of converting to low temperature circuit manufacturing may be too expensive to be feasible. Intermediate temperatures between 300 K and 77 K should also be considered as possible operating regimes. By plotting HSPICE parameters as a function of temperature, the best temperature can be found with the least amount of processing changes ncessary.

- Resistance and effective channel length modeling at 77 K. It is still not well understood why standard extraction techniques for R_{sd} and ΔL fail at low temperatures. Development of an extraction technique for source/drain resistance which gives physically meaningful and accurate data over all temperatures is essential. With the trend towards sub-micron channel lengths, it will be essential to characterize source/drain resistance and find ways of reducing it. Low temperature operation may reduce the resistance, although the physical mechanisms behind it remain to be resolved.

- Mobility modeling. Improved mobility models at all temperatures will be needed for better fitting of simulation and measurement data. Below 300 K, significant changes in mobility behavior occur [30].

- Cooling technology at 77 K. Improvements have been made in refrigerated systems, but if low temperature electronics is to ever become a reality, reliable,

stable cooling systems are a necessity, especially if the devices are redesigned for optimal 77 K operation. Such circuits will not work properly if the environmental temperature around it is not maintained at 77 K.

Bibliography

[1] F.H. Gaensslen, V.L. Rideout, E.J. Walker, and J.J. Walker, "Very Small MOSFET's for Low-Temperature Operation", *IEEE Trans. on Electron Devices*, vol. ED-24, p. 218-229, 1977.

[2] Jason C.S. Woo and J.D. Plummer, "Short-Channel Effects in MOSFET's at Liquid-Nitrogen Temperature", *IEEE Trans. on Electron Devices*, vol. ED-33, p. 1012-1018, 1986.

[3] Jack Y.C. Sun, Y. Taur, R.H. Dennard, and S.P. Klepner, "Submicrometer-Channel CMOS for Low-Temperature Operation", *IEEE Trans. on Electron Devices*, vol. ED-34, p. 19-26, 1987.

[4] M. Aoki, S. Hanamura, T. Masuhara, and K. Yano, "Performance and Hot-Carrier Effects of Small CRYO-CMOS Devices", *IEEE Trans. on Electron Devices*, vol. ED-34, p. 8-17, 1987.

[5] M. Kakumu, D. Peters, H.Y. Liu, and K.Y. Chiu, "Design Optimization for Deep-Submicron CMOS Device at Low Temperature Operation", *IEDM Tech. Digest*, p. 211-214, 1990.

[6] B. Johnson, T. Quarles, A.R. Newton, D.O. Pederson, A. Sangiovanni-Vincentelli, “Spice3 Version 3D2 User's Manual”, *Department of Electrical Engineering and Computer Sciences, University of California, Berkeley*, 1990.

[7] “HSPICE User's Manual (version h92b.01)”, *Meta-Software, Inc.*, 1992.

[8] B.J. Sheu, D.L. Scharfetter, P.K. Ko, and M.C. Jeng, “BSIM: Berkeley Short-Channel IGFET Model for MOS Transistors”, *IEEE Journal of Solid-State Circuits*, vol. SC-22, p. 558-566, 1987.

[9] J.S. Duster, M.C. Jeng, P.K. Ko, and C. Hu, “User's Guide for the BSIM2 Parameter Extraction Program and the SPICE3 with BSIM Implementation”, *Industrial Liaison Program, Software Distribution Office, University of California, Berkeley*, 1990.

[10] K.K. Ng and J.R. Brews, “Measuring the Effective Channel Length of MOSFETs”, *IEEE Circuits and Devices*, vol. 6, p. 33-38, 1990.

[11] J.G.J. Chern, P. Change, R.F. Motta, and N. Godinho, “A New Method to Determine MOSFET Channel Length”, *IEEE Electron Device Letters*, vol. EDL-1, p. 170-173, 1980.

[12] R.R. Troutman, “VLSI Limitations from Drain-Induced Barrier Lowering”, *IEEE Journal of Solid-State Circuits*, vol. SC-14, p. 383-391, 1979.

[13] S.C. Sun and J.D. Plummer, “Electron Mobility in Inversion and Accumulation Laysers on Thermally Oxidized Silicon Surfaces”, *IEEE Trans. on Electron Devices*, vol. ED-27, p. 1497-1508, 1980.

[14] J.T.C. Chen and R.S. Nuller, “Carrier Mobilites at Weakly Inverted Silicon Surfaces”, *Journal of Applied Physics*, vol. 45, p. 828, 1974.

[15] E.H. Nicollian and J.R. Brews, *MOS (Metal Oxide Semiconductor) Physics and Technology*, 1982.

[16] M. Song, K.P. MacWilliams, J.S. Cable, and Jason C.S. Woo, “Bias and Temperature Dependence of Hot Carrier Lifetime from 77 K to 300 K”, *IEDM Tech. Digest*, p. 707-710, 1992.

[17] M.H. Seavey, “Source and Drain Resistance Determination for MOSFET‘s”, *IEEE Electron Device Letters*, vol. EDL-5, p. 479-481, 1984.

[18] P.I. Suciu and R.L. Johnston, “Experimental Derivation of the Source and Drain Resistance of MOS Transistors”, *IEEE Trans. on Electron Devices*, vol. ED-27, p. 1846-1848, 1980.

[19] A. Emrani, G. Ghibaudo, and F. Balestra, “Generalised Method for Extraction of Source-Drain Series Resistance Against Temperature”, *Electronics Letters*, vol. 29, p. 786-788, 1993.

[20] Y. Taur, D.S. Zicherman, D.R. Lombardi, P.J. Restle, C.H. Hsu, H.I. Hanafi, M.R. Wordeman, B. Davari, and G.G. Shahidi, “A New 'Shift and Ratio' Method for MOSFET Channel-Length Extraction, *IEEE Electron Device Letters*, vol. EDL-13, p. 267-269, 1992.

[21] G.J. Hu, C. Chang, and Y.T. Chia, “Gate-Voltage-Dependent Effective Channel Length and Series Resistance of LDD MOSFET's”, *IEEE Trans. on Electron Devices*, vol. ED-34, p. 2469-2474, 1987.

[22] B.J. Sheu, C. Hu, P.K. Ko, and F.C. Hsu, "Source-and-Drain Series Resistance of LDD MOSFETs", *IEEE Electron Device Letters*, vol. EDL-5, p. 365-367, 1984.

[23] "TMA MEDICI: Two-Dimensional Device Simulation Program (version 1.1.3)", *Technology Modeling Associates, Inc.*.

[24] K.K. Ng and W.T. Lynch, "The Impact of Intrinsic Series Resistance on MOSFET Scaling", *IEEE Trans. on Electron Devices*, vol. ED-34, p. 503-511, 1987.

[25] K.K. Ng and W.T. Lynch, "Analysis of the Gate-Voltage-Dependent Series Resistance of MOSFET's", *IEEE Trans. on Electron Devices*, vol. ED-33, p. 965-972, 1986.

[26] K.K. Ng, R.J. Bayruns, and S.C. Fang, "The Spreading Resistance of MOSFET's", *IEEE Electron Device Letters*, vol. EDL-6, p. 195-198, 1985.

[27] S.E. Hansen, "Suprem-III User's Manual, Version 8520", *Board of Trustees of Stanford University*, 1985.

[28] J.J. Tzou, C.C. Yao, R. Cheung, and H. Chan, "Hot-Electron-Induced MOSFET Degradation at Low Temperatures", *IEEE Electron Device Letters*, vol. EDL-6, p. 450-452, 1985.

[29] M. Song, J.S. Cable, Jason C.S. Woo, and K.P. MacWilliams, "Optimization of LDD Devices for Cryogenic Operation", *IEEE Electron Device Letters*, vol. EDL-12, p. 375-377, 1991.

[30] A. Hairapetian, D. Gitlin, and C.R. Viswanathan, “Low-Temperature Mobility Measurements on CMOS Devices”, *IEEE Trans. on Electron Devices*, vol. ED-36, p. 1448-1455, 1989.