Briefs

Extraction of Gate Dependent Source/Drain Resistance and Effective Channel Length in MOS Devices at 77 K

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***Abstract*— A new extraction technique for obtaining the parasitic source/drain resistance and the effective channel length of an MOS device at 77 K is presented. Unlike previous methods, both parameters are assumed to vary with the gate voltage. This results in positive and physically meaningful results at any temperature. Simulation results show that, in non-LDD devices, the source/drain resistance decreases and the effective channel length increases with gate bias, indicating that the gate dependence of both parameters is inherent to MOS devices.**

I. Introduction

As the minimum channel length of MOSFET's decreases into the sub-micron range, the parasitic resistance of the source and drain regions becomes a greater limiting factor on device characteristics. Although current drive can be increased by scaling down the channel length, the resistance outside of the channel will not scale down accordingly. As a result, the source/drain resistance will ultimately limit the maximum current level in a MOSFET.

By operating the device at low temperature, current drive and overall device performance can be improved [1], offsetting the resistance limitation. However, a negative source/drain resistance and an effective channel length greater than the drawn length are always obtained using any of the standard extraction techniques [2]–[5]. Accurate determination of a physically meaningful parasitic resistance at low temperature is essential if cooling is to be used to improve device performance.

In this paper, an extraction technique is presented in which both the source/drain resistance and effective channel length are assumed to be dependent on the gate bias. MEDICI simulation results on several different doping profiles demonstrate the validity of our method. A positive source/drain resistance and an effective channel length less than the drawn channel length can be seen at both room temperature and low temperature. The gate dependence of both parameters will be shown for non-LDD MOSFET's, indicating that gate dependent parasitic resistance is inherent to MOSFET's.

II. Extraction Technique

The total resistance of a MOSFET is often modeled as three resistors in series.

$$R_{\rm tot} = R_{\rm source} + R_{\rm drain} + R_{\rm channel} = R_{\rm sd} + \frac{L_{\rm eff}}{W_{\rm eff}\mu_{\rm eff}C_{\rm ox}(V_{\rm gs} - V_{\rm th}).} \quad (1)$$

$R_{\rm sd}$ $(= R_{\rm source} + R_{\rm drain})$ is the total external, parasitic resistance on each side of the MOSFET. $L_{\rm eff}$ is the effective channel length and is equal to $L_{\rm drawn} - \Delta L$. $R_{\rm channel}$ $(= V_{\rm ds}/I_{\rm ds})$ has been replaced by the linear $I_{\rm ds}$-$V_{\rm gs}$ equation for the MOSFET at low drain bias.

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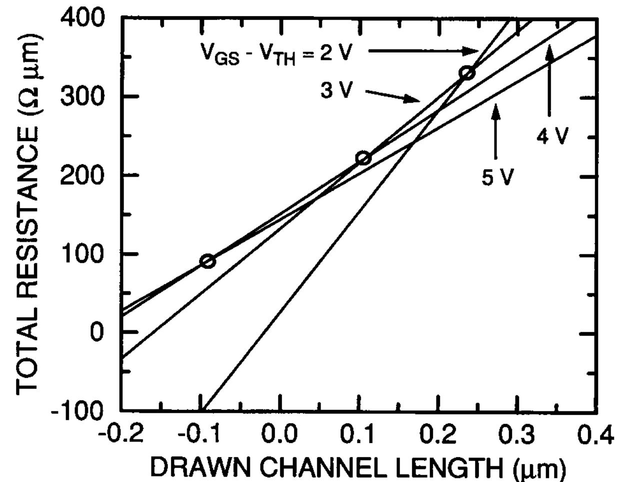

Fig. 1. Total resistance versus drawn channel length of a MOSFET at 77 K. Oxide thickness is 150 Å. The doping profile is a Gaussian source/drain with lateral diffusion of 0.8. The lines of constant $V_{\rm gs} - V_{\rm th}$ (2, 3, 4, and 5 volts) have been extrapolated back from simulation of 2 μm, 3 μm, 4 μm, and 5 μm NMOSFET's. The circles indicate where adjacent lines of constant $V_{\rm gs} - V_{\rm th}$ meet up.

The extraction method of [2] utilizes (1) by intersecting lines of constant $V_{\rm gs} - V_{\rm th}$ in a $R_{\rm tot}$ $(= V_{\rm ds}/I_{\rm ds})$ versus $L_{\rm drawn}$ plane. Fig. 1 shows the results of applying our technique on a simulated, Gaussian source/drain n-channel MOSFET at 77 K. Note that the lines do not intersect at one point, making it difficult to determine $R_{\rm sd}$ (the y-coordinate of the intersection) and ΔL (the x-coordinate). In fact, ΔL can be less than zero, indicating that the effective channel length is longer than the drawn channel length. At 300 K, the intersection is closer, but still not exact. Negative results at 77 K almost always occur if other extraction techniques are used [3]–[5].

The error in determining $R_{\rm sd}$ and ΔL using any of the aforementioned techniques results from the assumption that one or both of the parameters are independent of gate bias. In actuality, as $V_{\rm gs}$ increases, $R_{\rm sd}$ and ΔL should decrease since a greater portion of the channel region can be modulated and inverted by the higher gate bias. At lower temperatures, the vertical electric fields increase, especially near the source/drain junctions. This gives the gate greater control over the channel, leading to a stronger dependence of $R_{\rm sd}$ and ΔL versus gate bias.

A gate dependent $R_{\rm sd}$ and ΔL can be incorporated into (1), leading to positive results at 77 K. For two different, but relatively close, gate biases above the threshold voltage, $V'_{\rm gs1}$ and $V'_{\rm gs2}$, we have

$$R_{\rm tot} = R_{\rm sd1} + \frac{L_{\rm drawn} - \Delta L_1}{\mu_{\rm eff} W C_{\rm ox} V'_{\rm gs1}} \quad (2)$$

$$R_{\rm tot} = R_{\rm sd2} + \frac{L_{\rm drawn} - \Delta L_2}{\mu_{\rm eff} W C_{\rm ox} V'_{\rm gs2}} \quad (3)$$

where $R_{\rm sd1} = R_{\rm sd}(V'_{\rm gs1})$, $R_{\rm sd2} = R_{\rm sd}(V'_{\rm gs2})$, $\Delta L_1 = \Delta L(V'_{\rm gs1})$, $\Delta L_2 = \Delta L(V'_{\rm gs2})$, $V'_{\rm gs1} = V_{\rm gs1} - V_{\rm th}$, and $V'_{\rm gs2} = V_{\rm gs2} - V_{\rm th}$. $W_{\rm eff}$ is approximately equal to W if long channel width devices are used.

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Equations (2) and (3) each define a line in the L_{drawn}-R_{tot} plane. The intersection point of these two lines, defined here as $(\Delta L_{\text{locus}}, R_{\text{locus}})$, can be obtained by solving (2) and (3) simultaneously yielding

$$R_{\text{locus}} = R_{\text{sd1}} + V'_{\text{gs2}} \frac{R_{\text{sd2}} - R_{\text{sd1}}}{V'_{\text{gs2}} - V'_{\text{gs1}}} - \frac{1}{\mu_{\text{eff}} W C_{\text{ox}}} \frac{\Delta L_2 - \Delta L_1}{V'_{\text{gs2}} - V'_{\text{gs1}}} \quad (4)$$

$$\Delta L_{\text{locus}} = \Delta L_1 + \mu_{\text{eff}} W C_{\text{ox}} V'_{\text{gs1}} V'_{\text{gs2}} \times \frac{R_{\text{sd2}} - R_{\text{sd1}}}{V'_{\text{gs2}} - V'_{\text{gs1}}} - V'_{\text{gs1}} \frac{\Delta L_2 - \Delta L_1}{V'_{\text{gs2}} - V'_{\text{gs1}}}. \quad (5)$$

If V'_{gs1} is close enough to V'_{gs2}, the differences in R_{sd}, ΔL, and V'_{gs} can be replaced with differentials:

$$R_{\text{locus}} = R_{\text{sd}}(V'_{\text{gs}}) + V'_{\text{gs}} \frac{\partial R_{\text{sd}}}{\partial V_{\text{gs}}} - \frac{1}{\mu_{\text{eff}} W C_{\text{ox}}} \frac{\partial \Delta L}{\partial V_{\text{gs}}} \quad (6)$$

$$\Delta L_{\text{locus}} = \Delta L(V'_{\text{gs}}) + \mu_{\text{eff}} W C_{\text{ox}} V'^2_{\text{gs}} \frac{\partial R_{\text{sd}}}{\partial V_{\text{gs}}} - V'_{\text{gs}} \frac{\partial \Delta L}{\partial V_{\text{gs}}}. \quad (7)$$

Note that R_{locus} and ΔL_{locus} reduce to a single R_{sd} and ΔL (i.e., the results in [2]) if no gate dependence in either parameter is assumed. However, our extraction technique goes one step further than [2] by assuming a gate dependence in both parameters. A series of gate dependent R_{locus} and ΔL_{locus} points will be generated and curve fitted to yield $R_{\text{sd}}(V'_{\text{gs}})$ and $\Delta L(V'_{\text{gs}})$. In order to achieve this, a functional gate dependency will be first assumed for R_{sd} and ΔL. Then, the right hand side of (6) and (7) can be evaluated and fitted to R_{locus} and ΔL_{locus} (the left hand side of the equations).

To obtain R_{locus} and ΔL_{locus}, the method in [6] is used. Adjacent lines of constant V'_{gs} $(= V_{\text{gs}} - V_{\text{th}})$ are intersected, resulting in a family of $R_{\text{locus}}(V'_{\text{gs}})$ and $\Delta L_{\text{locus}}(V'_{\text{gs}})$ points. The technique above should be reasonably accurate as long as the spacing between adjacent V'_{gs}'s is not large. Note that in [6], the locus points were assumed to be equal to R_{sd} and ΔL. Their assumption holds only if the gate dependence is minimal. Our technique does not directly equate the locus data to R_{sd} and ΔL. In fact, our resulting R_{sd} and ΔL do not show exactly the same gate dependence as the locus points.

To incorporate a gate dependent mobility into the extraction, the independent variable V'_{gs} is replaced by $\mu_{\text{eff}} V'_{\text{gs}}$ in (6) and (7). The resulting R_{sd} and ΔL become functions of $\mu_{\text{eff}} V'_{\text{gs}}$. The locus points are still determined as described above. Since the slope of each line of constant $V_{\text{gs}} - V_{\text{th}}$ equals $1/\mu_{\text{eff}} C_{\text{ox}}(V_{\text{gs}} - V_{\text{th}})$, $\mu_{\text{eff}} V'_{\text{gs}}$ can be obtained by averaging the slopes.

III. Simulation Results and Discussion

Using MEDICI [8], R_{sd} and ΔL has been determined for two different non-LDD, source/drain profiles. Fig. 2 shows the results for a uniform source/drain profile at 300 K. Abrupt junctions were placed 0.2 μm underneath the gate on each side. In this particular simulation, the mobility was set to be independent of the gate bias, so that (6) and (7) could be used directly. A $1/(V_{\text{gs}} + a)$ dependency [7] in both R_{sd} and ΔL was used to fit the locus data. The "a" in the denominator roughly corresponds with the point at which the locus data diverges. The extracted ΔL is reasonably close to the expected value of 0.4 μm.

Fig. 3 shows the results for the same profile at 77 K. R_{sd} and ΔL decrease only slightly at low temperature. Although the vertical electric fields are higher and the source-to-channel potential is lower at low temperature [9], the extremely abrupt junction between the source/drain and the channel limits the amount of channel modulation that can occur. It is important to note that, at both 300 K and 77 K, the locus points and the final forms of R_{sd} and ΔL are very different from each other. This contradicts the extraction method of [6], which assumed that they were identical.

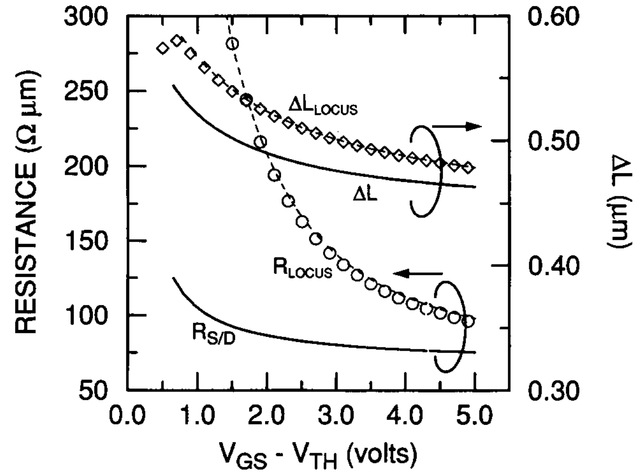

Fig. 2. R_{locus}, R_{sd}, ΔL_{locus}, and ΔL at 300 K for a uniform source/drain profile. Oxide thickness is 150 Å. Metallurgical junctions occur 0.2 μm underneath the gate on each side. Mobility is independent of gate and drain biases in this example (μ_n = 650 cm²/V sec and μ_p = 350 cm²/V sec). Locus points (obtained from simulation) are indicated with circles and diamonds. Associated curve fits are shown with dotted lines. The solid lines are the extracted R_{sd} and ΔL. $R_{\text{sd}} = 68 + 37/(V_{\text{gs}} - V_{\text{th}})$ and $\Delta L = 0.44 + 0.13/(V_{\text{gs}} - V_{\text{th}} + 0.6)$.

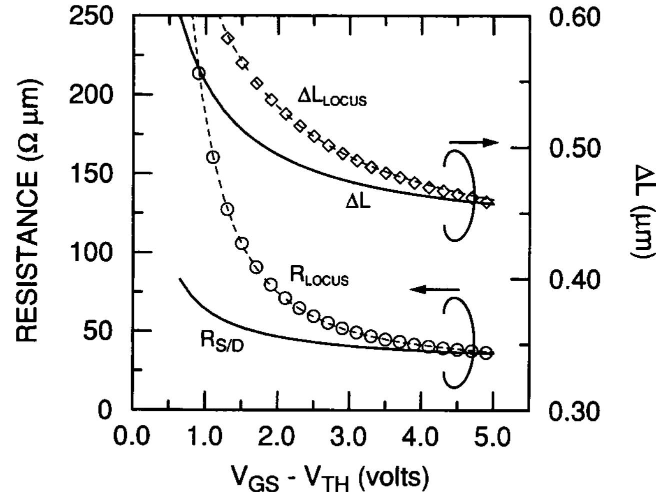

Fig. 3. R_{locus}, R_{sd}, ΔL_{locus}, and ΔL at 77 K for a uniform source/drain profile. Oxide thickness is 150 Å. Metallurgical junctions occur 0.2 μm underneath the gate on each side. Mobility is independent of gate and drain biases in this example (μ_n = 650 cm²/V sec and μ_p = 350 cm²/V sec). Locus points (obtained from simulation) are indicated with circles and diamonds. Associated curve fits are shown with dotted lines. The solid lines are the extracted R_{sd} and ΔL. $R_{\text{sd}} = 29 + 35/(V_{\text{gs}} - V_{\text{th}})$ and $\Delta L = 0.43 + 0.14/(V_{\text{gs}} - V_{\text{th}} + 0.18)$.

Figs. 4 and 5 show the 300 K and 77 K results for a non-LDD, Gaussian source/drain profile. A lateral diffusion constant of 0.8 and an electric field dependent mobility were employed. The latter results in the x-axis being $\mu_{\text{eff}}(V_{\text{gs}} - V_{\text{th}})$. Due to the more gradual change in doping from the channel to the source/drain regions, there is a stronger gate dependence in both R_{sd} and ΔL. The overall trend of

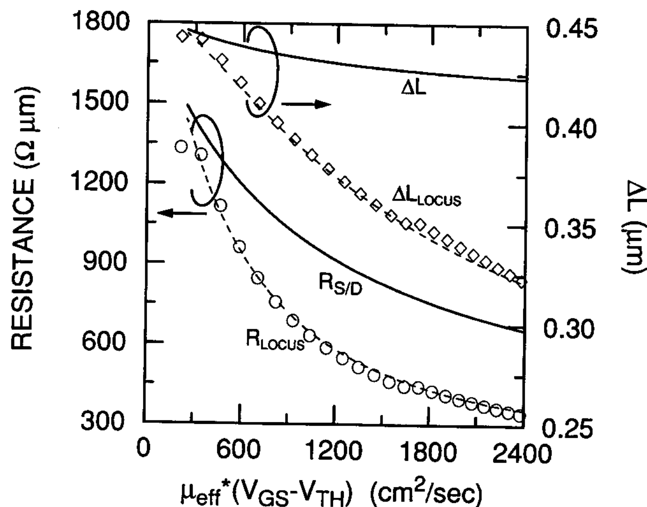

Fig. 4. $R_{\rm locus}$, $R_{\rm sd}$, $\Delta L_{\rm locus}$, and ΔL at 300 K for a Gaussian S/D profile. Oxide thickness is 150 Å. The metallurgical junctions occur 0.18 μm underneath the gate on each side. Locus points (obtained from simulation) are indicated with circles and diamonds. Associated curve fits are shown with dotted lines. The solid lines are the extracted $R_{\rm sd}$ and ΔL. $R_{\rm sd} = 200 + 1.52e6/(x + 934)$ and $\Delta L = 0.41 + 43/(x + 934)$, where $x = \mu_{\rm eff}(V_{\rm gs} - V_{\rm th})$.

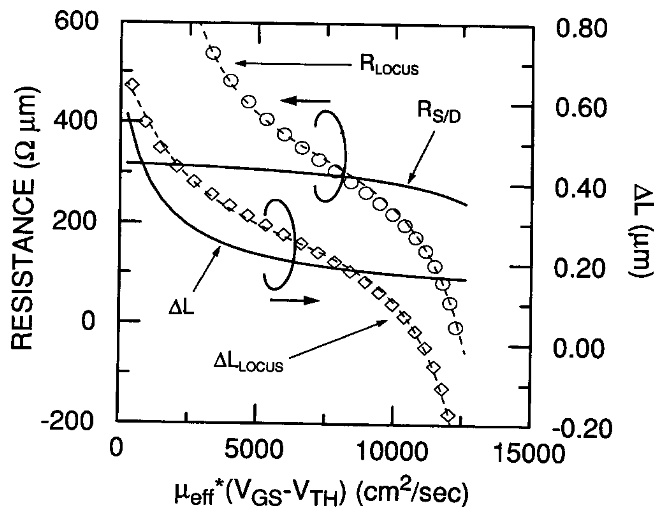

Fig. 5. $R_{\rm locus}$, $R_{\rm sd}$, $\Delta L_{\rm locus}$, and ΔL at 77 K for a Gaussian S/D profile. Oxide thickness is 150 Å. The metallurgical junctions occur 0.18 μm underneath the gate on each side. Locus points (obtained from simulation) are indicated with circles and diamonds. Associated curve fits are shown with dotted lines. The solid lines are the extracted $R_{\rm sd}$ and ΔL. $R_{\rm sd} = 340 + 3.74e5/(x - 16400)$ and $\Delta L = 0.12 + 658/(x + 1200)$ where $x = \mu_{\rm eff}(V_{\rm gs} - V_{\rm th})$.

the locus data is significantly different at 77 K than at 300 K because a greater range of $\mu_{\rm eff} V'_{\rm gs}$ is covered. In fact, there are singularity points near at both ends of the 77 K locus data.

For the 77 K case at high gate biases, both $R_{\rm locus}$ and $\Delta L_{\rm locus}$ are negative. These results correlate with the negative results which are obtained at low temperature using the techniques of [2] or [6]. However, using our method and assuming a gate dependent $R_{\rm sd}$ and ΔL, positive results have been obtained. It should also be noted that both of the simulated profiles are non-LDD. Previous works have only demonstrated gate dependencies in LDD devices [6], [7]. Additional simulations using an LDD profile yielded a similar decreasing trend in both the locus data and the final $R_{\rm sd}$ and ΔL.

Similar trends in $R_{\rm locus}$ and $\Delta L_{\rm locus}$ were observed from experimental data at both 300 K and 77 K. However, due to freezeout effects and fluctuations between devices at lower temperatures, the experimental $R_{\rm locus}$ and $\Delta L_{\rm locus}$ were not smooth and did not fit as well. Nevertheless, the trends were similar to the simulation results. A polynomial dependence in $R_{\rm sd}$ and ΔL could be used instead of $1/(x + a)$ to fit experimental data, although much of the physical meaning would be lost as a result.

IV. Conclusion

By incorporating a gate dependence in the source/drain resistance and effective channel length, a more physically meaningful extraction of these parameters in an MOS device can be performed. Both parameters have been given a gate dependence, rather than simplifying the problem by assuming that one or both of them are constant. Though the functional dependence of each parameter is arbitrary, a previously suggested $1/(x + a)$ variation [7] has been used. At low temperatures, our method can yield positive, meaningful results for both $R_{\rm sd}$ and ΔL. The gate dependent models for $R_{\rm sd}$ and ΔL can be easily implemented in circuit simulation programs, such as SPICE [11].

Our technique is ultimately limited by the original modeling of the MOS device as three resistors in series. The transition from the external source/drain to the channel is not completely abrupt. At the edges of the channel, the inversion charge is no longer equal to $C_{\rm ox}(V_{\rm gs} - V_{\rm th})$. As a result, $R_{\rm ch}$, which is based on the $I_{\rm ds}$-$V_{\rm gs}$ equation and the assumption that the inversion charge is equal to $C_{\rm ox}(V_{\rm gs} - V_{\rm th})$, cannot be used to model the entire active channel region. Additional resistances can be introduced near the source/drain junction to more accurately characterize the entire channel [10].

It is important to accurately determine both $R_{\rm sd}$ and ΔL, as these parameters will ultimately limit device performance. With some modifications of SPICE, the gate dependency obtained from our extraction technique can be included, and its impact on circuit performance can be studied.

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