of actual operating conditions, so that any errors associated with lifetime extrapolation are minimized.

References

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[3] C. Hu, S.C. Tam, F. Hsu, P. Ko, T. Chan, and K.W. Terrill, *IEEE Trans. Elec. Dev.*, **ED-32** (Feb. 1985), p. 375-385.

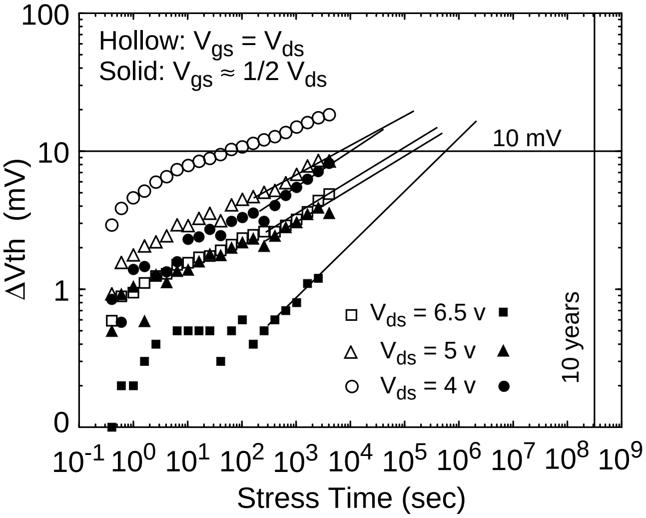

Figure 3: Degradation in Vth at 150 K for stress conditions of $V_{gs} = V_{ds}$ and $V_{gs} \approx 1/2\ V_{ds}$. Δg_m shifts at this temperature do not consistently rise.

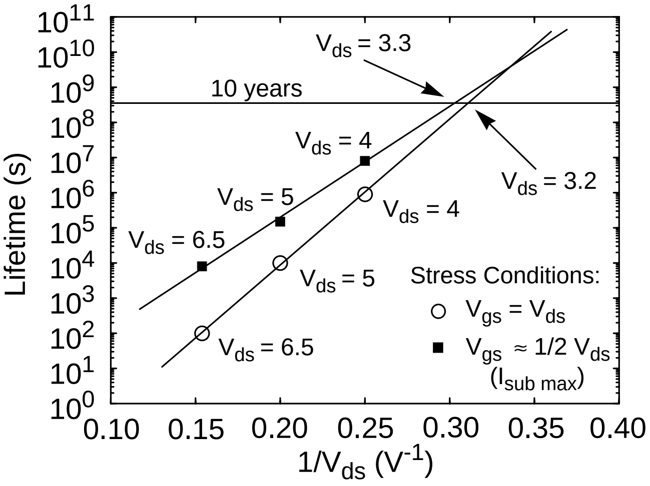

Figure 4: Lifetime vs. V_{ds}^{-1} for 25 x 1 µm NMOS devices at 150 K. The worst case degradation depends on the drain bias (electron injection above 3 v, interface states below 3 v).

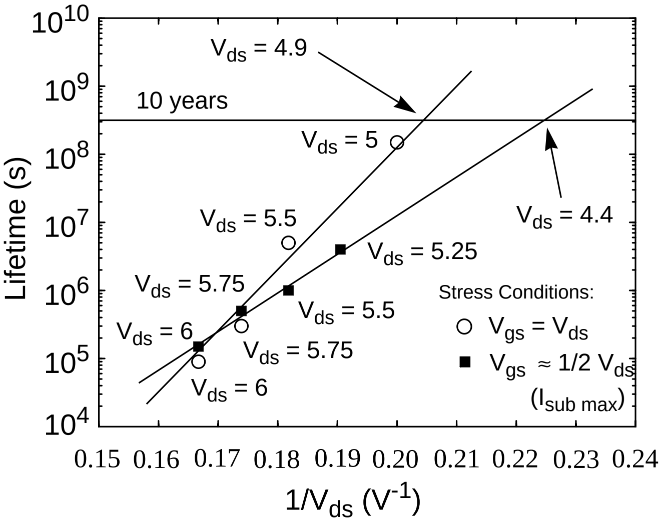

Figure 5: Lifetime vs. V_{ds}^{-1} for 25 x 1 µm NMOS devices at 218 K. Interface state generation limits the device lifetime up to drain voltages of 5.9 v.

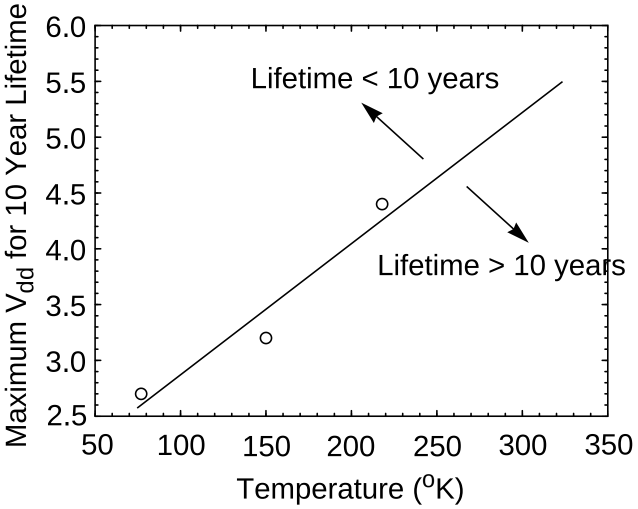

Figure 6: Maximum V_{dd} at different temperatures so that a 10 year device lifetime is possible.

drain bias dependence on the most prevalent degradation mechanism for intermediate temperatures. This transition voltage is proportional to the temperature (5.9 v at 218 K, 3 v at 150 K).

4. CONCLUSION

The reliability of NMOS devices have been studied here between room temperature and 77 K. At lower temperatures, lower power supply voltages are necessary (Figure 6) to maintain a 10 year lifetime. The worst case degradation condition is drain bias dependent. Above a certain drain voltage, electron trapping limits the maximum operating voltage. Below this voltage, interface state generation dominates the degradation. For temperatures in between 300 K and 77 K, this critical voltage is comparable to the power supply voltages under consideration. Therefore, a more careful treatment is needed in order to determine the worst case degradation condition. It is also desirable to choose stress conditions which are representative

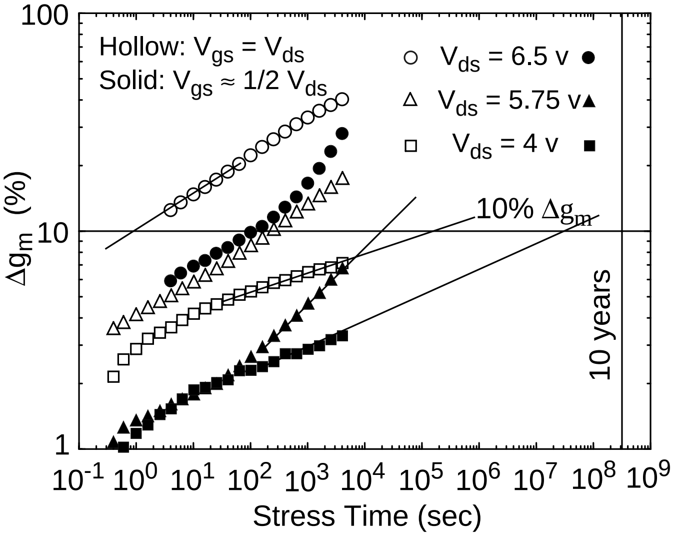

Figure 1: Degradation in g_m at 77 K for stress conditions of $V_{gs} = V_{ds}$ (maximum electron injection) and $V_{gs} \approx 1/2\ V_{ds}$ (maximum interface state generation).

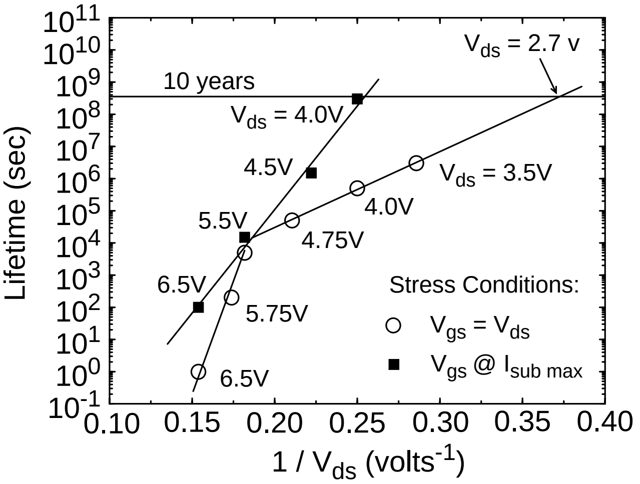

Figure 2: Lifetime versus 1/(drain bias) for 25 x 1 µm NMOS devices at 77 K. A 10% degradation in maximum transconductance (g_m) is used to define device lifetime. For all drain biases, electron injection ($V_{gs} = V_{ds}$) leads to a shorter lifetime. A two slope behavior is also evident for this stress condition.

$V_{gs} \approx 1/2\ V_{ds}$ (worst case stress at 300 K) cases. A novel two-slope behavior occurs for the $V_{gs} = V_{ds}$ stress condition. A similar phenomena has been observed in SOI devices stressed at room temperature [2]. Different damage locations or mechanisms at high and moderate drain biases may explain this trend. Δg_m changes at a different rate (slope) between the high bias (6.5 v, 5.75 v) and low bias (4 v) stress conditions. In any case, this two-slope behavior emphasizes the need to perform hot carrier stressing over a large range of drain voltages, preferably near the desired power supply voltage. Accelerated, high bias hot carrier stressing may not be representative of the actual damage mechanisms under normal operation. If hot carrier stressing had only been performed at high drain biases (V_{ds} > 5 v), a one-slope linear dependence vs. $1/V_{ds}$ would be obtained, and the extrapolated 10-year lifetime (5 v) would be too optimistic.

3.2 Device Lifetime at 150 K

At 150 K, ΔV_{th} is used instead of Δg_m to monitor device degradation due to inconsistent trends in Δg_m for devices under the same stress conditions. Threshold voltage consistently increased versus stress time (Figure 3). A 10 mV shift in Vth was used to define device lifetime at this temperature. Lifetime curves at 150 K are shown in Figure 4 for both $V_{gs} = V_{ds}$ and $V_{gs} \approx 1/2\ V_{ds}$. A two-slope behavior for $V_{gs} = V_{ds}$ is not seen here. A much higher or lower drain voltage stress may be necessary to located the second slope. However, the results here already cover the desired lifetime range. Unlike the 77 K results, the dominant degradation mechanism at 150 K depends on V_{ds}. Above 3 v, $V_{gs} = V_{ds}$ yields lower lifetimes for the same power supply voltage. Below 3 v, the $V_{gs} \approx 1/2\ V_{ds}$ curve will limit the maximum operating voltage.

3.3 Device Lifetime at 218 K

Figure 5 shows the 218 K lifetime curves for devices stressed at gate biases of $V_{gs} \approx 1/2\ V_{ds}$ and $V_{gs} = V_{ds}$. As at 150 K, ΔV_{th} is used instead of Δg_m to measure degradation and lifetime. For V_{ds} values below 5.9 v, $V_{gs} \approx 1/2\ V_{ds}$ results in the worst case degradation. Above this point, the dominant degradation mechanism becomes $V_{gs} = V_{ds}$. Unlike the scenarios at 300 K and 77 K, where only one gate condition condition ($V_{gs} \approx 1/2\ V_{ds}$ at 300 K [3] and $V_{gs} = V_{ds}$ at 77 K) always results in the worst case degradation, there is a

ABSTRACT: CMOS device lifetime is determined at temperatures of 77 K, 150 K, and 218 K. Due to enhanced hot carrier degradation, lower operating voltages are necessary at lower temperatures. A novel two-slope lifetime behavior is observed at 77 K, emphasizing the need to stress devices near the desired operating voltage. The dominant degradation mechanism depends on the drain bias. Above this critical voltage, electron injection dominates. Below this bias, interface-state generation leads to a shorter lifetime. The voltage at which this transition occurs is a function of temperature and is of the same order as the power supply voltage at intermediate temperatures. This explains the change of dominant degradation mechanism from interface states (at 300 K) to electron injection (at 77 K).

1. INTRODUCTION

As MOS transistors are scaled to smaller dimensions to improve both performance and packing density, the impact of hot carriers on device reliability becomes an ever-growing concern. While hot carrier lifetime extraction has been studied in depth at room temperature, very little investigation has been made at low and intermediate operating temperatures. This work will show hot carrier degradation results and ten year device lifetimes for temperatures between 218 K and 77 K.

2. EXPERIMENTAL

Devices used in this study were 25 x 1 μm NMOS transistors with a gate oxide thickness of 150 Å. All devices were DC stressed for 4000 seconds at drain biases ranging from 3 v to 6.5 v using an HP 4142B measurement system connected to a Lakeshore MTD Cryotronics temperature controlled dewar. Gate voltages for each stress condition were either $V_{gs} = V_{ds}$ (maximum electron injection) or $V_{gs} \approx 1/2\ V_{ds}$ ($I_{sub\ max}$: maximum interface state generation). These stress conditions have been shown to cause maximum degradation at 77 K and 300 K, respectively.

3. RESULTS AND DISCUSSION

3.1 Device Lifetime at 77 K

A conventional 10% degradation in g_m is used to define device lifetime at 77 K. Figure 1 shows Δg_m for a variety of different stress conditions. As expected, for any V_{ds}, the $V_{gs} = V_{ds}$ stress condition results in the shortest lifetime [1]. The lifetime curves at 77 K are shown in Figure 2 for both the $V_{gs} = V_{ds}$ and