even more improvement. However, other issues such as testability at room temperature and maximum off-state current need to be considered.

5. CONCLUSION

In conclusion, by simply adjusting the threshold voltage implants for a room temperature technology, significant performance improvements at low temperature are possible. Additional process changes can be made to further improve low temperature performance, such as redesigning the LDD, using P^+ polysilicon for the PMOS gate (to prevent channel doping freezeout), and adding a retrograded well. However, the cost of implementing these more complex processes needs to be considered and carefully examined.

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[4] TMA MEDICI: Two-Dimensional Device Simulation Program (ver. 1.1.3), Technology Modeling Associates, Inc.

[5] M. Song, J. Cable, J. Woo, and K. MacWilliams, *IEEE Elec. Dev. Let.*, **EDL-12** (1991), p. 375-377.

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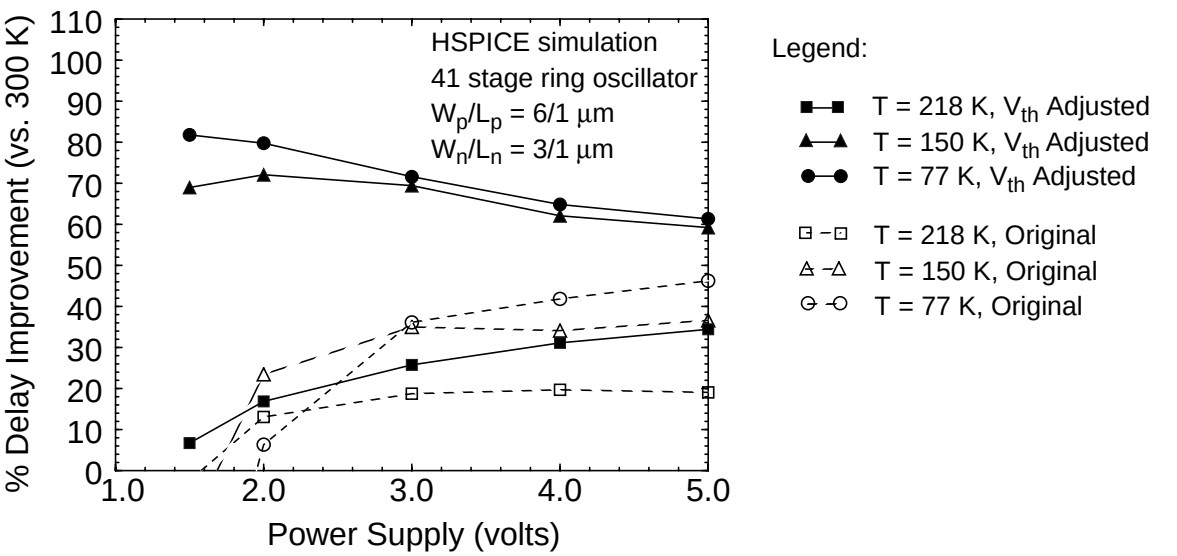

Figure 8: Improvement in ring oscillator delay (normalized to 300 K results) versus power supply voltage as a result of threshold implant adjustment. Delays at 218 K, 150 K, and 77 K were simulated. Original results are also shown for comparison.

LDD regions minimizes the improvement between 150 K and 77 K. Changing the LDD implant to reduce the high parasitic resistance and increase reliability [5,6] will further improve the 77 K performance.

4.2 Below Room Temperature Value

Due to the improvement in subthreshold slope at lower temperatures, a lower than room temperature threshold voltage can be used without causing additional off-state leakage. Figure 9 shows the amount of performance enhancement possible at 77 K with a "25% lower than room temperature" threshold voltage. The improvement is more significant for lower power supply voltages, which will be the desired operating voltage as suggested by the lifetime data (Figure 10). The threshold voltage can be further lowered to gain

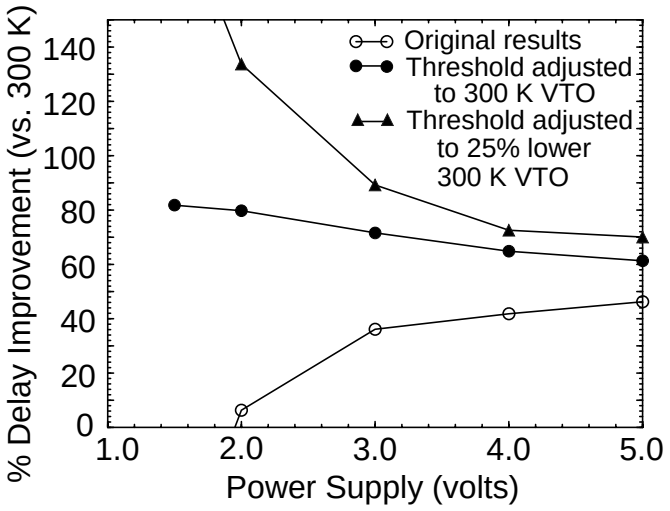

Figure 9: Improvement in delay at 77 K versus power supply voltage for a lower than room temperature threshold voltage. Delay improvements based on the original, measured results and threshold adjustment to a room temperature threshold voltage are shown for reference. A 2x improvement in delay at low power supply (2.8 v) is now possible.

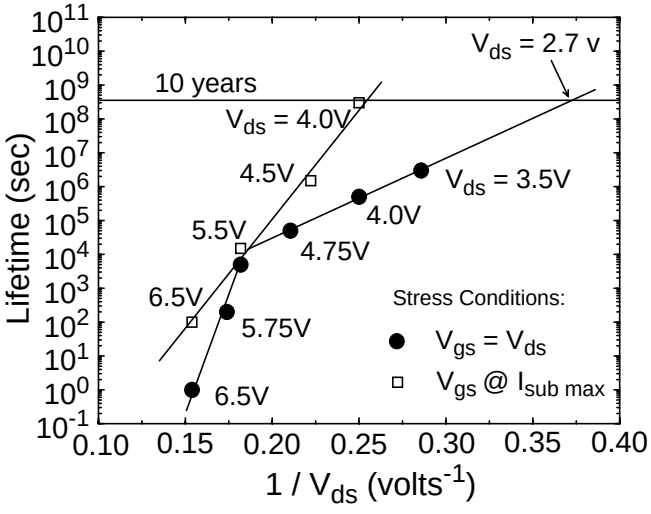

Figure 10: Lifetime versus 1/(drain bias) for 25 x 1 µm NMOS devices at 77 K. A 10% degradation in maximum transconductance (g_m) is used to define device lifetime. Two different stress conditions are used: V_{gs} corresponding to maximum substrate current (worst case degradation at 300 K) and V_{gs} = V_{ds} (worst case at 77 K).

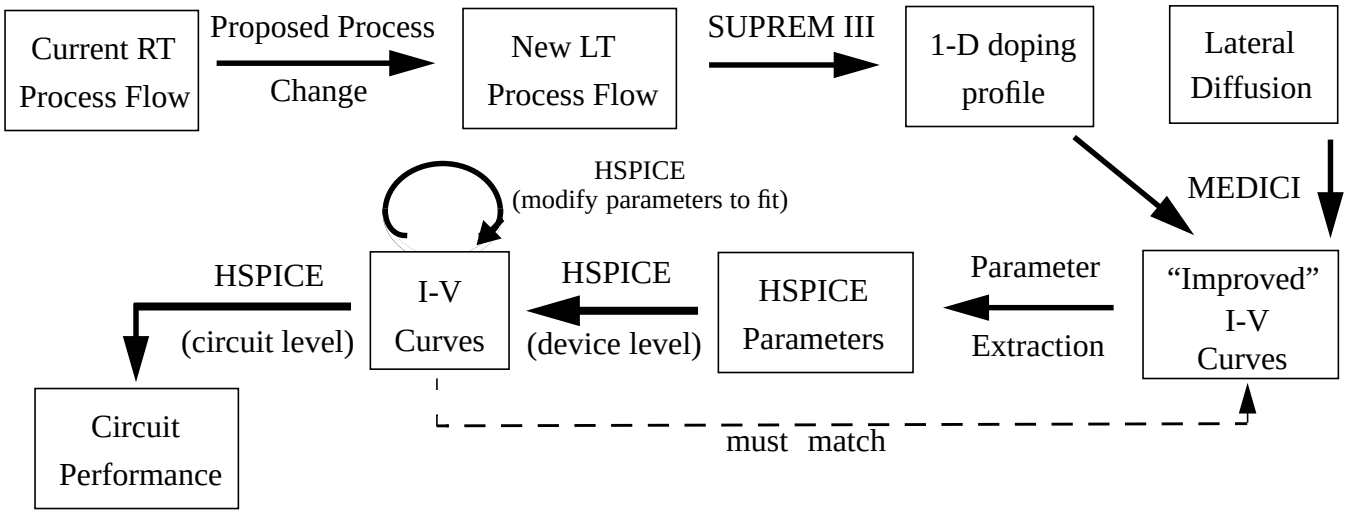

Figure 5: Illustration of how process (SUPREM), device (MEDICI), and circuit (HSPICE) simulation tools are used together to improve the performance of low temperature CMOS. Input decks identical to those used to fit the original, measured results (except for the doping profile) are used as a starting point.

4. THRESHOLD VOLTAGE ADJUSTMENT

4.1 To Room Temperature Value

Using the above technique, the threshold voltage implants were modified to decrease the high threshold voltage at low temperature. Figure 6 shows the implant doses needed to obtain the same room temperature threshold voltage. A larger increase in the PMOS threshold implant dose is necessary to counter freezeout effects. However, the changes are not large enough to worsen short channel effects. The effect of the threshold adjustments on the device level is shown in Figure 7 for a 25 x 1 μm NMOS transistor. Although the linear current only improves slightly, performance on the circuit level is greatly enhanced. Figure 8 shows HSPICE ring oscillator delays for the original and threshold adjusted cases. The amount of improvement is larger at lower temperatures due to the greater shift in threshold voltage. Freezeout of the

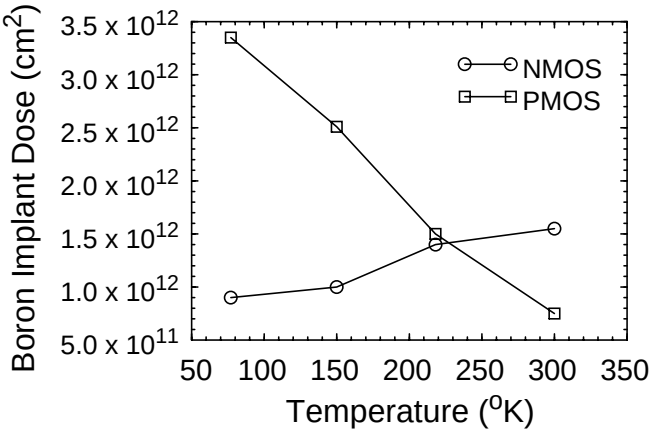

Figure 6: Threshold adjustment implant doses (boron) necessary to maintain a 300 K threshold voltage for a given operating temperature.

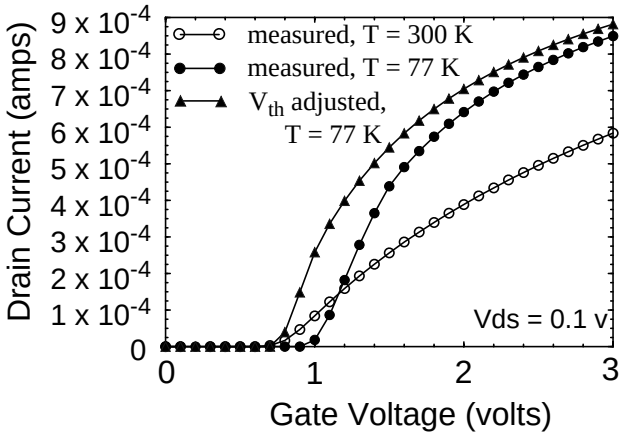

Figure 7: Improvement in the linear drain current characteristics of a 25 x 1 μm NMOS device at 77 K as a result of threshold adjustment. A better match with the 300 K threshold voltage is evident. Freezeout in the LDD regions limit the improvement in current.

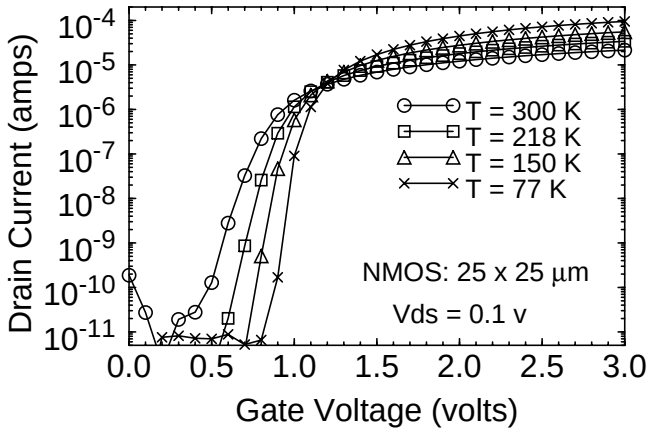

Figure 1: I_{ds}-V_{gs} curves (log scale) for a 25 x 25 μm NMOS device at 300 K, 218 K, 150 K, and 77 K.

Improvement ≡ 100 x [(300 K delay)/(low temp delay) -1]

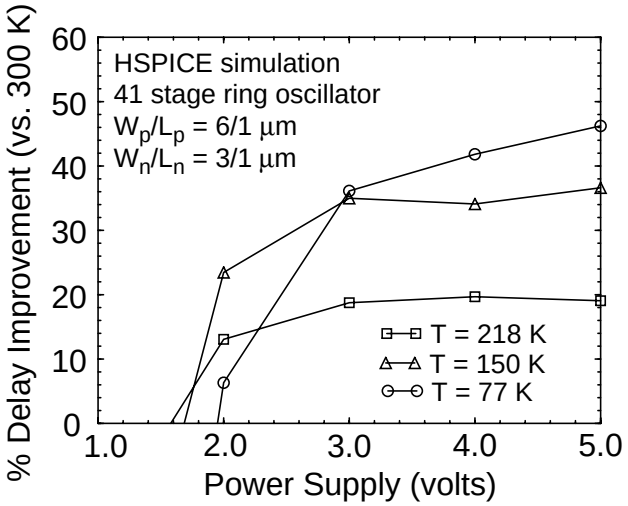

Figure 2: Improvement in delay versus power supply voltage for temperatures of 218 K, 150 K, 77 K. Data is normalized to the propagation delay of a 41 stage ring oscillator at 300 K. At best, only a 1.5x delay reduction is achievable. (77 K, 5 v)

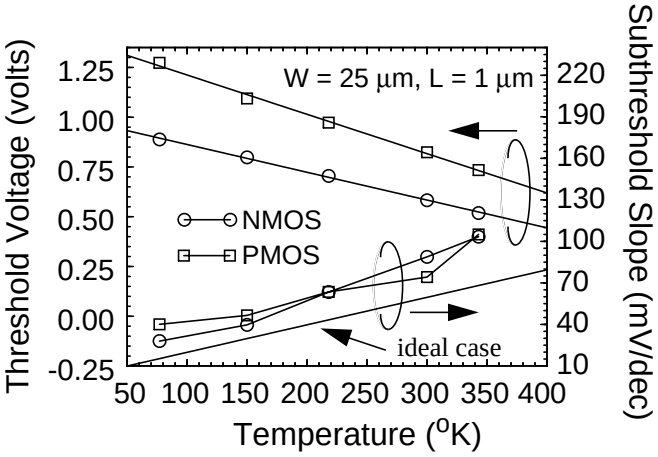

Figure 3: Threshold voltage and subthreshold slope versus temperature for 25 x 1 μm devices. A constant 250 nA current is used to define V_{th}.

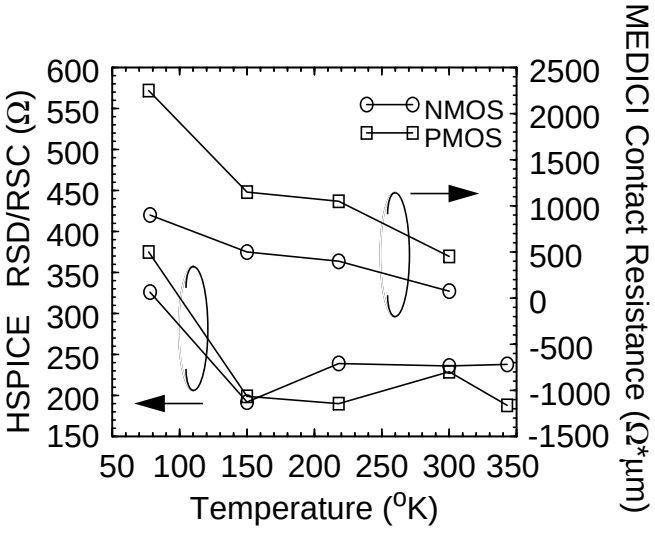

Figure 4: Parasitic source/drain resistances used in HSPICE and MEDICI programs to fit the measured data at 300 K, 218 K, 150 K, and 77 K. The increase in resistance at lower temperatures is due to LDD freezeout.

3. DESIGN APPROACH FOR LOW TEMPERATURE CMOS

A series of TCAD tools were used to examine the effects of process modification on low temperature performance (Figure 5). Starting with the baseline room temperature process flow, process changes are first run through SUPREM to obtain a new doping profile. MEDICI [4] then imports the profile, producing I-V curves. Improvement on the device level can be obtained by comparing these new I-V curves with the original results. To measure circuit level improvement, an extraction and fit to HSPICE should be performed.

ABSTRACT: Only minimal performance improvement is achievable when a standard, room-temperature CMOS component is cooled down to low temperatures. However, by modifying the process flow, a 2-3x increase in performance is possible. TCAD tools can be used to study and optimize an original, room temperature CMOS process for low temperature operation. By adjusting the low temperature threshold voltage to a room temperature value, CMOS ring oscillator delays drop in half. Even greater improvement is possible if a lower threshold voltage is used.

1. INTRODUCTION

Low temperature CMOS has attracted considerable interest in recent years due to its many improvements in device performance, including higher carrier mobility, increased current drive, and lower subthreshold slope. In designing and optimizing CMOS for low temperature operation, new structures and guidelines different from and unrelated to standard room temperature approaches have been proposed [1,2]. Modification of an already existing room temperature process may be a more practical, cost-effective way to implement a low temperature CMOS technology. In addition, the impact of adjusting certain process steps for improved low temperature performance can be better understood and quantified. In this paper, improvements in low temperature CMOS performance will be studied through changing a conventional 1 μm room temperature CMOS process.

2. PERFORMANCE LIMITATIONS OF ROOM TEMPERATURE CMOS

Cooling down a room temperature technology only enhances performance to a small degree. Figure 1 shows the linear I_{ds}-V_{gs} characteristics of a 25 x 25 μm NMOS device at different temperatures. Higher drain current and more rapid turn-off characteristics are evident as the temperature is decreased. However, HSPICE ring oscillator simulations based on measured I-V results (Figure 2) suggest only minimal circuit level performance improvement. Delays are especially poor at lower power supply voltages, which will be the desired operating point at low temperatures to avoid enhanced hot-carrier degradation [3] and to ease required cooling power.

The lack of improvement in the room temperature designed devices at low temperature is caused by an increase in threshold voltage, which limits the improvement in current (Figure 3). In addition, carrier freezeout of the p-channel threshold implant leads to an even larger increase in the PMOS threshold voltage and poorer subthreshold slope improvement. The NMOS and PMOS LDD regions also freezeout and cause an increase in the parasitic source/drain resistances at lower temperature (Figure 4), further limiting the current.