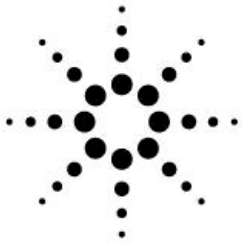
The HDCS Family of CMOS Image Sensors



Agilent Technologies
Innovating the HP Way

Agilent Technologies Part Number HDCS-2020/1020
Product Technical Specification
Revision 1.2

Imaging Electronics Division
Agilent Technologies, Inc.
1020 NE Circle Boulevard
Corvallis, Oregon 97330

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1. Sensor Overview

1.1 Introducing The HDCS Family

HDCS-2020(VGA) and HDCS-1020(CIF) are CMOS active pixel image sensors with integrated A/D conversion and full timing control. They provide random access of sensor pixels which allows windowing and panning capabilities. The sensor is designed for video conferencing applications and still image capabilities. The HDCS family achieves excellent image quality with very low dark current, high sensitivity, and superior anti-blooming characteristics. The devices operate from a single DC bias voltage, are easy to configure and control, and feature low power consumption.

1.2 Features

- Available in two image array sizes: VGA (640 x 480) and CIF (352 x 288)
- RGB Bayer color filter array
- Programmable window size ranging from the full array down to a 4 x 4 pixel window
- Programmable panning capability which allows a specified window(minimum 4x4 pixels) to be located anywhere on the sensor array
- Independent X and Y sub-sampling modes (2:1 each) providing up to a 4X frame rate increase
- HDCS-1020 Full frame video rate at 8 bit resolution: 30 fps CIF at 30 MHz and 25.8 fps at 25 Mhz
- HDCS-2020 Full frame video rates at 10 bit resolution: 14 fps VGA at 25 MHz
- Still image capability
- Mechanical shutter and external flash mode
- Low power modes
- Shadow gain and exposure registers
- Integrated analog to digital converters. HDCS-2020 (10 bit), HDCS-1020 (8 bit)
- Integrated programmable gain amplifiers with independent gain control for each color (R, G, B)
- Integrated voltage references
- Automatic subtraction of column fixed pattern noise
- Internal register set programmable via either the UART or Synchronous serial interface
- Integrated timing controller with rolling electronic shutter, row/column addressing, and operating mode selection with programmable exposure control, frame rate, and data rate
- Digital image data output via 8 bit(HDCS-1020) and 10 bit(HDCS-2020) synchronous parallel interface or serial interface
- Programmable horizontal, vertical, and shutter synchronization signals
- Programmable horizontal and vertical blanking intervals
- A Single 3.3 volt power supply is all that is needed

1.3 Applications

- Digital still camera
- PC Camera
- Handheld Computers
- Cellular Phones
- Notebook Computers
- Toys

1.4 Typical Electrical Specifications

Electrical Specifications	
Pixel size	7.4 x 7.4 um
Maximum Clock Rate	25 MHz (VGA), 30Mhz (CIF)
Effective Sensor Dynamic Range	65 db
Effective Noise Floor	45 electrons
Dark Signal [1]	1500 electrons/sec at 22 C ambient
Sensitivity [2]	20 V/(Lux-S) at 20 fps
Peak Quantum Efficiency [1, 2]	20%
Saturation Voltage	1.3V
Full Well Capacity	71,000 electrons
Conversion Gain [2]	18 u V/electron
Programmable Gain Range	1 - 40 (8 bit resolution)
Fill Factor	40%
Exposure Control	0.5 u sec minimum, 0.5 u sec increments
Package	32 pin J Lead optical package
Supply Voltage	3.3v, -5/+10%
Power Consumption	200 mW max operating, 3.3 mW max standby
Operating Temperature	-5 to +65 C
Storage Temperature	-40 to +125 C

Table 1. Electrical Specifications

Notes: (1) Specified over complete pixel area (2) Measured at unity gain

1.5 HDCS Sensor Top Level Block Diagram

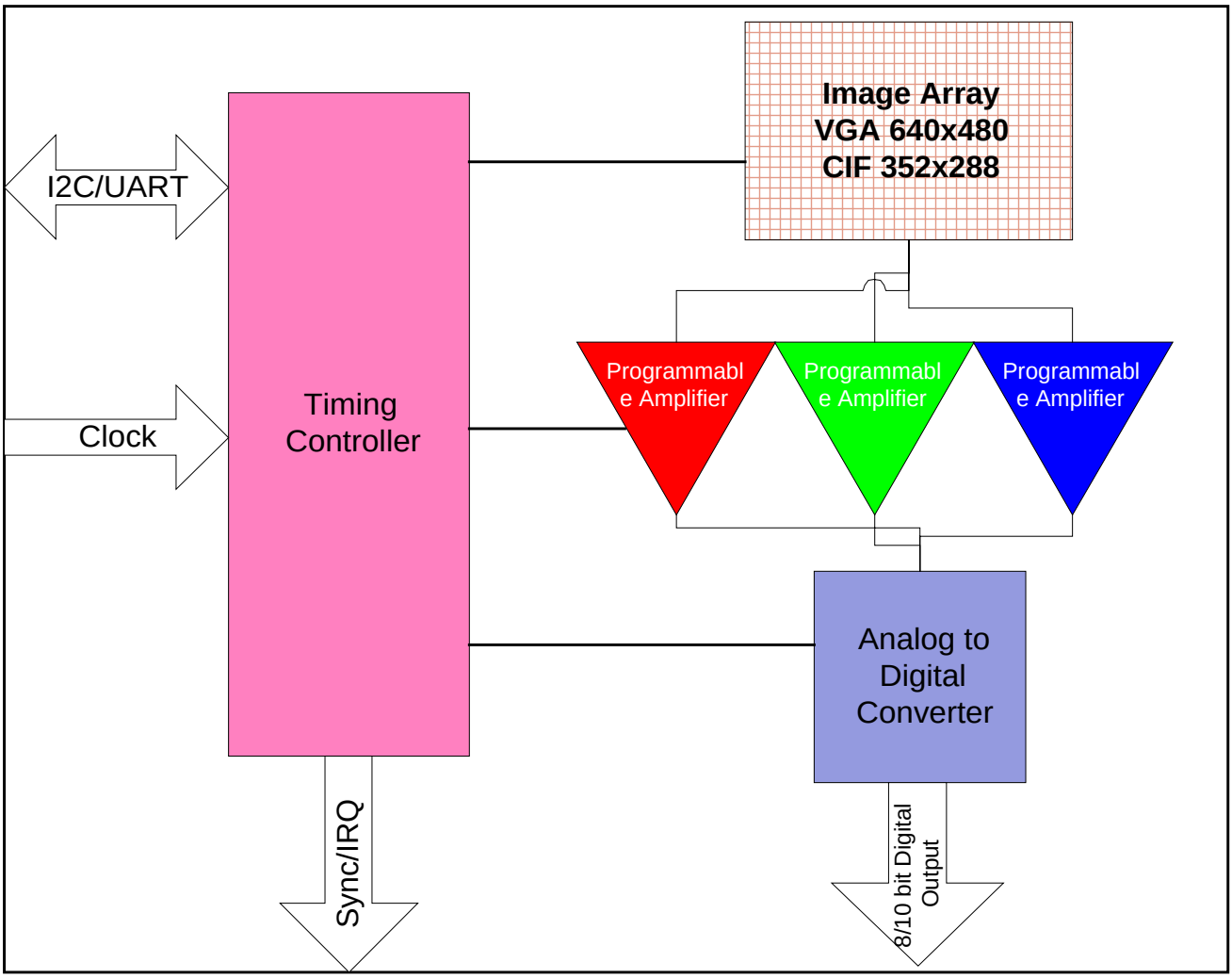

Figure 1. Top Level Architectural Block Diagram

1.6 High Level Description of Operation

HDCS Sensors are controlled through a serial interface. The serial interface may be configured as a half-duplex UART slave, or as a Synchronous Serial slave. The serial interface is used to write the system registers to set up the viewing window coordinates, integration/exposure time, frame rate, PGA gain, interrupt masks, status pins functions, output pin switching speed, output data format, and output data timing.

A system reset must be performed by asserting the nRST pin before operation may begin.

The CONFIG register selects one of the operating modes: 1) normal, or 2) mechanical shutter. The CONFIG register also allows the selection of sub-sampling mode, and either single frame capture mode, or continuous run mode. Operation begins when the RUN bit in the CONTROL register is set.

The following discussion pertains to operation in normal mode.

When operation begins the timing generator resets the top pixel row of the viewing window. After a pixel row is reset it begins integration. After one Row Process time elapses the next row is reset. This continues until the bottom row of the viewing window is reached. In continuous mode this process repeats by wrapping to the top row of the viewing window. IN single frame capture mode the process ends when the bottom row of the viewing window is reached. IN continuous run mode if the integration time is less than the time to cycle through a frame there is no overhead time between frames. If the integration time is greater than the time to cycle through a frame there is an overhead delay between frames equal to integration time minus the time to cycle through a frame.

Row Processing has 2 parts: 1) Row Sample followed by 2) Column Processing. Row Sampling consists of selecting a row and reading it into the analog row buffer. Column processing consists of reading pixel data out of the analog row buffer, converting it to digital data, then outputting the digital value from the chip. Column Processing time depends on the input clock (CLK) speed, and the TCTRL system register. See the Register Set chapter and Programmer reference for more details.

The output portion of Column Processing is suppressed until the first row finishes integration. Therefore if the integration time equals 8 Row Process times, data for Row (N) is begin read out, while Row (N+8) is begin reset. After the initial overhead of waiting for the first row to integrate, during each Row Process time one row is being reset, and a different row is being read out.

When the row has finished integration it is transferred to the analog row buffer using double correlated sampling and reference column subtraction, then Column Processing begins.

Column Processing reads data out of the analog row buffer in pixel pairs. The pixel pairs are processed by 2 parallel channels. The first row is an even row. Even rows are green-red rows from the bayer filter pattern. The first pixel of a green-red row is a green pixel. Odd rows are blue-green rows of the bayer filter pattern. The first pixel of a blue-green row is a blue pixel. Each pixel is transmitted through a PGA (programmable gain amplifier). Pixels are amplified by different values corresponding to the pixel position in the 2 by 2 block of the RGB bayer color filter pattern. In other words each color (R/G/B) is amplified by a different number. Each ADC (analog to digital converter) channel converts the analog PGA output to a 10 bit digital value. The ADC values for both channels are output in sequential order on the parallel DATA pins along with the assertion of the DRDY pin. The timing of the DATA and DRDY pins is programmable. Column Processing continues until all the pixels for the viewing window have been output on the DATA pins. The nROW status signal is asserted when the data for the last pixel of the row has been output.

When nROW is asserted for the bottom row of the viewing window, nFRAME is also asserted.

If the CFC bit of the CONFIG register equals ‘0’, then the sensor is in single frame mode. In single frame mode if the nIRQ_nCC (interrupt/capture complete) status pin is enabled as capture complete, then nIRQ_nCC is asserted at

the same time as nFRAME. The RF (run flag) is turned off in the STATUS register and the sensor idles until it is told to run another frame.

If the CFC bit of the CONFIG register equals '1', then HDCS sensor is in continuous run mode. In continuous run mode after the assertion of an nFRAME, the sensor immediately begins the next frame which as already started integrating. If integration time is less than the time to cycle through 1 frame, then there is no delay between the processing of the bottom row of frame X and the top of frame X+1. If integration time is greater than the time to cycle through 1 frame, then there is a delay between the bottom row of frame X and top row of frame X+1. The delay equals integration time minus the time to cycle through one frame.

Continuous Run mode is terminated by resetting the RUN bit of the CONTROL register. Single Frame mode may also be terminated by de-asserting the RUN bit. If the SFC (stop when frame complete) bit of the CONFIG register is set when the RUN bits is de-asserted HDCS sensor will process until nFRAME is asserted at the normal time, then return to idle. If the SFC (stop when frame complete) bit of the CONFIG register is not set when the RUN bit is de-asserted, the sensor will immediately assert in nFRAME, nROW, and nIRQ_nCC and return to the idle state. If enabled for the capture complete function, the nIRQ_nCC (interrupt/capture complete) status flag is asserted at the same time as nFRAME for the last frame.

Time = 1	
Row 0	**RESET (0)**
Row 1	
Row 2	
Row 3	
Row 4	
Row 5	

Time = 2	
Row 0	**INTEGRATE(1)**
Row 1	**RESET(0)**
Row 2	
Row 3	
Row 4	
Row 5	

Time = 3	
Row 0	**INTEGRATE(2)**
Row 1	**INTEGRATE(1)**
Row 2	**RESET(0)**
Row 3	
Row 4	
Row 5	

Time = 4	
Row 0	**READ(3)**
Row 1	**INTEGRATE(2)**
Row 2	**INTEGRATE(1)**
Row 3	**RESET(0)**
Row 4	
Row 5	

Time = 5	
Row 0	
Row 1	**READ(3)**
Row 2	**INTEGRATE(2)**
Row 3	**INTEGRATE(1)**
Row 4	**RESET(0)**
Row 5	

Time = 6	
Row 0	
Row 1	
Row 2	**READ(3)**
Row 3	**INTEGRATE(2)**
Row 4	**INTEGRATE(1)**
Row 5	**RESET(0)**

Time = 7	
Row 0	**RESET(0)**
Row 1	
Row 2	
Row 3	**READ(3)**
Row 4	**INTEGRATE(2)**
Row 5	**INTEGRATE(1)**

Time = 8	
Row 0	**INTEGRATE(1)**
Row 1	**RESET(0)**
Row 2	
Row 3	
Row 4	**READ(3)**
Row 5	**INTEGRATE(2)**

Time = 9	
Row 0	**INTEGRATE(2)**
Row 1	**INTEGRATE(1)**
Row 2	**RESET(0)**
Row 3	
Row 4	
Row 5	**READ(3)**

Time = 10	
Row 0	**READ(3)**
Row 1	**INTEGRATE(2)**
Row 2	**INTEGRATE(1)**
Row 3	**RESET(0)**
Row 4	
Row 5	

Time = 11	
Row 0	
Row 1	**READ(3)**
Row 2	**INTEGRATE(2)**
Row 3	**INTEGRATE(1)**
Row 4	**RESET(0)**
Row 5	

Time = 12	
Row 0	
Row 1	
Row 2	**READ(3)**
Row 3	**INTEGRATE(2)**
Row 4	**INTEGRATE(1)**
Row 5	**RESET(0)**

Figure 2. Example of 6 view window with integration time = 2 rows

Time = 1	
Row 0	**RESET (0)**
Row 1	
Row 2	
Row 3	
Row 4	
Row 5	

Time = 2	
Row 0	**INTEGRATE(1)**
Row 1	
Row 2	
Row 3	
Row 4	
Row 5	

Time = 3	
Row 0	**INTEGRATE(2)**
Row 1	**INTEGRATE(1)**
Row 2	**RESET(0)**
Row 3	
Row 4	
Row 5	

Time = 4	
Row 0	**INTEGRATE(3)**
Row 1	**INTEGRATE(2)**
Row 2	**INTEGRATE(1)**
Row 3	**RESET(0)**
Row 4	
Row 5	

Time = 5	
Row 0	**INTEGRATE(4)**
Row 1	**INTEGRATE(3)**
Row 2	**INTEGRATE(2)**
Row 3	**INTEGRATE(1)**
Row 4	**RESET(0)**
Row 5	

Time = 6	
Row 0	**INTEGRATE(5)**
Row 1	**INTEGRATE(4)**
Row 2	**INTEGRATE(3)**
Row 3	**INTEGRATE(2)**
Row 4	**INTEGRATE(1)**
Row 5	**RESET(0)**

Time = 7	
Row 0	**INTEGRATE(6)**
Row 1	**INTEGRATE(5)**
Row 2	**INTEGRATE(4)**
Row 3	**INTEGRATE(3)**
Row 4	**INTEGRATE(2)**
Row 5	**INTEGRATE(1)**

Time = 8	
Row 0	**INTEGRATE(7)**
Row 1	**INTEGRATE(6)**
Row 2	**INTEGRATE(5)**
Row 3	**INTEGRATE(4)**
Row 4	**INTEGRATE(3)**
Row 5	**INTEGRATE(2)**

Time = 9	
Row 0	**READ(8)**
Row 1	**INTEGRATE(7)**
Row 2	**INTEGRATE(6)**
Row 3	**INTEGRATE(5)**
Row 4	**INTEGRATE(4)**
Row 5	**INTEGRATE(3)**

Time = 10	
Row 0	**RESET(0)**
Row 1	**READ(8)**
Row 2	**INTEGRATE(7)**
Row 3	**INTEGRATE(6)**
Row 4	**INTEGRATE(5)**
Row 5	**INTEGRATE(4)**

Time = 11	
Row 0	**INTEGRATE(1)**
Row 1	**RESET(0)**
Row 2	**READ(8)**
Row 3	**INTEGRATE(7)**
Row 4	**INTEGRATE(6)**
Row 5	**INTEGRATE(5)**

Time = 12	
Row 0	**INTEGRATE(2)**
Row 1	**INTEGRATE(1)**
Row 2	**RESET(0)**
Row 3	**READ(8)**
Row 4	**INTEGRATE(7)**
Row 5	**INTEGRATE(6)**

Time = 13	
Row 0	**INTEGRATE(3)**
Row 1	**INTEGRATE(2)**
Row 2	**INTEGRATE(1)**
Row 3	**RESET(0)**
Row 4	**READ(8)**
Row 5	**INTEGRATE(7)**

Time = 14	
Row 0	**INTEGRATE(4)**
Row 1	**INTEGRATE(3)**
Row 2	**INTEGRATE(2)**
Row 3	**INTEGRATE(1)**
Row 4	**RESET(0)**
Row 5	**READ(8)**

Time = 15, go to time=7	
Row 0	**INTEGRATE(5)**
Row 1	**INTEGRATE(4)**
Row 2	**INTEGRATE(3)**
Row 3	**INTEGRATE(2)**
Row 4	**INTEGRATE(1)**
Row 5	**RESET(0)**

Figure 3. Example of 6 row view window with integration time = 7 rows

2. Register Set

2.1 Register List and Address Map

The registers used to configure and control the HDCS sensor are organized as a sequential array of 8 bit registers. The register names, mnemonics, size, and offset from the chip base address are listed here:

Register Name	Mnemonic	Address (hex)
Identifications Register	IDENT	0x00
Status Register	STATUS	0x01
Interrupt Mask Register	IMASK	0x02
Pad Control Register	PCTRL	0x03
Pad Drive Control Register	PDRV	0x04
Interface Control Register	ICTRL	0x05
Interface Timing Register	ITMG	0x06
Baud Fraction Register	BFRAC	0x07
Baud Rate Register	BRATE	0x08
ADC Control Register	ADCCTRL	0x09
First Window Row Register	FWROW	0x0A
First Window Column Register	FWCOL	0x0B
Last Window Row Register	LWROW	0x0C
Last Window Column Register	LWCOL	0x0D
Timing Control Register	TCTRL	0x0E
PGA Gain Register: Even Row, Even Column	ERECPGA	0x0F
PGA Gain Register: Even Row, Odd Column	EROCPGA	0x10
PGA Gain Register: Odd Row, Even Column	ORECPGA	0x11
PGA Gain Register: Odd Row, Odd Column	OROCPGA	0x12
Row Exposure Low Register	ROWEXPL	0x13
Row Exposure High Register	ROWEXPH	0x14
Sub-Row Exposure Register	SROWEXP	0x15
Error Control Register	ERROR	0x16
Interface Timing 2 Register	ITMG2	0x17
Interface Control 2 Register	ICTRL2	0x18
Horizontal Blank Register	HBLANK	0x19
Vertical Blank Register	VBLANK	0x1A
Configuration Register	CONFIG	0x1B
Control Register	CONTROL	0x1C

Table 2. Register Set Declaration

2.2 Register Descriptions

2.2.1 IDENT: Identification Register

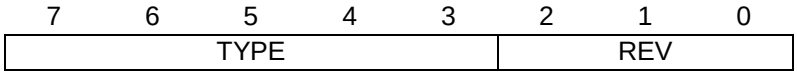

Figure 4. Identification Register Format

Mnemonic	Read/Write Control	Description
REV	R	Revision. **REV** 000 : Revision A. 0001 - 111: Reserved.
TYPE	R	Chip Type. **TYPE** 00010 : HDCS - 1020 00011 : HDCS - 2020 00100- 11111: Reserved

Table 3. Identification Register bit descriptions

2.2.2 STATUS: Status Register

	7	6	5	4	3	2	1	0
	RSV	SSF	SFS	EFS	CC	FC	RC	RF
Reset Value	X	0	0	0	0	0	0	0

Figure 5. Status Register Format

Mnemonic	Read/Write Control	Description
RF	R	Run flag. When 1, indicates an image capture process is executing. When 0, indicates no image capture process is executing.
RC	R/W	Row Complete flag. When 1, indicates a row has been completed since RC flag last cleared. When 0, indicates a row has not been completed since RC flag last cleared. Clear by writing a 1 to the RC flag.
FC	R/W	Frame Complete flag. When 1, indicates a frame has been completed since FC was last cleared. When 0, indicates a frame has not been completed since FC flag was last cleared. Clear by writing a 1 to the FC flag.
CC	R/W	Image Capture Complete flag. When 1, indicates an image capture process has been completed since CC flag last cleared. When 0, indicates an image capture process has not been completed since the CC flag was last cleared. Clear by writing a 1 to the CC flag.
EFS	R/W	Exposure Frame registers Sampled. When 1, indicates that the shadow registers related to exposure frames have been updated with the contents of the corresponding register in the directly user accessible register set. Cleared by writing a 1 to the EFS flag.
SFS	R/W	Sample Frame Registers Sampled. When 1, indicates that the shadow registers related to sample frames have been updated with the contents of the corresponding register in the directly user accessable register set. Cleared by writing a 1 to EFS flag.
SSF	R/W	Shutter Sync flag. When 1, indicates that all rows in the selected image window have been reset while running in the "shutter mode" and that the timing controller has started a delay period to allow the host system to activate either a mechanical shutter or strobe light since the flag was last cleared. When 0, indicates no shutter synchronization event has been detected since the flag was last cleared. Clear by writing a 1 to SSF.
RSV	N/S	Reserved.

Table 4. Status Register bit descriptions

2.2.3 IMASK: Interrupt Mask Register

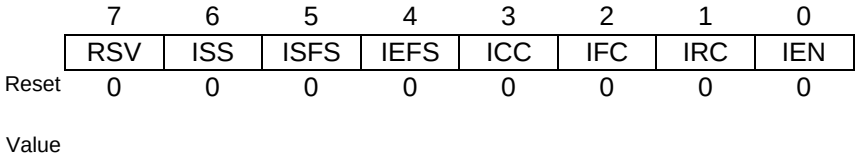

Figure 6. Interrupt Mask Register Format

Mnemonic	Read/Write Control	Description
IEN	R/W	Interrupt Enable. When 1, active and enabled interrupt sources will generate an interrupt. When 0, all interrupts are disabled.
IRC	R/W	Interrupt when Row Complete. When 1, an interrupt will be asserted after completion of each row. When 0, no row complete interrupt will be asserted.
IFC	R/W	Interrupt when Frame Complete. When 1, an interrupt will be asserted after completion of each frame. When 0, no frame complete interrupt will be asserted.
ICC	R/W	Interrupt when Capture Complete. When 1, an interrupt will be asserted after completion of each image capture process. When 0, no image capture complete interrupt will be asserted.
IEFS	R/W	Interrupt when the exposure frame registers sampled flag is set. When 1, an interrupt request will be asserted when the EFS flag of the STATUS register is set. When 0, no interrupt request will be asserted when the EFS flag is set.
ISFS	R/W	Interrupt when the sample frame registers sampled flag is set. When 1, an interrupt request will be asserted when the SFS flag of the STATUS register is set. When 0, no interrupt request will be asserted when the SFS flag is set.
ISS	R/W	Interrupt when shutter sync flag set. When 1, an interrupt will be asserted when the shutter synchronization flag of the STATUS register is set. When 0, no interrupt will be asserted when the shutter synchronization flag is set.
RSV	N/A	Reserved.

Table 5. Interrupt Mask Register bit descriptions

2.2.4 PCTRL: Pad Control Register

	7	6	5	4	3	2	1	0
	LVC	LVF	LVR	IPD	ICE	FSS	FSE	RCE
Reset Value	0	0	0	1	1	0	1	1

Figure 7. Pad Control Register Format

Mnemonic	Read/Write Control	Description
RCE	R/W	Row Complete Enable. When 1, enables the row complete status output signal (TCLK). When 0, disables the row complete status signal.
FSE	R/W	Frame Complete/Shutter Sync Enable. When 1, enables the multifunction frame complete/shutter sync status output signal (nFRAME_nSYNC). When 0, disables the multifunction frame complete/shutter sync status signal.
FSS	R/W	Multifunction pin mode select. When 1, the multifunction nFRAME_nSYNC signal is configured to operate as the shutter sync signal. When 0, the multifunction nFRAME_nSYNC signal is configured to operate as the frame complete signal.
ICE	R/W	Image capture complete enable. When 1, the multifunction nIRQ_nCC pin functions as the image capture complete status output. When 0, the multifunctions nIRQ_nCC pin functions as the active low interrupt request output.
IPD	R/W	Interrupt pin internal pull-up disable. When 1, internal circuitry does not drive the nIRQ_nCC output high. When 0, a weak internal pull-up driver is enabled for the nIRQ_nCC output pin. Only applies when the ICE bit is configured for the interrupt request mode.
LVR	R/W	Level row status signal select. When 1, the nROW status signal is asserted for the entire row processing time when it is enabled. When 0, the nROW status signal is asserted for 4 clock cycles at the end of row processing time when it is enabled.
LVF	R/W	Level frame status signal select. When 1, the nFRAME_nSYNC status signal is asserted for the entire frame processing time when it is enabled and configured as the frame complete signal. When 0, the nFRAME_nSYNC status signal is asserted for 4 clock cycles at the end of frame processing time when it is enabled.
LVC	R/W	Level capture complete status signal select. When 1, the nIRQ_nCC status signal is asserted for the entire duration an image capture process is running when the signal is enabled and configured as the capture complete signal. When 0, the nIRQ_nCC status signal is asserted for 4 clock cycles at the end of a completed image capture process time when it is enabled.

Table 6. Pad Control Register Bit Descriptions

2.2.5 PDRV: Pad Drive Control Register

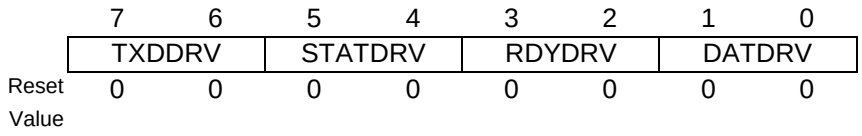

Figure 8. Pad Drive Control Register Format

Mnemonic	Read/Write Control	Description
DATDRV	R/W	Parallel data port drive level select. **DATDRV** 00: High drive (5 ns) 01: Medium high drive (10 ns) 10: Medium low drive (15 ns) 11: Low drive (20 ns)
RDYDRV	R/W	DRDY signal drive level select. **RDYDRV** 00: High drive (5 ns) 01: Medium high drive (10 ns) 10: Medium low drive (15 ns) 11: Low drive (20 ns)
STATDRV	R/W	nRow, tclk_nFrame, nIRQ_nCC, status signal output pin drive level select. **STATDRV** 00: High drive (5 ns) 01: Medium high drive (10 ns) 10: Medium low drive (15 ns) 11: Low drive (20 ns)
TXDDRV	R/W	Serial transmit data signal drive level select. **TXDDRV** 00: High drive (5 ns) 01: Medium high drive (10 ns) 10: Medium low drive (15 ns) 11: Low drive (20 ns)

Table 7. Pad Drive Control Register Bit Descriptions

2.2.6 ICTRL: Interface Control Register

	7	6	5	4	3	2	1	0
	HAVG	DSC		DDO	DOD		DAD	AAD
Reset 2020	0	0	1	0	0	0	0	0
Reset 1020	0	1	1	0	RSV	RSV	0	0

Figure 9. Interface Control Register Format

Mnemonic	Read/Write Control	Description
AAD	R/W	Auto Address Disable. When 0, register addresses are automatically incremented after each register write. When 1, the desired register address must be set prior to each register write.
DAD	R/W	Device Address Disable. When 0, the device address must be included in each serial message packet. When 1, the device address is not included in the serial message packets.
DOD	R/W	Data Output Disable. DOD 00: DATA[9:0] is driven with ADC_data[9:0]. 01: DATA[1:0] outputs are driven to zero. DATA[9:2] is driven with ADC_data[9:0] rounded up to 8 significant bits. 10: DATA[1:0] are driven to zero. If ADC_data[9] or ADC_data[8] is one, DATA[9:2] is forced to be xFF, otherwise DATA[9:2] is driven with ADC_data[7:0]. This is called saturation mode 2. 11: DATA[1:0] are driven to zero. If ADC_data[9] is one, DATA[9:2] is forced to be xFF, otherwise DATA[9:2] is driven with ADC_data[8:1]. This is called saturation mode 1.
DDO	R/W	Delay Data Output. When 0, parallel data outputs switch relative to the rising edge of the system clock. When 1, parallel data outputs switch relative to the falling edge of the system clock. When DSYNC is set, will control nROW, nFRAME_nSYNC and nIRQ_nCC as per data.
DSC	R/W	Data Setup cycle count before DRDY is asserted. 00: 0 clock, 01: clocks, 10: 2 clocks, 11: 3 clocks
HAVG	R/W	Horizontal average enable. When 1, horizontal averaging of RGB outputs is enabled. When 0, horizontal averaging is disabled.

Table 8. Interface Control Register Bit Descriptions

2.2.7 ITMG: Interface Timing Control Register

	7	6	5	4	3	2	1	0
	RSV		DPS	DHC		RPC		
Default 2020	X	X	0	0	1	0	1	0
Default 1020	X	X	0	1	1	0	1	0

Figure 10. Interface Timing Register Format

Mnemonic	Read/Write Control	Description
RPC	R/W	Data Ready Pulse Count: The number of cycles that the DRDY signal is asserted. **RPC Number of Clock Cycles DRDY Signal Asserted** 000: 1 clock 001: 2 clocks 010: 3 clocks 011: 4 clocks 100: 5 clocks 101: 6 clocks 110: 7 clocks 111: 8 clocks
DHC	R/W	Data Hold cycle count after de-assertion of DRDY. 00: 0 clock, 01: 1 clocks, 10: 2 clocks, 11: 3 clocks
DPS	R/W	DRDY signal Polarity Select. When 0, DRDY is active high. When 1, DRDY is active low.
RSV	N/A	Reserved.

Table 9. Interface Timing Register Bit Descriptions

2.2.8 BFRAC: Baud Fraction Register

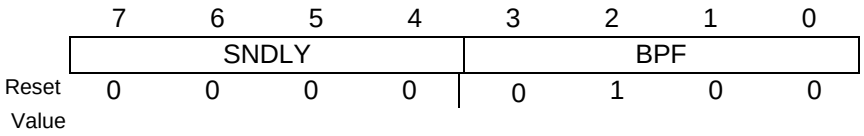

Figure 11. Baud Fraction Register Format

Mnemonic	Read/Write Control	Description
BPF	R/W	Baud Rate Fraction. Fractional portion of the baud period. **BPFBAUD Rate Fraction** 0000:Zero fractional portion. 0001:1 / 16 …etc 1111:15/16
SNDLY	R/W	Number of Stop Bits to delay when sending bytes. This applies to delay before sending the first byte, and delay between subsequent bytes. There is always 1 stop bit delay and SBDLY is the number of additional stop bits to delay.

Table 10. Baud Fraction Register Bit Descriptions

2.2.9 BRATE: Baud Rate Register

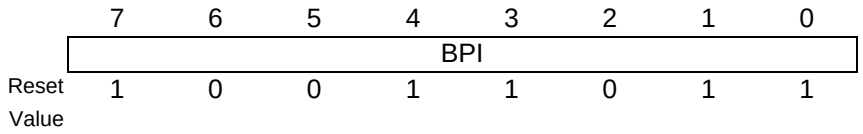

Figure 12. Baud Rate Register Format

Mnemonic	Read/Write Control	Description
BPI	R/W	Baud Rate Integer. Integer portion of baud rate. BAUD_PERIOD = 1 / (BAUD_RATE) BAUD_RATE = CLK_FREQ * [16 * (BPI + 1) + (BPF)]

Table 11. Baud Rate Register Bit Descriptions

2.2.10 ADCCTRL: ADC Control Register

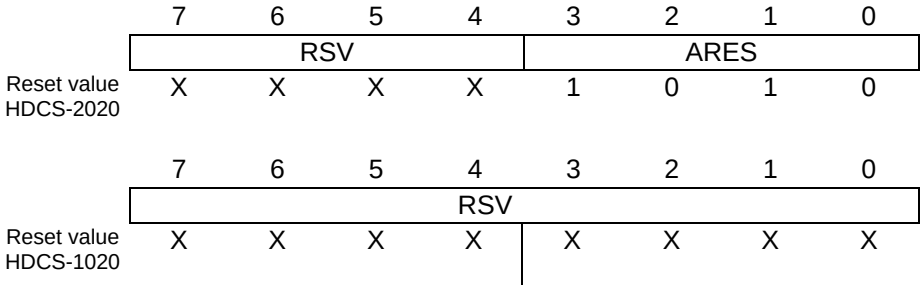

Figure 13. ADC Control Register Format

Mnemonic	Read/Write Control	Description
ARES	R/W	ADC Conversion Resolution. **ARES** 0000: Reserved 0001 - 1010: Number corresponds to bits of ADC output resolution 1011 - 1111: Reserved Note: Legal settings in normal operation are 1000 - 1010. The ADC resolution impacts the minimum allowable column timing. Reserved for HDCS-1020
RSV	N/A	Reserved

Table 12. ADC Control Register Bit Descriptions

2.2.11 FWROW: First Window Row Register

This register is used to define the row address of the first row of the image window.

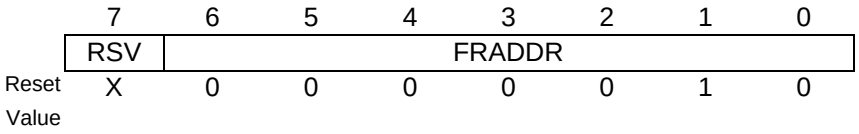

Figure 14. First Window Row Register

Mnemonic	Read/Write Control	Description
FRADDR[8:2]	R/W	First Row Address. Represents bits [8:2] of the address of first row of the image window. Bits [1:0] of the first row address are hard wired as “00” to force the window to begin on an even row boundary that is a multiple of four. The legal range is from zero to the last row address minus three. 0<=FRADDR[8:0]<=LRADDR[8:0] - 3.
RSV	N/A	Reserved

Table 13. First Window Row Register Bit Descriptions

2.2.12 FWCOL: First Window Column Register

This register is used to define the address of the first column of the image window. When using the full array for image capture, the value should be zero.

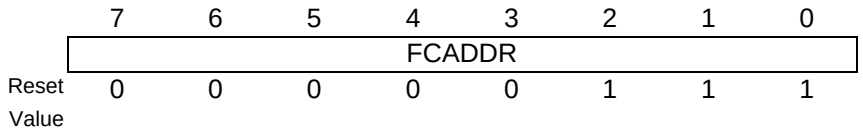

Figure 15. First Window Column Register Format

Mnemonic	Read/Write Control	Description
FCADDR	R/W	First Column Address. Represents bits [9:2] of the address of the first column of the image window. Bits [1:0] of the first column are hard wired as "00" to force the window on an even row boundary this is a multiple of four. The legal range of the first column address is from zero to the last column address minus the minimum number of columns in the image windows: 0<=FCADDR[9:0}<=LCADDR[9:0} - MINC + 1 where MINC represents the minimum number of columns in the image windows for the given operating mode and column timing. See "Column Timing Related Equations" for the equation for MINC.

Table 14. First Window Column Register Bit Descriptions

2.2.13 LWROW: Last Window Row Register

This register is used to define the address of the last row of the image window. When using the full array for image capture, the value should be the number of rows - 1.

	7	6	5	4	3	2	1	0
	RSV	LRADDR						
Reset value HDCS-2020t	X	1	1	1	1	0	0	1
HDCS-1020	X	1	0	0	1	0	0	1

Figure 16. Last Window Row Register Format

Mnemonic	Read/Write Control	Description
LRADDR	R/W	Last Row Address. Represents bits [8:2] of the address of the last row of the image window. Bits [1:0] of the last row address are hard wired as “11” to force the window to end on an odd row boundary that is a multiple of four minus one. The legal range is from the address of the first row plus three to the number of rows minus one. FRADDR[8:] + 3 <=LRADDR[8:0]<=number of rows in array - 1
RSV	N/A	Reserved

Table 15. Last Window Row Register Bit Descriptions

2.2.14 LWCOL: Last Window Column Register

This register is used to define the address of the last column of the image window. When using the full array for image capture, the value should be the number of columns - 1.

	7	6	5	4	3	2	1	0
	LCADDR							
Reset Value HDCS-2020	1	0	1	0	0	1	1	0
HDCS-1020	0	1	0	1	1	1	1	0

Figure 17. Last Window Column Register Format

Mnemonic	Read/Write Control	Description
LCADDR	R/W	Last Column Address. Represents bits [9:2] of the address of last column of the image window. Bits [1:0] of the last column address are hard wired as "11" to force the window to end on an odd column boundary that is a multiple of four minus one. The legal range of the last column address is from the first column address plus the minimum number of columns, to the number of columns in the array minus one. FCADDR[9:0] + MINC - 1<=LCADDR[9:0]<= number of columns in array – 1 where MINC represents the minimum number of columns in the image windows for the given operating mode and column timing. See "Column Timing Related Equations" for the equation for MINC.

Table 16. Last Window Column Register Bit Descriptions

2.2.15 TCTRL: Timing Control Register

	7	6	5	4	3	2	1	0
	ASTRT		PSMP					
Reset Value	0	0	0	0	0	1	1	0
HDCS-2020								
HDCS-1020	0	0	0	0	0	1	0	0

Figure 18. Timing Control Register Format

Mnemonic	Read/Write Control	Description
PSMP	R/W	PGA Sample duration. The number represents the number of clock cycles that the PGA sample signal is asserted. Valid numbers range from 4 to 31 where PSMP + CTO + 1>= ARES.
ASTRT	R/W	ADC Start Signal Duration. **ASTRT adcStart Signal Duration ADC Sample Duration** 00: 2 clock cycles 1 clock cycle 01: 3 clock cycles 2 clock cycles 10: 4 clock cycles 3 clock cycles 11: 5 clock cycles 4 clock cycles

Table 17. Timing Control Register Bit Descriptions

2.2.16 ERECPGA: Even Row, Even Column PGA Gain Register

This register is used to set the PGA gain for pixels on even rows and even columns.

	7	6	5	4	3	2	1	0
	EEH	EREC						
Reset Value	0	0	0	0	0	1	1	0
HDCS-2020								
HDCS-1020	0	0	0	0	0	0	0	0

Figure 19. Even Row, Even Column PGA Gain Register Format

Mnemonic	Read/Write Control	Description
EREC	R/W	PGA gain for pixels on Even Rows and Even Columns. Legal values range from 0 to 127. PGA Voltage gain setting: Av = (1+19*n/127)*(EEH+1) where n = binary to decimal conversion of EREC
EEH	R/W	PGA Even row Even column High gain enable. When 1, the PGA gain value programmed in the EREC bit field is doubled. When 0, PGA gain value programmed in EREC bit field is used.

Table 18. Even Row, Even Column PGA Gain Register Bit Description

2.2.17 EROCPGA: Even Row, Odd Column PGA Gain Register

This register is used to set the PGA gain for pixels on even rows and odd columns.

	7	6	5	4	3	2	1	0
	EOH	EROC						
Reset Value HDCS-2020	0	0	0	0	0	1	1	0
HDCS-1020	0	0	0	0	0	0	0	0

Figure 20. Even Row, Odd Column PGA Gain Register Format

Mnemonic	Read/Write Control	Description
EROC	R/W	PGA gain for pixels on Even Rows and Odd Columns: Legal values range from 0 to 127. PGA Voltage gain setting: Av=(1+19*n/127)*(EOH+1) where n=decimal conversion of EROC
EOH	R/W	PGA Even row Odd column High gain enable. When 1, PGA gain value programmed in EROC bit field is doubled. When 0, PGA gain value programmed in EROC bit field is used.

Table 19. Even Row, Odd Column PGA Gain Register Bit Description

2.2.18 ORECPGA: Odd Row, Even Column PGA Gain Register

This register is used to set the PGA gain for pixels on odd rows and even columns.

	7	6	5	4	3	2	1	0
	OEH	OREC						
Reset Value HDCS-2020	0	0	0	0	0	1	1	0
HDCS-1020	0	0	0	0	0	0	0	0

Figure 21. Odd Row, Even Column PGA Gain Register Format

Mnemonic	Read/Write Control	Description
OREC	R/W	PGA gain for pixels on Odd Rows and Even Columns: Legal values range from 0 to 127. PGA Voltage gain setting: Av=(1+19*n/127)*(OEH+1) where n=decimal conversion of OREC
OEH	R/W	PGA Odd row Even column High gain enable. When 1, the PGA gain value programmed in the OREC bit field is doubled. When 0, PGA gain value programmed in OREC bit field is used.

Table 20. Odd Row, Even Column PGA Gain Register Bit Description

2.2.19 OROCPGA: Odd Row, Odd Column PGA Gain Register

This register is used to set the PGA gain for pixels on odd rows and odd columns.

	7	6	5	4	3	2	1	0
	OOH	OROC						
Reset Value HDCS-2020	0	0	0	0	0	1	1	0
HDCS-1020	0	0	0	0	0	0	0	0

Figure 22. Odd Row, Odd Column PGA Gain Register Format

Mnemonic	Read/Write Control	Description
OROC	R/W	PGA gain for pixels on Odd Rows and Odd Columns: Legal values range from 0 to 127. PGA Voltage gain setting: Av=(1+19*n/127)*(OOH+1) where n=decimal conversion of OROC
OOH	R/W	PGA Odd row Odd Column High gain enable. When 1, PGA gain value programmed in OROC bit field is doubled. When 0, PGA gain value programmed in OROC bit field is used.

Table 21. Odd Row, Odd Column PGA Gain Register Bit Description

2.2.20 ROWEXPL: Row Exposure Low Register

	7	6	5	4	3	2	1	0
	REXPL							
Reset Value	1	1	0	1	1	0	0	1
HDCS-2020								
HDCS-1020	0	0	1	0	1	1	0	0

Figure 23. Row Exposure Low Register Format

Mnemonic	Read/Write Control	Description
REXPL	R/W	Row Exposure Low Register. Least significant bits of the row exposure register (REXP[7:0]) formed by the concatenation of the ROWEXPH[6:0] and ROWEXPL[7:0] registers (i.e., REXP[14:0] = {ROWEXPH[6:0], ROWEXPL[7:0]}). In the “Normal” mode and “Shutter” mode, the row exposure register defines the number of row processing periods (see “Diagram of the Row Processing Period”) that the image is exposed. The legal range of values for the row exposure register is: 0<=ROWEXP[15:0]<=32,767.

Table 22. Row Exposure Low Register Bit Descriptions

2.2.21 ROWEXPH: Row Exposure High Register

	7	6	5	4	3	2	1	0
	RSV	REXPH						
Reset Value HDCS-2020	X	0	0	0	0	0	0	0
HDCS-1020	X	0	0	0	0	0	0	1

Figure 24. Row Exposure High Register Format

Mnemonic	Read/Write Control	Description
REXPH	R/W	Row Exposure High Register. Most significant bits of the row exposure register (ROWEXP[14:8]) formed by the concatenation of the ROWEXPH[6:0] and ROWEXPL[7:0] registers (i.e., REXP[14:0] = {ROWEXPH[6:0], ROWEXPL[7:0]}). In the “Normal” mode and “Shutter” mode, the row exposure register defines the number of row processing periods that the image is exposed. The legal range of values for the row exposure register is: 0<=ROWEXP[15:0]<=32,767.
RSV	N/A	Reserved

Table 23. Row Exposure High Register Bit Descriptions

2.2.22 SROWEXP: Sub-Row Exposure Register

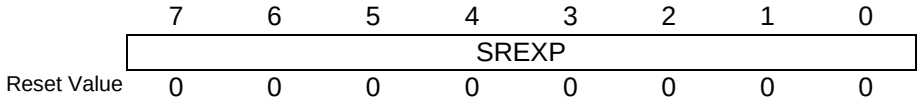

Figure 25. Sub-row Exposure Register Format

Mnemonic	Read/Write Control	Description
SREXP	R/W	Sub-row exposure register. Represents bits [9:2] of the sub-row exposure count used internally. Bits [1:0] is hard wired “00” such that the internal sub-row exposure value used is SREXP[9:0] = {SREXP[9:1],0,0} and the minimum granularity of the sub-row exposure count is four column timing periods. This register has no effect when operating in the “Shutter” mode and applies only to the “Normal” mode of operation. This register is used to specify the sub-row duration of time that each pixel is exposed before being sampled. The unit of measurement is one clock cycle. The legal range of values is: 0<=SROWEXP[9:0],<= NCTP - MNCT

Table 24. Sub-row Exposure Register Format

2.2.23 ERROR: Error Control register

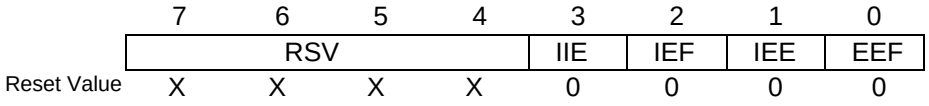

Figure 26. Error Register Format

Mnemonic	Read/Write Control	Description
EEF	R/W	Exposure error flag. When 1, indicates an exposure error was detected since the flag was last cleared. When 0, indicates no exposure error has been detected. Clear by writing a 1 to EEF flag and correcting the exposure settings.
IEE	R/W	Interrupt when exposure error occurs. When 1, an interrupt will be asserted when an exposure setting error has been detected. When 0, no interrupt will be asserted when an exposure setting error is detected.
IEF	R/W	Interface error flag. When 1, indicates an error was detected by the interface controller since the flag was last cleared. When 0, indicates no serial interface error has been detected since the flag was last cleared. Clear by writing a 1 to IEF.
IIE	R/W	Interrupt when interface error occurs. When 1, an interrupt will be asserted when an serial interface error has been detected. When 0, no interrupt will be asserted when a interface error is detected.
RSV	N/A	Reserved

Table 25. Error control register description

2.2.24 ITMG2: Interface Timing 2 Register

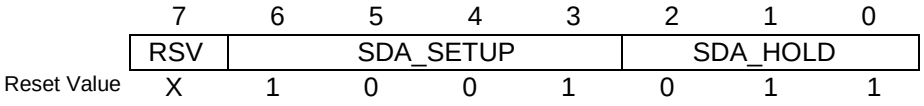

Figure 27. Interface Timing 2 Register Format

Mnemonic	Read/Write Control	Description
SDA_HOLD	R/W	SDA_HOLD controls the number of cycles after SCLK falls before the sensor stops driving the data on SDA. HOLD_CYCLES = 2 + (SDA_HOLD*2)
SDA_SETUP	R/W	When the sensor is driving a data bit, SDA_SETUP controls the number of cycles after SCLK falls until data is driven on SDA. SETUP_CYCLES = 2 + (SDA_HOLD*2) + (SDA_SETUP*2)
RSV	N/A	Reserved

Table 26. Interface Timing 2 Register bit description

2.2.25 ICTRL2: Interface Control 2 Register

	7	6	5	4	3	2	1	0
	DRD	FRMT	ROWT	RDYT	DATT	FSM	RSM	DSYNC
Reset Value	X	0	0	0	0	0	0	0

Figure 28. Interface Control 2 Register Format

Mnemonic	Read/Write Control	Description
DSYNC	R/W	Data synchronization mode. When set, nROW, nFRAME_nSYNC and nIRQ_nCC are synchronized with DATA
RSM	R/W	Row synchronization mode. It is used only when DSYNC is set. When 0, nROW asserts when the first DATA of row is transferred. When 1, nROW asserts when last DATA of row is transferred.
FSM	R/W	Frame synchronization mode. It is used only when DSYNC is set. When 0, nFRAME asserts when the first DATA of frame is transferred. When 1, nFRAME asserts when last DATA of frame is transferred.
DATT	R/W	Tristates DATA output. When 1, DATA outputs are tristated.
RDYT	R/W	Tristates DRDY output. When 1, DRDY is tristated..
ROWT	R/W	Tristates nROW output. When 1, nROW is tristated..
FRMT	R/W	Tristste nFRAME_nSYNC output. When 1, nFRAME_NSYNC is tristated.
DRD	R/W	Delay DRDY output. When 0, DRDY output switches relative to the rising edge of the system clock. When 1, to the falling edge.

Table 27. Interface Control 2 Register Bit Descriptions

2.2.26 HBLANK: Horizontal Blank Register

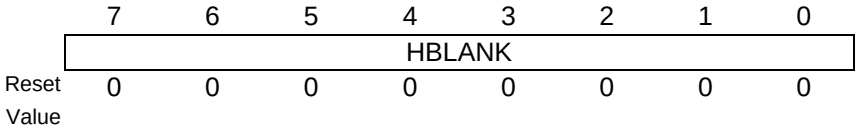

Figure 29. Horizontal Blank Register Format

Mnemonic	Read/Write Control	Description
HBLANK	R/W	Horizontal blank time. This register value represents the number of clock cycles that is added to the internally controlled minimum horizontal blank interval. Legal values range from 0 to 255.

Table 28. Horizontal Blank Register Description

2.2.27 VBLANK: Vertical Blank Register

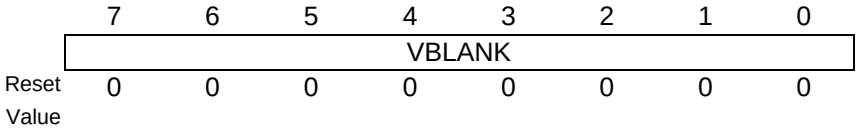

Figure 30. Vertical Blank Register Format

Mnemonic	Read/Write Control	Description
HBLANK	R/W	Vertical blank time. This register value represents the number of row processing time intervals used to either create or increase the vertical blanking interval independently of the configured integration time. Legal values range from 0 to 255.

Table 29. Vertical Blank Register Description

2.2.28 CONFIG: Configuration Register

The configuration register is used to select the method of image capture to be used.

	7	6	5	4	3	2	1	0
	RSV	SDOE	RSS	CSS	CFC	SFC	SEN	MODE
Reset Value HDCS-2020	X	0	0	0	1	1	0	0
HDCS-1020	X	0	0	0	1	1	X	0

Figure 31. Configuration Register Format

Mnemonic	Read/Write Control	Description
MODE	R/W	Operating mode select. **MODE** 0: Normal operation mode. 1: Shutter mode.
SEN	R/W	Reserved for HDCS-1020 Single Channel Enable. When 1, single channel Mode is enabled. SEN mode reduces the data output and frame rate to half.
SFC	R/W	Stop when Frame Complete. When 1, the internal timing controller will complete processing the current frame before stopping following de-assertion of the RUN control bit. When 0, the internal timing controller will stop execution immediately upon de-assertion of the RUN control bit. Data currently in the image pipe will be output.
CFC	R/W	Continuous Frame Capture: 1 forces continuous multiple frame capture when RUN flag asserted. 0 forces single frame image capture when RUN flag asserted.
CSS	R/W	Column Sub-Sample enable. When 1, one half of the columns in the image window are processed. When 0, all columns in the image window are processed.
RSS	R/W	Row Sub-Sample enable. When 1, one half of the rows in the image window are processed. When 0, all rows in the image window are processed.
SDOE	R/W	Serial data output enable. When 1, DATA[1] is used as SD0, serial data output for the even channels, DATA[1] is used as SD1, serial data output for the odd channels. When 0, DATA[7:0] is used as the parallel data outputs.
RSV	N/A	Reserved

Table 30. Configuration Register Bit Descriptions

2.2.29 CONTROL: Control Register

The configuration register is used to initiate and monitor an image capture process, and control the reset and power up state of the chip.

	7	6	5	4	3	2	1	0
	RSV		PWR	LCK	ARST	RUN	SLP	RST
Reset Value	X	X	1	0	0	0	0	0

Figure 32. Control Register Format

Mnemonic	Read/Write Control	Description
RST	R/W	Hardware Reset. When 1, an internal hardware reset is asserted. When 0, does not assert an internal hardware reset.
SLP	R/W	Sleep mode enable. When 1, internal sleep mode is asserted, the internal timing controller clocks and state machines are disabled, and power to the analog sections blocks is disabled. When 0, internal sleep mode is not asserted.
RUN	R/W	Run enable. Transition from 0 to 1 initiates the configured image capture process which may be single or multiple frames depending on the state of the CFC control bit. Normal termination of a single frame image capture process automatically drives RUN to a 0. When 1, writing a 0 to RUN posts a request to the internal timing controller to stop the current image capture process. Depending on the state of the SFC bit, the stop request will be executed immediately or at the next frame boundary.
ARST	R/W	Global Array Reset. When 1, enable the pixel array to be globally reset.
LCK	R/W	Register lock. When 1, internal shadow registers will retain their values and modifications to the main register settings will be ignored. When 0, the main register values will be sampled synchronously to internal timing controller cycles.
PWR	R/W	Low Power Mode. When 1, as RUN is deasserted, the power to the analog modules is disabled, and the clocks to all of the digital logic(except the serial interface and control registers)are disabled. Hence, when the HDCS is reset, (PWR=1), the control register is the only writable register. In order to write to the other registers, PWR has to be deasserted. When 0, low power mode is not asserted.
RSV	N/A	Reserved

Table 31. Control Register Bit Descriptions

3. Programming Reference

3.1 Programming Reference Overview

The HDCS sensor supports a wide variety of operating modes, window sizes and locations, exposure control settings, timing control settings, analog to digital conversion settings, and data output format settings. Operation of the system is primarily controlled by a set of internal registers that must be initialized to the desired settings prior to use. All register reads and writes occur via one of two user selectable serial communication interfaces, both of which support multiple user configurable data rates and operating modes. When an image capture process is running, image data is output from the HDCS Sensor via the parallel interface. Depending on the programmed operating mode and exposure settings, data may be output in bursts or a steady stream.

3.2 Windowing and Panning

The HDCS sensor supports a very flexible windowing and panning scheme in that numerous windows sizes, aspect ratios, and positions are supported. The image window can be placed virtually anywhere within the boundaries of the array.

3.3 Programmable Gain Settings

The material used to create color filter patterns such as the RGB Bayer pattern combined with the frequency response of the photodiodes combine to produce different degrees of sensitivity to red, green and blue light. The HDCS sensor allows the host to compensate for these differences, if necessary, by allowing four different gain settings independently programmed via the four PGA gain registers. The gain values are applied as even row even column, even row odd column, odd row even column, and odd row odd column. Since the programmable gain settings modify the resulting signal levels driving the on-chip ADC/S, the gain settings should be factored into the exposure control algorithm.

The voltage gain settings are given by:

Gain = [1 + (19 * n / 127)] * [m + 1]

where “n” is the number defined by the seven least significant bits of the corresponding gain register (i.e., n = ERECPGA[6:0], EREOCPGA[6:0], ORECPGA[6:0], or OROCPGA[6:0]) and “m” is the most significant bit of the same register (i.e., M=ERECPGA[7], EROCPGA[7], ORECPGA[7], or OROCPGA[7]).

For gain settings lower than 20 (decimal) , the best results will be obtained by setting “m” equal to zero. Also, for PGA gain settings higher than 10, it is recommended that the “PSMP” and “ASTRT” portions of the column timing period be increased over the minimum values.

3.4 Internal Timing Controller Operation

Once initiated, the internal timing controller generates all of the control signals and executes all of the sequences required to capture one or more frames of image data with minimal host system intervention. To initiate an image capture process, the host controller must first configure the register set and then assert the “RUN” bit of the “CONTROL” register. If the system is configured to capture a single frame, the timing controller will execute a finite sequence of operations and stop execution after outputting a single frame of data. If the system is configured to capture multiple frames, the timing controller will continue to sequence and output data until forced to stop by the host system. The host system can stop the HDCS sensor by de-asserting the “RUN” bit of the “CONTROL” register, asserting an internal or external reset, or asserting an internal or external low power mode condition.

The HDCS sensor supports multiple image capture modes classified as either a major or minor mode. Major modes define the general operation of an image capture process and are mutually exclusive in that only one mode can be applied at a time. Minor modes further refine the behavior of the major mode, can be applied to every major mode, affect the major mode operation in a similar manner, and are not mutually exclusive.

3.5 Power Saving Options

The HDCS Family of sensors offer a reduced power mode controlled by an external input signal and several user programmable reduced power modes.

3.5.1 Externally Controlled Power Saving Options

When asserted, the nRST_nSTBY input signal asserts an internal system reset which sets all registers and state machines to their default values. It also turns off the internal system clock and to the analog sub-systems.

The Sensor is not is not operational in this state and requires that the registers be reconfigured upon exit.

3.5.2 Internally Programmable Power Saving Options

The internally controlled power savings options are programmed via the system control register.

The low power mode is an operational mode which the sensor enters automatically when not in an image capture process. The chip remains in this “sleep” mode until the power mode is changed by the host system, or the host begins an image capture process. The sensor defaults to the low power mode on reset. This will cause the register clocks to be disabled except to the CONTROL register. The PWR bit in the CONTROL register must be cleared before one can write to the rest of the registers.

The sleep mode is a non-operational mode in which power to the analog sub-system is disabled and the clocks running all digital systems, except the host system interface and the CONTROL register, are disabled. The contents of the registers are preserved while in this mode.

3.5 Major Image Capture Modes

The major operating mode is selected by programming the “MODE” field of the “CONFIG” register. The two major image capture modes include the “Normal Mode” and “Shutter Mode”.

All image capture processes are initiated by the host system first configuring the register set (image window size and location, operating modes, exposure duration, gain settings, etc.) and then asserting the “RUN” bit of the “CONTROL” register. Internal circuitry generates all of the control signals necessary to address, sample, convert, and output one or more frames of image data with minimal host system interaction.

3.5.1 Normal Image Capture Mode

The “Normal” image capture mode is the default mode and is intended to be used for capturing high quality still or video images. The exposure duration is internally controlled by implementing a rolling electronic shutter that does not require the use of an external mechanical shutter or external flash. Following assertion of the “RUN” bit, the internal timing controller begins sequentially resetting rows in the selected image window to individually start the integration period of each row. To ensure that the integration period of all rows are equivalent, the rows are reset at a rate equal to the rate at which they will subsequently be sampled. All row operations occur in ascending order and wrap back to the first row in the image window after operating on the last row. When the first row in the image window has been exposed for the programmed duration, the system samples, converts, and outputs data for each row in ascending order. If they system is configured to capture one frame, this process automatically terminates upon

completion of the first frame. If it is configured to capture multiple frames, the process continues terminated by host interaction.

The vertical blanking register (VBLANK), row exposure registers (ROWEXP) and the number of rows in the image window determine the first frame and the inter-frame delay periods. The duration of the delays and it's timing can be classified into the following 4 groups.

1. ROWEXP >= #Rows, VBLANK >= ROWEXP+1 : The row exposure duration is larger than the time to process one frame. The VBLANK value is larger than the row exposure register plus one.
2. ROWEXP >= #Rows, VBLANK < ROWEXP+1 : The row exposure duration is larger than the time to process one frame. The VBLANK value is less than the row exposure register plus one.
3. ROWEXP <= #Rows, VBLANK >= ROWEXP+1 : The row exposure duration is less than the time to process one frame. The VBLANK value is larger than the row exposure register plus one.
4. ROWEXP <= #Rows, VBLANK < ROWEXP+1 : The row exposure duration is less than the time to process one frame. The VBLANK value is less than the row exposure register plus one.

The basic principle in the interaction between ROWEXP, VBLANK and #rows are, in order of decreasing priority:

1. The exposure duration for each row must equal to the ROWEXP+1
2. The first frame and inter-frame delays are determined by VBLANK

The first frame and inter-frame delays can be more than VBLANK if condition 1 is not met.

When VBLANK>ROWEXP+1, regardless of the exposure duration against the time it takes to sample a frame, the first frame delay is determined by the VBLANK register value. When VBLANK<ROWEXP+1, the first frame delay is determined by ROWEXP+1. When the exposure duration is more than the time it takes to sample a frame, the inter-frame delay is determined by the larger of VBLANK and ROWEXP+1- #rows. When the exposure duration is less than the time it takes to sample a frame, the inter-frame delay is determined by VBLANK.

The following diagram columns "exposure reset row" and "sample reset row" are referring to the row number that is being reset to start the exposure period, and the row number that is being sampled. In equation format, the first and last rows in the image window are referred to as "n" and "m" respectively. The row exposure count is referred as "R". Equations are enclosed in parenthesis. Values enclosed in the square brackets are row numbers based on the assumption that n=0, m=7, and R=2.

When the inter-frame delay is present, the image data will be output in single frame bursts with a delay between each burst. When the row exposure duration is larger than the time it takes to process one frame, if enabled and configured as the shutter sync signal, the nFRAME_nSYNC signal will be asserted at the end of the exposure reset period to facilitate operation of an external shutter or flash. When the exposure duration is not greater than the time required to process one frame, the shutter sync signal will not be asserted.

The sample reset occurs during the row sample portion of the row processing time and occurs immediately after the row is sampled (i.e., the end of the integration time for that row). Similarly, the exposure reset essentially marks the start of the integration time for the row that is reset. The column processing time is a function of the number of columns in the image window, the programmed column timing, and the column sub-sampling mode.

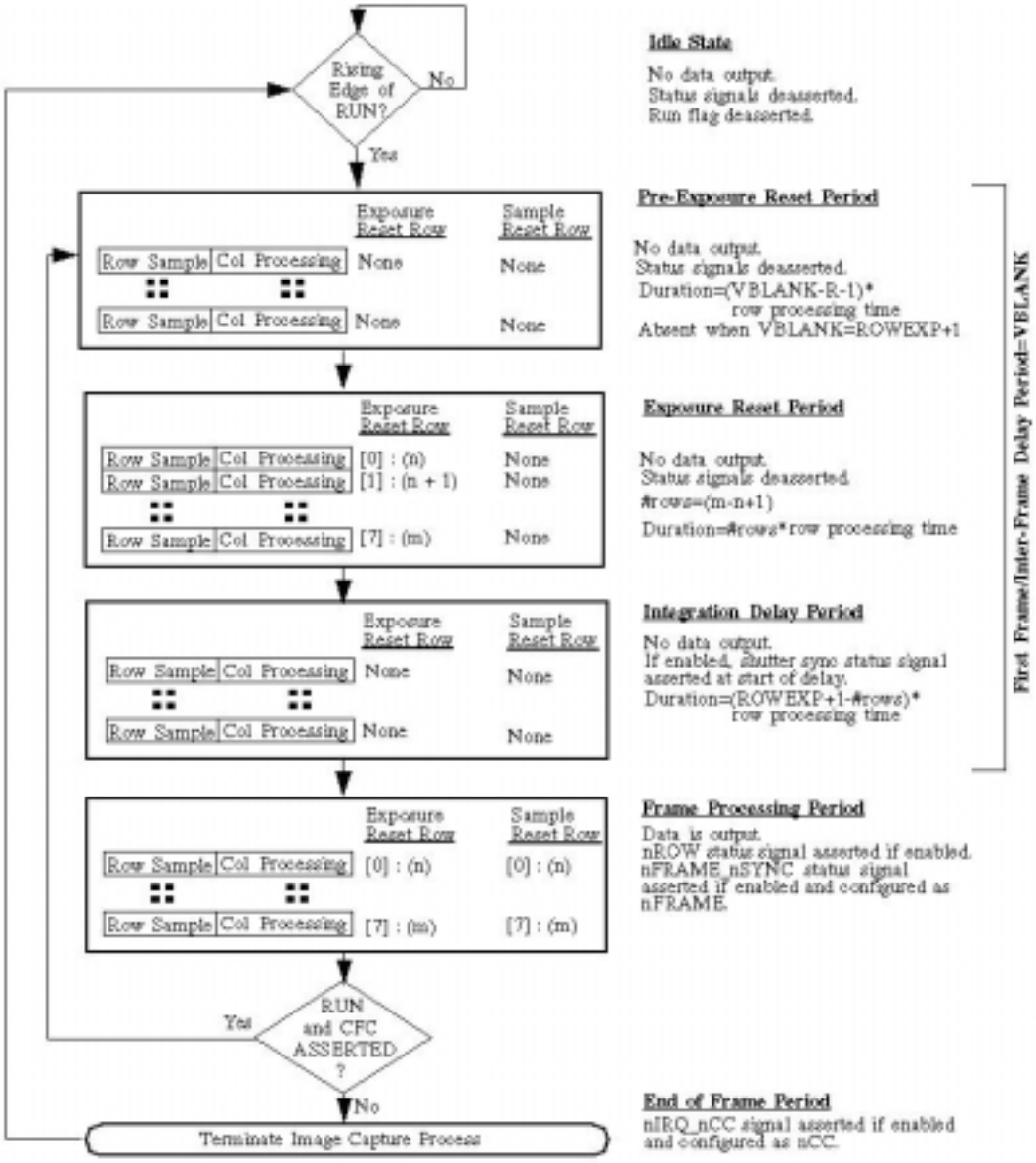

Figure 33. Normal Mode Image Capture Process with ROWEXP>=#rows and VBLANK>=ROWEXP+1

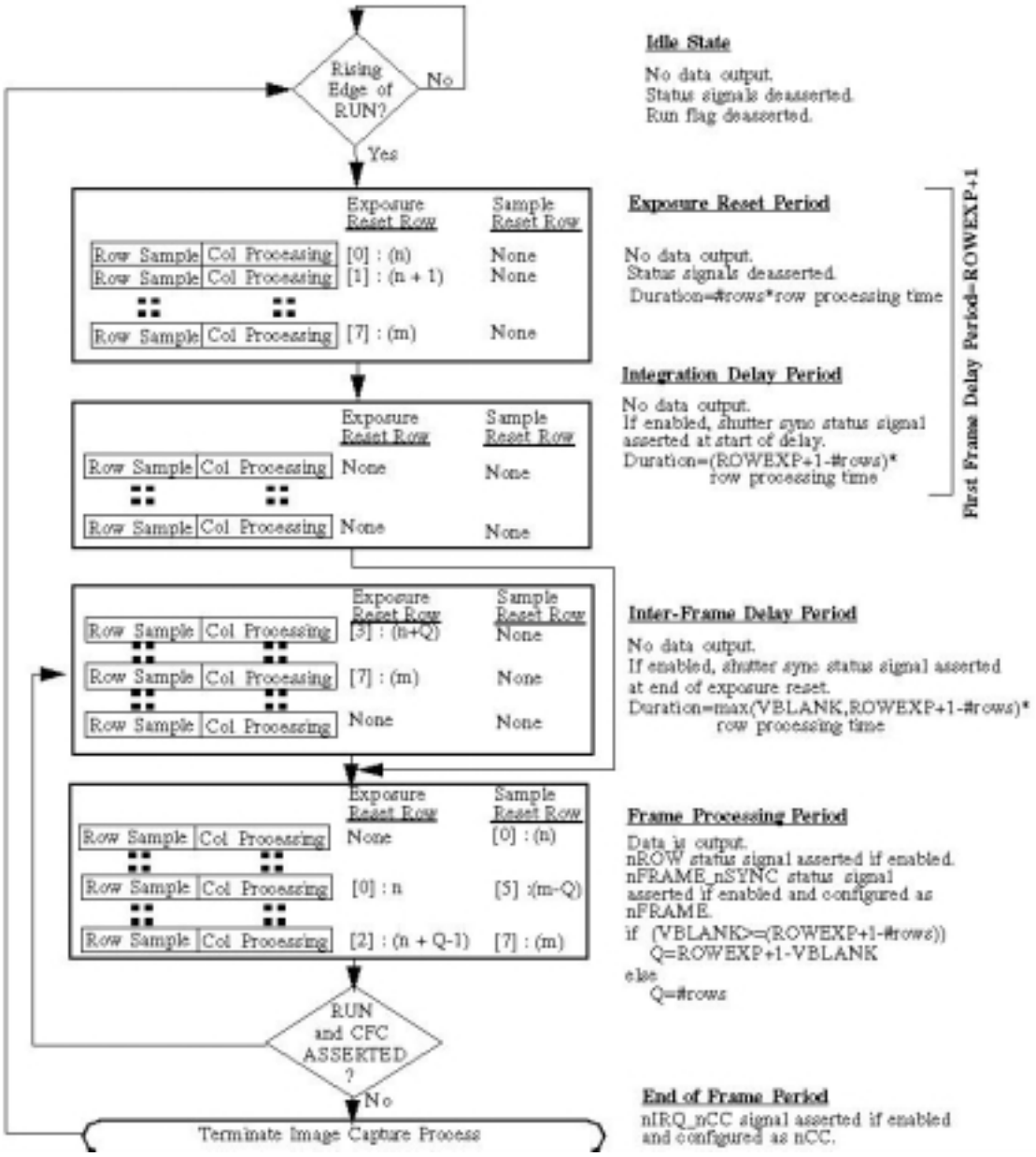

Figure 34. Normal Mode Image Capture Process with ROWEXP>=#rows and VBLANK<ROWEXP+1

The following diagram depicts the sequence of operations for a “Normal” mode image capture process with an exposure duration less than the time required to process one frame. The diagram columns “Exposure Reset Row” and “Sample Reset Row” are referring to the row number that is being reset to start the exposure, and the row number that is being sampled. In equation format, the first and last rows in the image window are referred to as “n” and “m” respectively. The row exposure count is denoted by “R”. Equations are enclosed in left and right parenthesis. Values enclosed in square brackets represent a row number based on the assumption that n=0, m=7, and R=2.

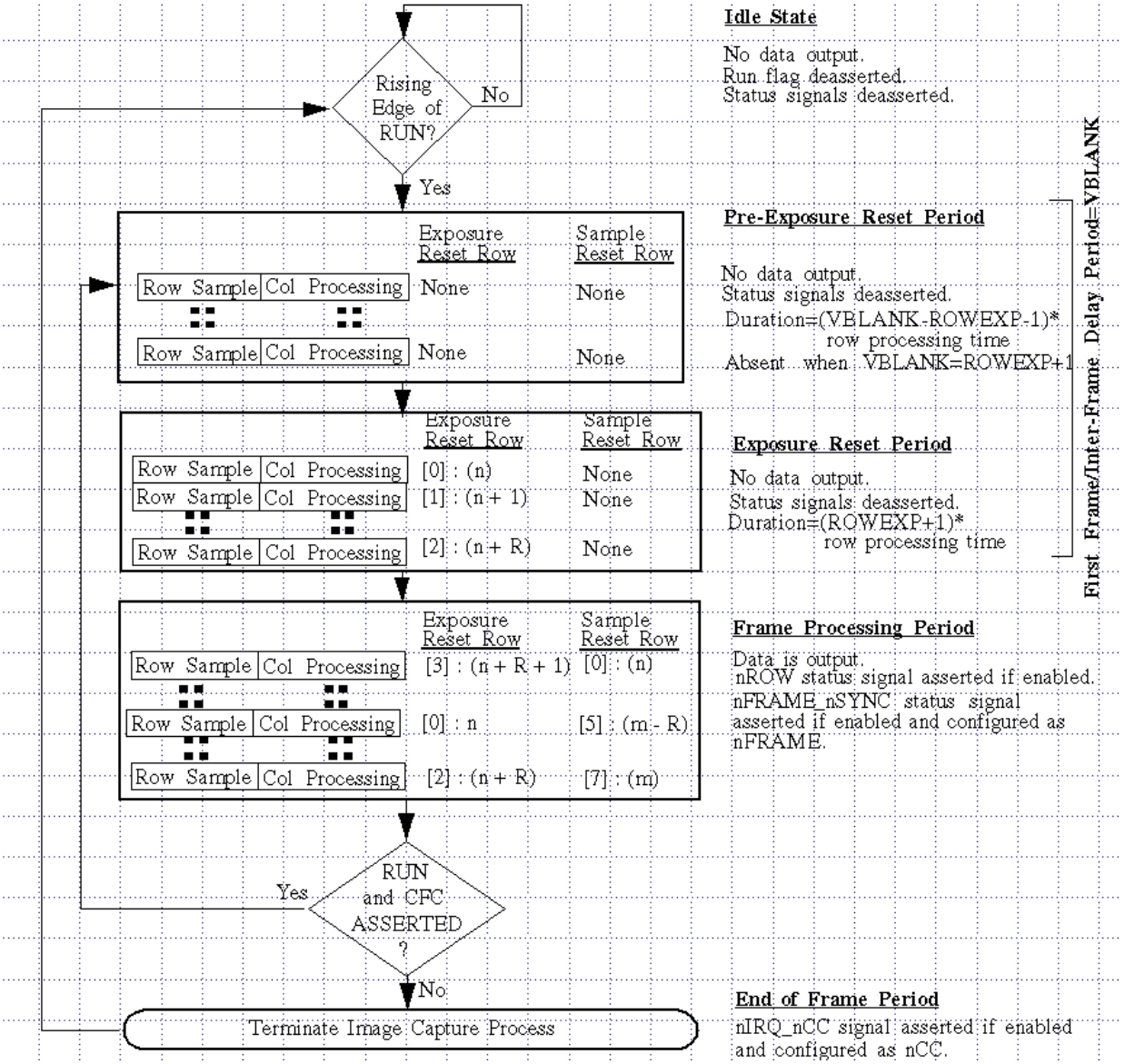

Figure 35. Normal Mode Image Capture Process (ROWEXP, #Rows, VBLANK>=ROWEXP+1)

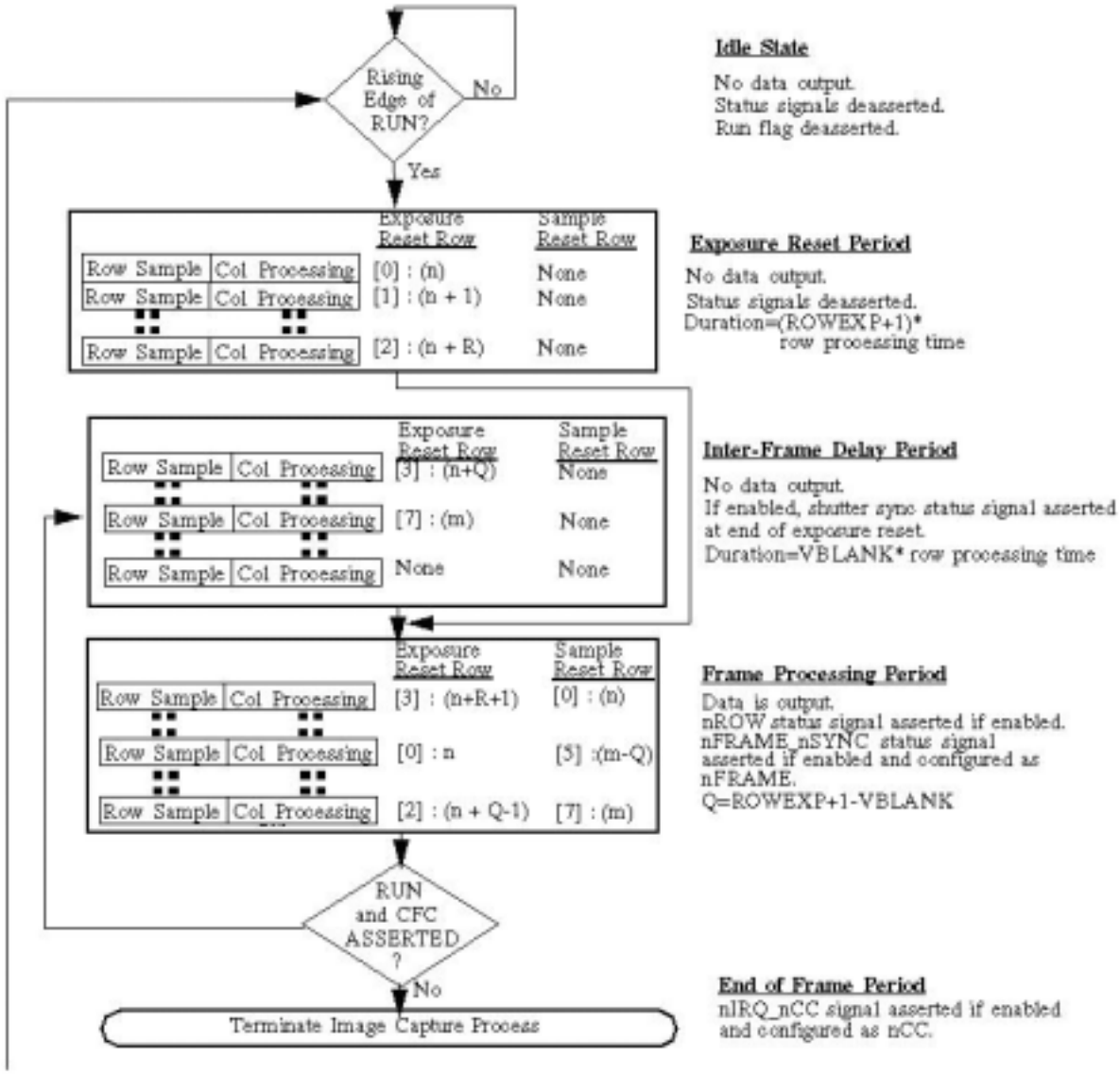

Figure 36. Normal Mode Image Capture Process (ROWEXP< #Rows, VBLANK<ROWEXP+1)

3.5.2 Shutter Mode Image Capture Process

The “Shutter Mode” image capture mode is intended to be used for capturing high quality still or video images in conjunction with an external shutter or flash. The basic sequence of operations is to execute a “fast rolling rest” on all rows in the image window, assert the shutter sync signal, delay a time duration programmed via the row exposure control registers (ROWEXPH and ROWEXPL), then sample, convert, and output the frame of data.

The objective of using the “fast rolling reset” is to minimize the pre-integration period and hence the latency between initiating the image capture process and when the shutter or flash can be opened. Due to the difference in duration of the row processing time and the time required to simply reset one row, the duration of time that each row is allowed to integrate is not equal. Rather, it increases from row to row in ascending order. As such, the dark current contribution is greater for the last row in the image window than the first. Obtaining high quality results in this mode requires that the dark current contribution be negligible relative to the light intensity when the shutter is opened or the flash is strobed. Also, if using a flash without a shutter, the ambient light level contribution must be negligible relative to the flash intensity.

Since the fast rolling reset is used to start integration of each row in this mode, there is no requirement to execute an exposure reset during the column processing time. As such, the minimum window size in this mode is reduced to the minimum window addressable via the register set.

In equation format, the first and last rows in the image window are referred to as “n” and “m” respectively, and the row exposure count is denoted by “R”. Equations are enclosed in left and right parenthesis. Values enclosed in square brackets represent a row number based on the assumption that n=0, m=7, and R=2.

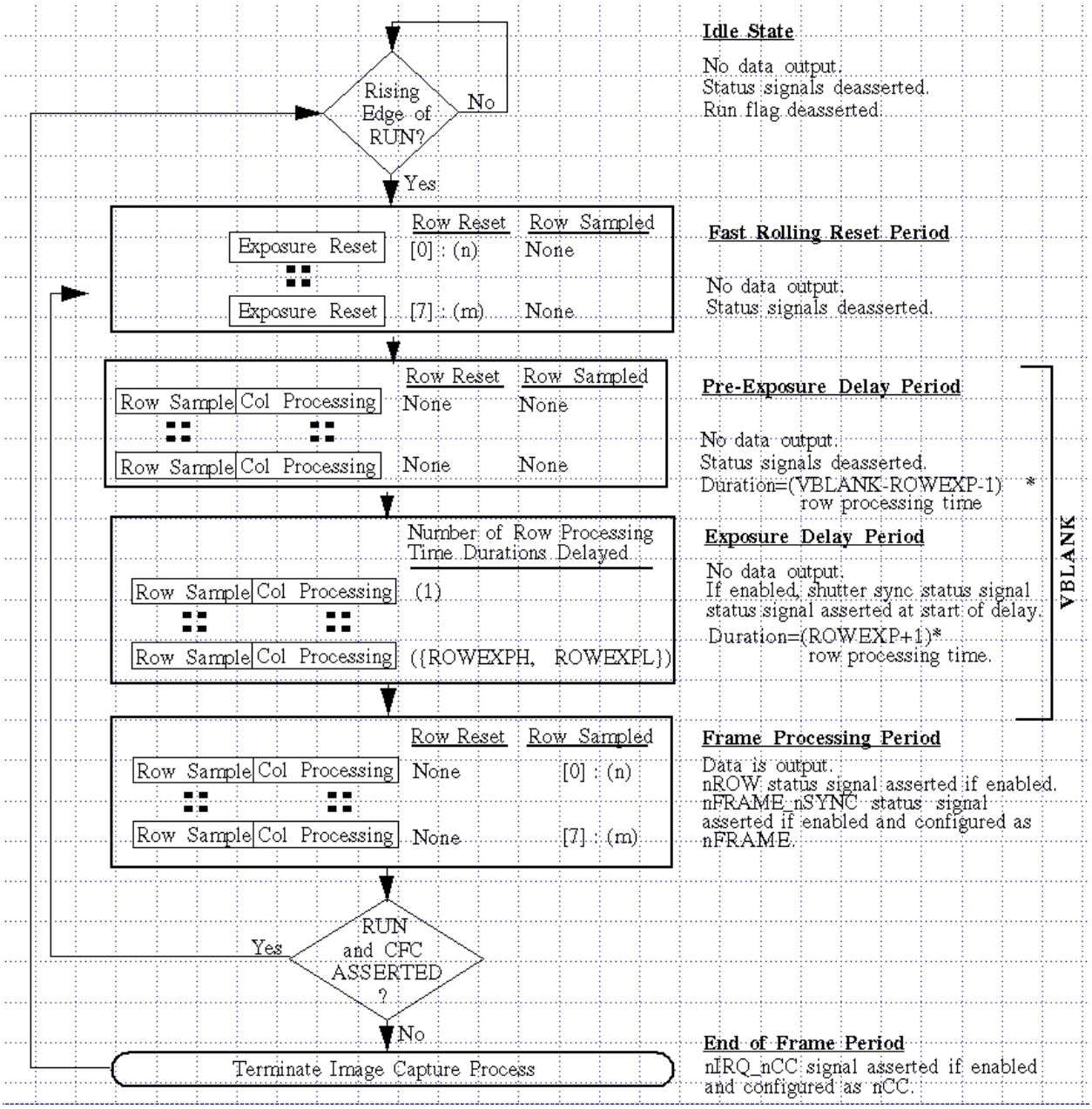

Figure 37. Graphical Depiction of the Shutter Mode Image Capture Process (VBLANK>ROWEXP+1)

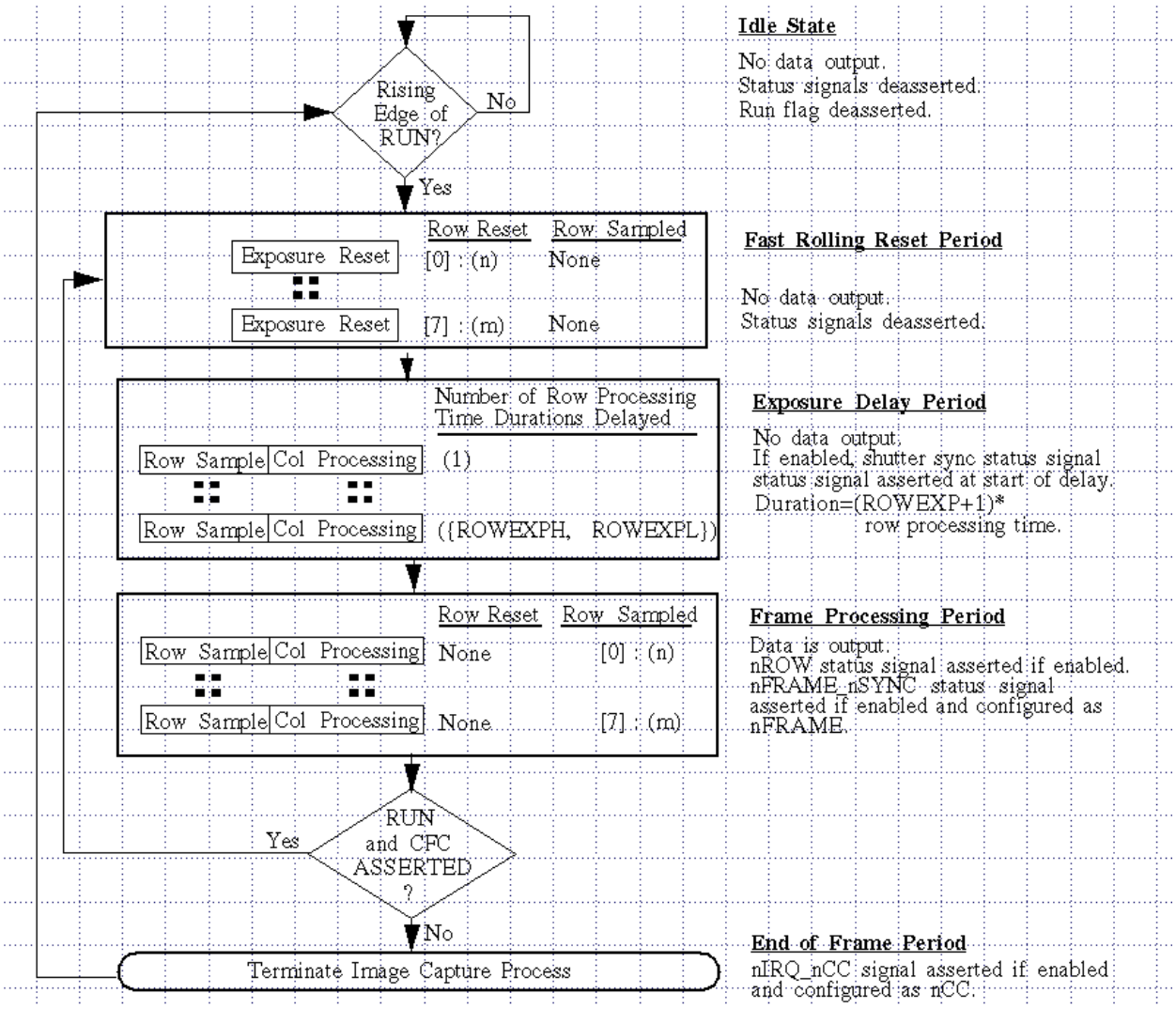

Figure 38. Graphical Depiction of the Shutter Mode Image Capture Process(VBLANK<ROWEXP+1)

3.5.3 Minor Image Capture Modes

Every minor operating mode can be applied to every major operating mode and have a similar affect on every major mode. Each minor mode can be enabled or disabled regardless of the state of other minor modes. Supported minor modes include row sub-sampling and single frame versus video mode. The state of each minor mode is controlled by fields in the "CONFIG" register.

3.5.3.1 Single Frame Versus Video Mode

The "CFC" field of the "CONFIG" register determines whether the system operates in single frame or video mode. Initiation of an image capture process when in single frame mode causes one frame of data to be output, after which the timing controller automatically terminates the image capture process. When in the video mode, the initiated image capture process will continue indefinitely until the host system intervenes by de-asserting the "RUN" bit in the "CONTROL" register, asserting a sleep condition, or asserting a reset condition.

3.5.3.2 Single Channel Mode (HDCS-2020 only)

The "SEN" field of the "CONFIG" register determines if the HDCS-2020 is in single channel mode.
When single channel mode is enabled, the column processing time is doubled which has the result of reducing the frame rate and data rates.

3.5.3.3 Row and Column Sub-Sampling Modes

The row and column sub-sampling modes can be used to implement a zoom feature, support exposure and focus algorithms, or simply as a means to create “fun house” style images for the end user. Sub-sampling modes are controlled by the “RSS” and “CSS” fields of the “CONFIG” register.

When both the row and column sub-sampling modes are disabled, every pixel within the defined image window is sampled during an image capture process. Enabling sub-sampling reduces the number of pixels sampled per frame by a factor of two. However, the impact on the actual frame rate and data rate depends on the major operating mode, the exposure register settings, the size of the image window, and the selected column timing. In general, sub-sampling will increase the frame rate.

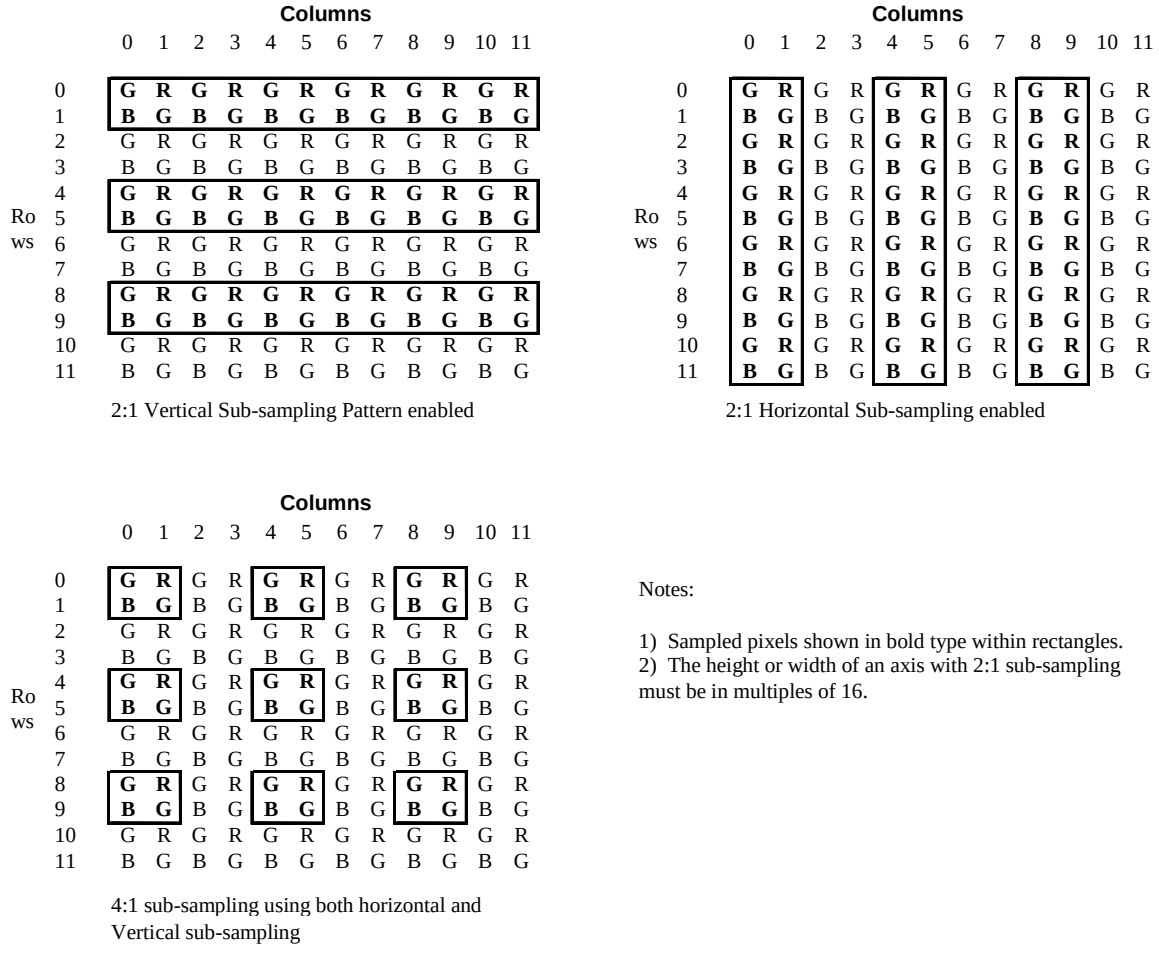

Figure 39. Sub-Sampling Patterns

3.5.4 Basic Timing Controller Operations

The internal operation of the timing controller, and hence the rate and timing of data output, is deterministic and can be calculated. The objective of this section is to describe the timing of the basic sequences and the registers that affect them.

3.5.4.1 Row Processing Period

The period of time required to process one row is a fundamental piece of information required to correctly program the exposure duration and to understand the rate and timing at which data is output from the sensor. Rows are processed sequentially in ascending order. The data output rate and overall timing controller sequencing corresponds to the rate at which individual rows are processed. The rate at which rows are processed is highly programmable and depends on the image window size, whether sub-sampling is enabled, and the selected timing control parameters.

As shown below, row processing is comprised of three major portions called the “Horizontal Blanking Period”, “Row Sample Period” and the “Column Processing Period”. When operating in the “Normal Mode, an “Exposure Reset Period” occurs during the same time slots as the “Column Processing Period”. The sub-row exposure registers (SROWEXP) define the time delay from the start of the column processing period to the start of the exposure reset period and hence the sub-row component of the overall integration time. SROWEXP is specified in 4 column timing period units.

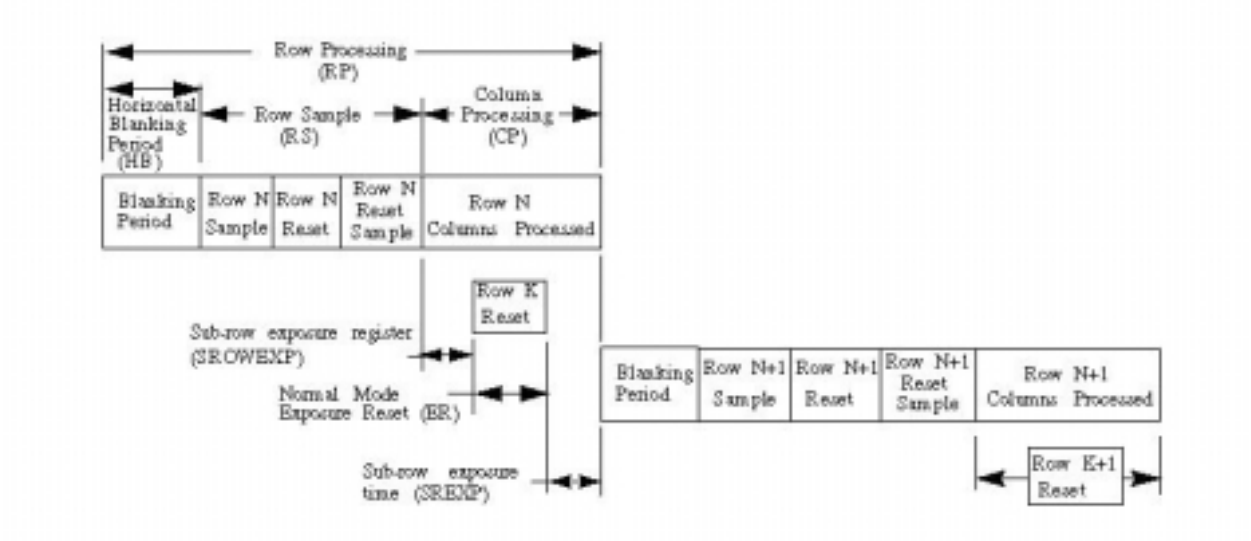

Figure 40. Diagram of the Row Processing Period

3.5.4.2 Row Sample Period

The row sample period is a constant duration regardless of the selected operating mode, image window size, or the programmed column timing. If current row has been fully exposed, it is sampled, reset, and sampled again to implement the double sampling feature. The reset that occurs in this time slot is referred to as the “sample reset”. If current row has not been fully exposed, the system does not actually sample or reset any rows, but simply delays an amount of time equivalent to what it would take to sample, reset, and sample again.

3.5.4.3 Column Processing Period

The analog to digital conversion of a row of sampled pixel data occurs during the column processing period. Data is also output from the chip during this period. The duration of time required to perform the column processing period of the row processing is highly programmable and depends on the number of columns in the image window, whether column sub-sampling is enabled and the selected column timing.

The column processing period begins with a constant duration overhead period following by some number of programmable duration column timing periods. The number of column timing periods ranges between two and the number of columns in the array and is user programmable based on the image window size and the operating mode. Regardless of the selected operating mode, columns are always processed and the data is always output in ascending order. Single channel mode is only for the HDCS-2020

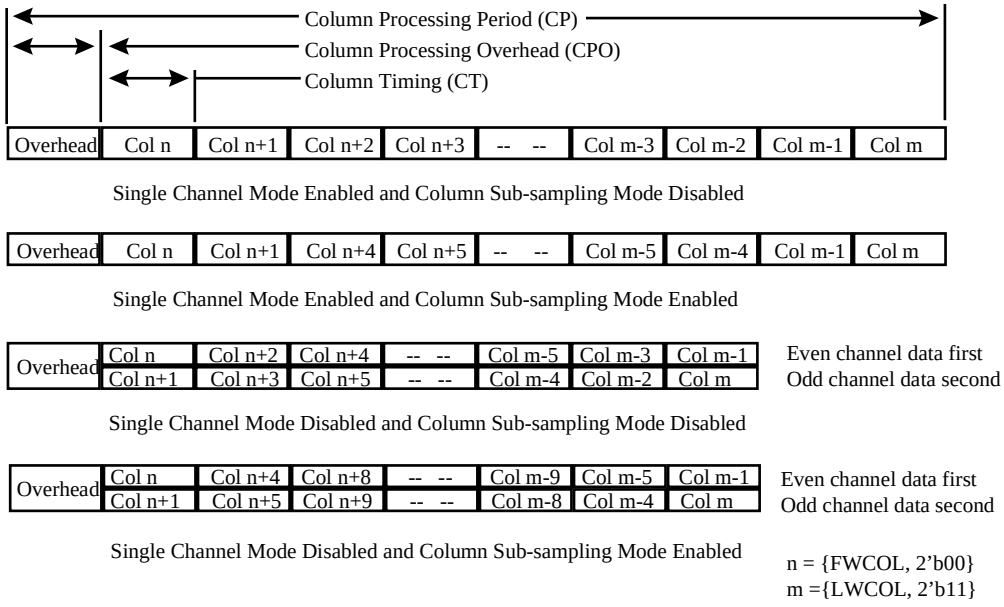

Figure 41. Column Processing Sequencing for Applicable Operating Modes

3.5.4.4 Column Timing Period

The column timing period is a basic unit of the column processing time and is comprised of a fixed duration overhead period and two independently programmable periods that can be used to vary the duration of each data conversion and output process. For any operating mode and image window size, increasing the column timing from the minimum will increase the row processing time, decrease the average data output rate, and decrease the frame rate. As such, the column timing can be used to scale the frame and data rates to match artificial lighting frequencies and host system bandwidth requirements.

The PGA Sample signal and ADC Start signal values are programmed via the “PSMP” and “ASTRT” fields of the timing control register. Note that the column timing period must be a minimum of 11 cycles when performing 10-bit A/D conversions.

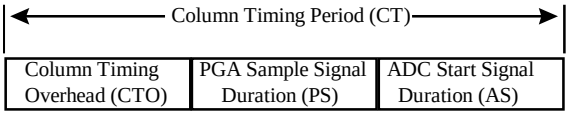

Figure 42. Column Timing Period

3.5.4.5 Frame Processing Period

The frame processing period is the period of time during which one frame of fully exposed data is sampled and output. The frame processing period is highly programmable and depends upon the size of the image window, the selected timing parameters, and whether row sub-sampling is enabled.

3.5.4.6 First Frame Delay Period

The first frame delay period defines the time when the RUN bit is set to the time that the data is output. The time duration is highly programmable and depends upon the row processing time, row exposure, and the vertical blanking register settings. The first frame delay period is determined by the larger of VBLANK and ROWEXP+1. This first frame delay period can be sub-divided into the pre-exposure period, the exposure period and the integration delay period. The pre-exposure period is present when VBLANK>ROWEXP+1. The exposure period is determined by the number of rows in the image window and the row processing time. The integration delay period is determined by (ROWEXP+1-#rows in image window) and the row processing time.

3.5.4.7 Inter-Frame Delay Period

The inter-frame delay period occurs between two frame processing periods. When VBLANK>ROWEXP+1, the delay period is determined by the VBLANK register. When VBLANK<ROWEXP+1, and the row exposure count is smaller than the time it takes to sample a frame, the delay is determined by the VBLANK register value. When VBLANK<ROWEXP+1, and the row exposure count is larger than the time it takes to sample a frame, the delay is determined by the larger of the VBLANK register value or the row exposure count. There is no data output during this time period and no rows are being sampled or reset. The inter-frame delay will be executed multiple times when operating in the video mode. The inter frame delay period can be sub-divided into the pre-exposure period, the exposure period and the integration delay period.

3.5.4.8 Fast Rolling Reset Period

The fast rolling reset period occurs only in the “Shutter Mode”. The duration of the fast rolling reset period is determined by the exposure reset duration, a fixed overhead per exposure reset, and the number of rows in the image

window that will be processed. During this period each row in the image window that will be processed is reset, starting with the first and continuing in ascending order.

3.5.4.9 Pre-exposure Delay Period

The pre-exposure delay period is determined by the difference between the VBLANK and the ROWEXP+1 values.

3.5.4.10 Exposure Delay Period

The exposure delay period occurs only in the “Shutter Mode” and the duration is determined by the row processing time and the row exposure register settings. To ensure that the shutter or flash do not conflict with the internal electronic shutter, the exposure delay should be configured to be the minimum setting that is greater than the time shutter will be opened or the flash asserted. To facilitate timing the opening of a shutter or assertion of a flash, a synchronization signal can be configured to be asserted at the beginning of the exposure delay period. This is accomplished by enabling the nFRAME_nSYNC output signal and configuring it for the nSYNC mode

3.5.5 Timing Equations

Symbol	Equation	Units	Description
T		Time	System clock period.
TSO	TSO = 1	Cycles	Timing controller start overhead. Delay from internal assertion of the RUN bit of the CONTROL register to when the timing controller starts operating.
ER	ER = 96	Cycles	Exposure reset duration.

Table 32. General Timing Controller Equations

Symbol	Equation	Units	Description
PI	PI = CP + (REXP * RP) if REXP <= NRP PI = CP + (NRP * RP) if REXP > NRP	Cycles	The pre-integration time occurs only in the "Normal" mode and depends on the row exposure settings and the row processing time.
IFD	IFD = 0 if REXP < NRP IFD = (REXP - NRP) + 1 if REXP >= NRP	Cycles	The inter-frame delay time occurs only in the "Normal" mode if the row exposure count exceeds the number of row processed minus one.
FP	FP = NRP * RP	Cycles	The frame processing time is defined by the number of rows processed and row processing time.
FRR	FRR = NRP * (ER + 4)	Cycles	The fast rolling reset period occurs only in the "Shutter" mode and is equal to the number of row processed times the exposure reset duration plus a constant.
ED	ED = REXP * RP	Cycles	The exposure delay occurs only in the "Shutter" mode and is equal to the row exposure count processed times the row processing time.
SDO	Normal Mode: SDO = TSO + PI + IFD + RS Shutter Mode: SDO = TSO + FRR + ED + RS	Cycles	The delay from the start of an image capture process to the first data output depends on the operating mode and row exposure settings.

Table 33. Operating Mode Timing Related Equations

Symbol	Equation	Units	Description
RS	RS = 155	Cycles	The row sample period is constant.
RP	RP = HB+RS + CP	Cycles	The row processing period is determined by the sum of the row sample and column processing periods.
RSSF	RSSF = 1 if RSS is "0" RSSF = 2 if RSS is "1"	Cycles	The row sub-sample scale factor is determined by the state of the row sub-sample enable (see the RSS field of CONFIG register).
NRP	NRP = [last row address - first row address + 1] / RSSF	Cycles	The Number of Rows Processed is determined by the vertical size of the image window and the state of the row sub-sample enable.

Table 34. Row Timing Related Equations

Symbol	Equation	Units	Description
CTO	CTO = 3	Cycles	Column timing overhead.
HB	0<=HB<=255	Cycles	Horizontal Blanking Period
PS	4 <= PS <= 63	Cycles	PGA sample signal duration defined by PSMP field of TCTRL reg. The PGA sample signal duration m
AS	2 <= AS <= 5	Cycles	ADC start signal duration defined by the ASTRT field of TCTRL reg.
CT	CT = CTO + PS + AS PS + CTO + 1 >= ARES	Cycles	The column timing period equals column timing overhead plus the PGA sample and ADC start signal duration. **Note:** The column timing period must be sufficient to allow for the ADC conversion time which depends on the operating mode.
CPO	CPO = 3	Cycles	The column processing overhead.
SCSF	SCSF = 1 if SEN = “1” SCSF = 2 if SEN= “0”	Cycles	The single channel scale factor is determined by the single channel mode enable.
CSSF	CSSF = 1 if CSS = “0” CSSF = 2 if CSS = “1”	Cycles	The column sub-sample scale factor is determined by the state of the column sub-sample enable (see the CSS field of CONFIG register).
NCP	NCP = [last column address - first column address + 1] / CSSF	Cycles	The number of columns processed is determined by the width of the image window and state of the column sub-sample enable.
CP	CP = CPO + (NCP * CT / SCSF)	Cycles	The column processing period is determined by the number of columns processed, the column processing overhead, and if single channel mode is enabled.
MINC	**Shutter Mode:** MINC >= 4 **Normal Mode:** MINC >= (ER +12) * SCSF * CSSF / CT	Cols	The minimum allowable number of columns in the image window (MINC) is a function of the major operating mode, the minor operating mode, and the selected column timing. Note: The number of columns in every image window is forced to be a multiple of four by the register set interface. If not an integer, or not a multiple of four, MINC must be rounded up to the next highest multiple of four that satisfies the expression for MINC.

Table 35. Column Timing Related Equations

Symbol	Equation	Units	Description
MNCT	MNCT >= (ER + 12) / CT **Note:** If not an integer, MNCT must be rounded up to the next highest integer that satisfies the expression for MINC.	CT	The minimum allowable number of column timing periods within the column processing period applies only to the “Normal” mode of operation when calculating the sub-row exposure register settings.
SROWEXP	0 <= SROWEXP*4 <= NCTP -MNCT	Cycles	The sub-row exposure register count is bounded by the duration of the column processing period.
NCTD	NCTD = SROWEXP*4	CT	The number of column timing periods of delay from the start of the column processing period to the start of the exposure reset is controlled by the sub-row exposure register settings.
SREXP	SREXP = CP - (NCTD * CT) - ER - 12 A simpler equation with an error (ERR) range of 0 <= ERR <= CT is: SREXP = CP - SROWEXP - ER - 6	Cycles	The sub-row exposure period applies only to the “Normal Mode” and is equal to the column processing time minus the sum of the sub-row exposure count and the minimum number of column timing periods required for the exposure reset period.
IEXP	IEXP = RS + (MNCT * CT)	Cycles	The duration of the illegal exposure reset time slot is equal to the sum of the row sample period and product of the minimum allowable number of column timing periods and the column timing period.
ROWEXP	ROWEXP = {ROWEXP, ROWEXPL}	Cycles	The row exposure count is equal to the number formed by the concatenation of the ROWEXPH and ROWEXPL registers.
EXP	Normal Mode: EXP = T * {SREXP + REXP * RP} Shutter Mode: EXP = T * REXP * RP	Time	In the “Normal” mode EXP represents the period of time that each pixel is exposed. In the “Shutter” mode, EXP represents the “Exposure Delay Period”

Table 36. Exposure Control Related Equations

3.5.6 Exposure Control

The term “exposure” refers to the duration of time between the point at which a pixel is reset and subsequently sampled. Another for this is the “integration time”. This section is intended to describe the mechanics of programming the HDCS sensor to expose each pixel for a pre-determined period of time. While methods of determining the correct exposure duration is not within the scope of this section, one should note that the PGA gain settings also factor into determining the correct exposure duration.

By default, pixels in the HDCS image sensor arrays are continuously integrating ambient light. During an image capture process, the period of time that a given row of pixels is integrated starts when an exposure reset is asserted and ends when either a sample reset is asserted and ends when a subsequent exposure reset is asserted. The time slot that an exposure (and sample) reset occurs in depends on the operating mode, but is of equal duration in all modes.

3.5.6.1 Shutter Mode Exposure Control

In the “Shutter Mode” a series of consecutive exposure resets, collectively called the “fast rolling reset”, are sequentially asserted in ascending order on individual rows within the image window boundary. The fast rolling reset occurs at the start of each captured frame. Note that in this mode the period of time between the exposure reset and the subsequent sample reset is not equal for each row and increases from the start of the frame to the end of the frame. For this mode to produce high quality pictures, the majority of the light integrated must be introduced during the exposure delay period by means of opening a mechanical shutter or timing the assertion of a bright flash of light.

The duration of the exposure delay period is primarily controlled by the row exposure register settings (ROWEXPH, ROWEXPL) which define the number of row processing periods to delay for. The row processing period is determined by the minor operating modes selected, the image window size, the selected column timing, and the system clock frequency. Since the exposure delay period is essentially an inter-frame delay, increasing the row exposure register value decreases the frame rate. Note that the sub-row exposure register settings have no effect in this mode of operation.

3.5.6.2 Normal Mode Exposure Control

In the “Normal Mode” each row is exposed for an equal time duration that is programmed via the row exposure, sub-row exposure, column timing, configuration, and window coordinate registers. The resulting exposure time is therefore a function of the size of the image window, whether or not sub-sampling is enabled, whether or not both PGA/ADC channels are used, and the period of time required to process each row in the image window. The time required to process each row is a function of the number of columns processed in the image window and the time required to process each column.

The row exposure registers define the number of row processing periods that each row is integrated for and therefore control the majority of the integration time. Note that the row exposure registers value can exceed the number of rows in the image window by a significant amount. When this occurs, a delay is inserted between each frame which decreases the frame rate from the maximum possible rate. As the name implies, the sub-row exposure registers provide exposure control granularity of fractions of row processing periods.

3.5.6.3 Sub-Row Exposure Control

The sub-row exposure registers only affect system behavior when operating in the “Normal” mode. In this operating mode, exposure resets are asserted during the column processing time slot. As such, the duration of the exposure reset defines the minimum acceptable column processing duration, and hence the minimum number of columns of the image window for a set of operating conditions and timing parameters. When image windows with a sufficient number of columns are used, the sub-row exposure registers ({SROWEXPH, SROWEXPL}) can be used to skew the assertion of the exposure reset within the column processing time to provide for sub-row granularity of the integration time. While the sub-row exposure register is programmed in units of clock cycles, the initiation of the exposure reset is internally synchronized within the column timing time slot which results in an effective granularity

of one column timing period. Note that increasing the sub-row exposure register value increases the delay from the start of column processing to the start of the exposure reset, and therefore decreases the sub-row exposure time.

Should the host system program an incompatible configuration such that either the exposure reset does not fit within the column processing time slot, or the sub-row exposure register values are so large that the exposure reset is delayed past the end of the column processing time slot, an internal flag is asserted and can be used to notify the host system of the error condition. In the event an exposure reset error condition occurs, the “EEF” flag of the “ERROR” register will be asserted and will remain asserted until cleared by host system intervention. The system can also be programmed to generate an interrupt request when this flag is asserted.

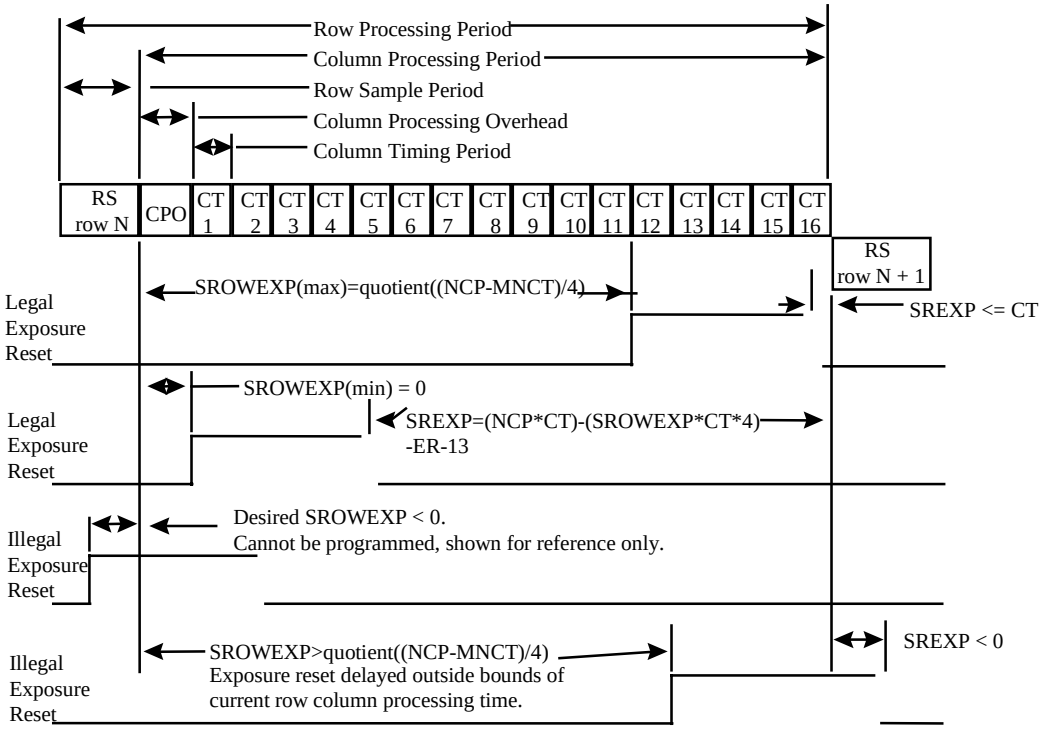

Figure 43. Sub-Row Exposure Control

3.5.6.4 Determining the Normal Mode Exposure Register Settings

Assuming the desired integration time is known, an integral number of clock cycles, and represented by “TEXP”, the row exposure register formed by the concatenation of ROWEXPH and ROWEXPH should be loaded with the integer quotient of the desired integration time divided by the time required to process one row;

ROWEXP = {ROWEXPH, ROWEXPL} = quotient {TEXP / (T * RP)}

Letting the remaining integration time be represented by SREXP, the sub-row exposure (SROWEXP) register should be loaded with a value determined by the following equations:

SREXP = TEXP / T - (ROWEXP * RP)

SROWEXP = quotient((NCP*CT-SREXP-ER-13)/(4*CT)

A negative SROWEXP value resulting from the above calculation indicates that desired integration time, combined with the configured row processing time, corresponds to an illegal value. A value greater than the legal range indicates an attempt to skew the exposure reset into the sample reset time.

4. Interface Reference

4.1 System Configuration

4.1.1 Serial Interface

When IMODE equals “0” the serial interface operates as a synchronous serial slave. The 7 bit device address is ‘101_0101’. The device address may be ignored by setting the DAD bit of the ICTRL register.

When IMODE equals ‘1’ and TCLK equals ‘0’ the serial interface operates as a half duplex UART slave. After system reset the UART operates at 9600 baud. Register writes to the BRATE and BFRAC registers can increase the BAUD rate.

4.1.2 Pad Speed

The PDRV register controls the switching speed of the HDCS sensor output pins. There are four groupings of output pins that can be controlled independently: DATA, DRDY, TxD, and STATUS. The STATUS group includes nROW, nFRAME_nSYNC, and nIRQ_nCC. Each group has 4 possible switching speed options. After system reset, the output pins are initialized to the fastest switching speed.

Since faster switching pads generate a small amount of noise, it is possible that under some conditions image quality could be enhanced by slowing the switching speed of the output pins.

4.1.3 Status Flags

There are three status output pins: nROW, nFRAME_nSYNC, and nIRQ_nCC. The status flags are all active low.

RCE	LVR	DSYNC	RSM	ROWT	Mode: Notes
‘0’	‘x’	‘0’	‘x’	‘0’	nROW Disabled. Drives a constant ‘1’.
‘1’	‘0’	‘0’	‘x’	‘0’	nROW pulse mode. Assert low for 4 cycles after trailing edge of last DRDY of row.
‘1’	‘1’	‘0’	‘x’	‘0’	nROW level mode. Assert low on leading edge of first DRDY of row. De-assert on trailing edge of last DRDY of row.
‘1’	‘0’	‘1’	‘0’	‘0’	nROW Start-of-Row DSYNC pulse mode. Assert low when first DATA of the row is transferred.
‘1’	‘0’	‘1’	‘1’	‘0’	nROW End-or-Row DSYNC pulse mode. Assert low when last DATA of the row is transferred.
‘1’	‘1’	‘1’	‘x’	‘0’	nROW DSYNC level mode. Assert low when first DATA of row is transferred. De-assert after last DATA of row is transferred.
‘x’	‘x’	‘x’	‘x’	‘1’	nROW is tristated.

Table 37. NROW Status Flag Control

FSE	FSS	LVF	DSYNC	FSM	FRMT	Mode: Notes
'0'	'x'	'x'	'0'	'x'	'0'	nFRAME_nSYNC is disabled. Drives a constant '1'.
'1'	'1'	'0'	'0'	'x'	'0'	nSYNC Pulse Mode. Assert 4 cycle active low pulse at the start of integration.
'1'	'1'	'1'	'x'	'x'	'0'	nSYNC Level Mode. Assert low at start of integration. De-assert on first DRDY leading edge.
'1'	'0'	'0'	'0'	'x'	'0'	nFRAME Pulse Mode. Assert low for 4 cycles after the trailing edge of last DRDY of frame.
'1'	'0'	'1'	'0'	'x'	'0'	nFRAME Level Mode. Assert low on leading edge of first DRDY of the frame. De-assert on trailing edge of last DRDY of the frame.
'1'	'1'	'1'	'1'	'x'	'0'	nSYNC DSYNC Level Mode. Assert low at start of integration. De-assert on start of first DATA transfer.
'1'	'0'	'0'	'1'	'0'	'0'	nFRAME Start-of-Frame DSYNC Pulse Mode. Assert low when the first DATA of the frame is transferred.
'1'	'0'	'0'	'1'	'1'	'0'	nFRAME End-of-Frame DSYNC Pulse Mode. Assert low when the last DATA of the frame is transferred.
'1'	'0'	'1'	'1'	'x'	'0'	nFRAME DSYNC Level Mode. Assert low when first data for a frame is transferred. De-assert after last data for a frame is transferred.
'x'	'x'	'x'	'x'	'x'	'1'	nFRAME is tristated.

Table 38. nFRAME_nSYNC Status Flag Control

ICE	IPD	LVC	DSYNC	Mode: Notes
'0'	'0'	'x'	'0'	Open Drain IRQ (interrupt request) with weak pull-up. Interrupt sources are in the STATUS register. Interrupt masks are in the IMASK register.
'0'	'1'	'x'	'0'	IRQ (interrupt request) driving to full high and low levels. Interrupt sources are in the STATUS register. Interrupt masks are in the IMASK register.
'1'	'x'	'0'	'0'	nCC (capture complete) pulse mode. Assert low for 4 cycles when the capture process completes. (After last DRDY trailing edge)
'1'	'x'	'1'	'0'	nCC (capture complete) level mode. Assert low when RUN bit is set. De-Assert after capture completes. (After last DRDY trailing edge).
'1'	'x'	'0'	'0'	nCC (capture complete) DSYNC pulse mode. Assert low during last DATA of capture.
'1'	'x'	'1'	'0'	nCC (capture complete) level mode. Assert low when RUN bit is set. De-Assert after capture completes. (After last DATA for last frame is transferred).

Table 39. NIRQ_nCC Status Flag Control

CONFIG[CFC] continuous frame capture	CONFIG [SFC] stop when frame complete	Capture Complete when…
"0"	“0”	At end of the first frame if CONTROL [RUN] is not de-asserted. Immediately after CONTROL [RUN] is de-asserted. If frame is stopped due to de-assertion of CONTROL [RUN] then: 1) If data has been transferred for current sensor row, then assert nROW if in nROW pulse mode. 2) If data has been transferred for current frame, then assert nFRAME if in nFRAME pulse mode.
“0”	“1”	After last data is transferred for first frame is de-asserted in.
“1”	“0”	Immediately after CONTROL [RUN] is de-asserted. If frame is stopped due to de-assertion of CONTROL [RUN] then: 1) If data has been transferred for current sensor row, then assert nROW if in nROW pulse mode. 2) If data has been transferred for current frame, then assert nFRAME if in FRAME pulse mode.
“1”	“1”	After last data is transferred for frame that CONTROL [RUN] is de-asserted in.

Table 40. Capture Complete

4.1.4 DATA and DRDY Timing

The timing of the DATA and DRDY pins is set by the DSC field of the ICTRL register, and the RPC field and DHC fields of the IFTMG register. The DATA/DRDY timing is set relative to the column timing. Data for 8 pixels are transferred during each period of column timing. Column timing is set by the ASTRT and PSMP field of the TCTRL register.

4.1.5 DATA Formatting(For HDCS-2020 only)

The ARES field of the ADCCTRL register determines the number of bits of resolution produced by the ADC. Legal values are 8, 9, and 10. The MSB for the ADC is always output on DATA [9]. The unused LSB bits of DATA will be ‘0’. It is possible to have the ADC produce 10 bits of resolution, then apply a transform to the ADC data to cut it down to 8 bits. The DOD field of the ICTRL register selects a data transforms. The data transforms are 1) pass the data directly without transform, 2) rounding, 3) saturation.

4.1.6 Setting Viewing Window Coordinates

The FWCOL register specifies the first column in the viewing window. The LWCOL register specifies the last column in the viewing window. The FWROW register specifies the first row in the viewing window. The LWROW register specifies the last row in the viewing window.

The array is surrounded by boarder pixels that are addressable but not part of the image. There are 28 boarder pixels on the left, 4 on the right, and 8 on the top and bottom. Included in these are 4 pixels (top, bottom, left, and right) that have RGB Bayer filters. The following table shows the location of these boarder pixels.

Pixel Type	HDCS-2020 Column Addresses	HDCS-2020 Row Addresses	HDCS-1020 Column Addresses	HDCS-1020 Row Addresses
Dark Pixels	0-1		0-1	
Reference Pixels	2-17		2-17	
Dark Pixels	18-23	0-3	18-23	0-3
Border Bayer Pixels	24-27	4-7	24-27	4-7
Active Area Pixels	28-667	8-487	28-371	8-303
Border Bayer Pixels	668-671	488-491	372-375	304-307
Dark Pixels		492-495		308-311

Table 41. HDCS Sensor Viewing Window Coordinates

Note that the FWCOL, LWCOL, FWROW, LWROW registers do not include the 2 LSB. The FWCOL and FWROW registers add the 2 LSB '00' on to the binary number to specify. While LWCOL and LWROW add the 2 LSB '11' onto the number you specify. For example say you want to specify the normal 640 by 480 viewing window in HDCS 2020. Set FWCOL to '0000_0111', set FWROW to '0000_0010', set LWCOL to '1010_0110' and set LWROW to '0111_1001'. Internally, the sensor appends the 2 LSB to achieve: first column address equals '00_0001_1100' (28), last column address equals '10_1001_1011' (667), first row address equals '00_000_0100' (8), and last row address equals '1_1110_0111' (487).

4.1.7 Setting Column Timing

Column timing is determined by PSMP and ASTRT fields of the TCTRL register. Column timing is the number of cycles to sample and convert 2 pixels in HDCS-2020 and 1 pixel in the HDCS-1020. The number of cycles to sample and convert pixel data is PSMP + ASTRT + 3.

The faster the column timing the faster the data output, and the less motion artifacts in the picture.

4.1.8 Setting Exposure

There are 2 components of exposure (integration) time: 1) Row Exposure and 2) Sub-row Exposure. Total integration time equals row exposure time plus sub-row exposure time. The ROWEXPL and ROWEXH registers determine the row exposure time. The SROWEXP register determine the sub-row exposure time. See the Programming Reference chapter for more details.

Row exposure is the number of row processing periods to wait. Row exposure is based on the number of columns per row, and the column processing time. Sub-row exposure in an additional delay that is shorter than 1 row.

4.1.9 Selecting Mode of Operation

The MODE field of the CONFIG register determines the operating mode. There are two modes of operation: 1) Normal and 2) Shutter.

4.1.10 Selecting Mode of Scanning

The CSS (column sub-sample) and RSS (row sub-sample) fields of the CONFIG register determine scanning mode.

Note that when CSS is active the number of effective columns to use in calculating exposure is cut in half. Note that when RSS is active the number of effective rows used to calculate exposure is cut in half. For example if you want row exposure to be the time to process 8 rows, if RSS equals '1' then the number 16 should be put into the ROWEXPL register.

The HAVG bit of the ICTRL register enables horizontal averaging mode. This does not effect the exposure time, but is halves the number of pixels that are output per row. For each row every other pixel of the same color is averaged together and only one value is output. If CSS equals '1' then the averaging is performed after column sub-sampling.

CSS	HAVG	Pixel Columns Read	Pixel Columns Output
0	0	64	64
0	1	64	32
1	0	32	32
1	1	32	16

Table 42. Effect of CSS and HAVG for viewing window with 64 columns

4.1.11 Starting and Stopping Operation

Operation starts when the RUN bit of the CONTROL register is asserted. If the CFC (continuous frame capture) bit of the CONFIG register equals '0', operation automatically stops at the end of the first frame. If CFC equals '1' operation does not terminate until RUN is de-asserted. If the SFC (stop when frame complete) bit of the CONFIG register equals '0' when the RUN bit is de-asserted operation immediately halts, even if the current frame is only partially processed. If SFC equals '1' when run is de-asserted, then operation stops at the end of the current frame.

4.2 Sending Commands on the Serial Interface

4.2.1 Device Address Control

The DAD (device address disable) bit of the ICTRL register can disable the requirement to send the device address byte for the serial synchronous interface. After system reset, the HDCS Chip requires that the serial synchronous interface use the device address byte. The first register write must use the device address. If the serial interface is point to point, the device address is unnecessary overhead. If the first write sets DAD to '1', then the device address will not be required again. See the Serial Interface section of the Host System Interface chapter.

If the serial interface is configured as a UART slave, the interface must be point to point, and the device address is not used.

4.2.2 Polling the STATUS Register

It is not necessary to poll the register set if the status flags are used. However if the status ins are not used it may be necessary to poll the STATUS register to detect an event such as the end of a frame. The AAD (auto address disable) bit of the ICTRL register normally equals '0' so that the register address is incremented after each transfer of a multiple bye transfer. For the UART this means that a 2 byte read command must be transmitted for each read of the STATUS register. For the serial synchronous interface with the device address enabled a 2 bye write command to set up the register address followed by a one byte read command is required for each reading of the STATUS register. For the serial synchronous interface with the device address disabled a one byte read command must be transmitted for each reading of the STATUS register.

If AAD equals '1' the register address does not increment between transfers. In UART mode the register address can be set to the STATUS register and the transfer count of the read command can be set to 'N'. HDCS Sensor will transmit the value of the STATUS register 'N' times. In serial synchronous mode if a read command is issued to the STATUS register address, the STATUS register will be repeatedly transmitted until a NACK or STOP.

4.3 Serial Synchronous Setup Example

Assume that the HDCS Sensor needs to be configured to continuously transmit CIF (352 by 288) frames with no sub-sampling or averaging using a point to point serial synchronous interface. The desired column timing is 12 cycles per pixel pair. Every 12 cycles 2 data values must be sent, so each data will be driven 6 cycles with a 3 cycle DRDY. Assume integration time equal to 743.36 uSec. If part of a frame is transmitted, then the entire frame must be transmitted. The nROW, nFRAME, nCC status flags will be used as levels. Border pixels will not be used.

Integration time of 743.36 uSec equals 18584 at 25 MHz. There are 352 columns, so there are 176 column pairs to process. Each pixel pair is processed for 12 cycles, for a total read out time of 2,112 cycles per row. There are 202 cycles of overhead per row for a total of 2,314 cycles per row. Eight rows of integration takes 18,512 cycles, which leave 72 cycles of sub-row exposure. The exposure register should be set to 8 rows.

The sub-row exposure register is then set to 2,040 cycles (2,112 cycles of readout time - 72 cycles of extra exposure).

95.440 uSec equals Each row has 352 columns. Columns are processed in pairs. There are 176 (352/2) column pairs in a row. To add 6 columns of integration delay for the sub-row delay, the sub-row exposure register pair must be set to delay for 170 (176-6) column timing delays. The sub-row exposure register must be set to 2,040 (170 * 12) cycles. See the Programming Reference chapter for more details.

Transmitter: Bits	Command Type	Register Address	[Bit Positions] Notes
master: start condition			
master: 1010101_0 slave: 0 (ACK)	Command		[7:1] Device Address [0] Write
master: 0_000011_0 slave: 0 (ACK)	Register Address	PCTRL (3)	[7] Reserved [6:1] Register Address [0] Write
master: 111_11_01_1 slave: 0 (ACK)	Write Data	PCTRL (3)	[7:5] Status Flags Act as levels [4:3] Enable nCC (capture complete) [2:1] Enable nFRAME [0] Enable nROW
master: 00_00_00_00 slave: 0 (ACK)	Write Data	PDRV (4)	[7:6] Fastest switching speed for TxD [5:4] Fastest switching speed for Status Flags [3:2] Fastest switching speed for DRDY [1:0] Fastest switching speed for DATA
master: 0_10_0_00_1_0 slave: 0 (ACK)	Write Data	ICTRL (5)	[7] Do not use Horizontal Averaging [6:5] DSC: 2 cycle DATA valid before assert DRDY [4] No phase shift of DRDY/DATA [3:2] Normal 10 bit output without rounding etc. [1] Disable the device address for future serial commands. [0] Register Address automatically increments. (If this bit is set it must be last byte of the command)
master: 00_0_01_010 slave: 0 (ACK)	Write Data	ITMG (6)	[7:6] Reserved [5] Positive active DRDY [4:3] DHC: DATA still valid 1 cycle after DRDY de-asserts [2:0] RPC: DRDY high for 3 cycles. (note DATA driven for a total of 6 cycles DSC+RPC+DHC)
master: 00000000 slave: 0 (ACK)	Write Data	BFRAC (7)	Not using UART, so value does not matter.
master: 00000000 slave: 0 (ACK)	Write Data	BRATE (8)	Not using UART, so value does not matter.
master: 0000_1010 slave: 0 (ACK)	Write Data	ADCCTRL (9)	[7:4] Reserved [3:0] 10 bit ADC resolution
master: 00000011 slave: 0 (ACK)	Write Data	FWROW (10)	[7:0] The HDCS Sensor tacks ‘00’ on the LSB end of this number to get 00_0000_1100 (12). The first row in the viewing window is row 12. (this skips 8 dark pixels and 4 border pixels)
master: 00000011 slave: 0 (ACK)	Write Data	FWCOL (11)	[7:0] The HDCS Sensor tacks ‘00’ on the LSB end of this number to get 00_0000_1100 (12). The first column of the viewing window is 12. (this skips 8 dark pixels and 4 border pixels)
master: 01001010 slave: 0 (ACK)	Write Data	LWROW (12)	[7:0] The HDCS Sensor tacks ‘11’ on the LSB end of this number to get 01_0010_1011 (299). The last row of the viewing window is 299. A total of 288 rows for CIF.

Table 43. Serial Synchronous Setup Example

Transmitter: Bits	Command Type	Register Address	[Bit Positions] Notes
master: 10010010 slave: 0 (ACK)	Write Data	LWCOL (13)	[7:0] The HDCS Sensor tacks '11' on the LSB end of this number to get 10_0100_1011 (363). The last column of the viewing window is 363. A total of 352 columns for CIF.
master: 0_00_00110 slave: 0 (ACK)	Write Data	TCTRL (14)	[7] Reserved [6:5] ASTRT = 2 cycles [4:0] PSMP = 6 cycles This sets the column timing. Number of cycles to process a column pair = SCC = PSMP + ASTRT + 4 = 12 cycles.
master: 0_0000101 slave: 0 (ACK)	Write Data	ERECPGA (15)	PGA gain for green pixels in green/red rows. This number should come from prior measurements.
master: 0_0000111 slave: 0 (ACK)	Write Data	EROCPGA (16)	PGA gain for red pixels. This number should come from prior measurements.
master: 0_0001010 slave: 0 (ACK)	Write Data	ORECPGA (17)	PGA gain for blue pixels. This number should come from prior measurements.
master: 0_0000101 slave: 0 (ACK)	Write Data	OROCPGA (18)	PGA gain for green pixels in green/blue rows. This number should come from prior measurements.
master: 0000_1000 slave: 0 (ACK)	Write Data	ROWEXPL (19)	Low Bits of Row Exposure. Integration lasts 8 whole rows.
master: 0000_0000 slave: 0 (ACK)	Write Data	ROWEXPH (20)	High Bits of Row Exposure. Integration lasts 8 whole rows.
master: 0100_1000 slave: 0 (ACK)	Write Data	SROWEXPL (21)	Low Bits of Sub-row Exposure. Total of 2040 cycles as explained above.
master: 1111_1000 slave: 0 (ACK)	Write Data	SROWEXPH (22)	High Bits of Sub-row Exposure. Total of 2040 cycles as explained above.
master: 00_00_11_00 slave: 0 (ACK)	Write Data	CONFIG (23)	[7:6] Reserved [5:4] No row or column sub-sampling [3] Continuous frame capture [2] Stop when frame complete [1:0] Normal operation mode for integration/reset
master: 00000_1_00 slave: 0 (ACK)	Write Data	CONTROL (24)	[2] RUN bit. Integration begins when this pin is turned on.
master: stop condition			nCC asserts as an active low level.

Table 44. Serial Synchronous Setup Example

4.4 Example of Changing Modes

In this example the previous capture process must be changed capture a single CIF frame with the same exposure time but using column sub-sampling and row sub-sampling.

In order to change modes the initial capture process must first be stopped. Then the new register settings must be applied, and then the new capture process must be started.

Since column sub-sampling effectively changes the number of columns, and the row exposure is based on the number of columns, the exposure registers need to be updated to keep the same exposure time. The integration time was previously calculated to be 18584 cycles. With sub-sampling only 176 (352/2) columns will be sampled which means there are 88 (176/2) column pairs. Read out time for the columns will be 1056 cycles per row (88 * 12). Each row has 202 cycles of overhead for a total of 1258 cycles per row. Setting the row exposure register to 14 rows

will account for 17612 cycles, leaving 972 cycles that sub-row exposure register must account for. The sub-row exposure register should be set to 24 (1056 - 972).

Transmitter: Bits	Command Type	Register Address	[Bit Positions] Notes
master: start condition			Note: the previous example disabled the need for a device address
master: 0_011000_0 slave: 0 (ACK)	Register Address	CONTROL (24)	[7] Reserved [6:1] Register Address [0] Write
master: 00000_0_00 slave: 0 (ACK)	Write Data	CONTROL (24)	[3] Turn off the RUN bit. Since SFC = '1', the HDCS sensor will stop at the end of the current frame.
master: stop condition			Master waits for the end of the capture process when the nCC status flag (acting as a level) de-asserts. If the nCC status flag is not used, this can be determined by polling the STATUS register.
master: start condition			
master: 0_010011_0 slave: 0 (ACK)	Register Address	ROWEXPL (19)	[7] Reserved [6:1] Register Address [0] Write
master: 0000_1110 slave: 0 (ACK)	Write Data	ROWEXPL (19)	Low Bits of Row Exposure. Integration lasts 14 whole rows.
master: 0000_0000 slave: 0 (ACK)	Write Data	ROWEXPH (20)	High Bits of Row Exposure. Integration lasts 14 whole rows.
master: 0001_1000 slave: 0 (ACK)	Write Data	SROWEXPL (21)	Low Bits of Sub-row Exposure. Total of 24 cycles as explained above.
master: 0000_0000 slave: 0 (ACK)	Write Data	SROWEXPH (22)	High Bits of Sub-row Exposure. Total of 24 cycles as explained above.
master: 00_11_01_00 slave: 0 (ACK)	Write Data	CONFIG (23)	[7:6] Reserved [5:4] Row sub-sampling and Column sub-sampling both enabled. [3] Single frame capture [2] Stop when frame complete [1:0] Normal operation mode for integration/reset
master: 00000_1_00 slave: 0 (ACK)	Write Data	CONTROL (24)	[2] RUN bit. Integration begins when this pin is turned on. The above settings will run 1 frame and automatically stop. nCC will de-assert when done.
master: stop condition			nCC asserts as an active low level

Table 45. Serial Synchronous Change Example

4.5 UART Setup Example

Same setup as the serial synchronous setup example. Only difference is that an additional write is performed to increase the bit rate to send 1 bit every 16 cycles (640 nSec).

Transmitter: Bits	Command Type	Register Address	[Bit Positions] Notes
master: 0 (start) master: 0000111_0 master: 1 (stop)	Register Address	BFRAC (7)	[7:1] Device Address [0] Write
master: 0 (start) master: 0000_0001 master: 1 (stop)	Transfer Count		Transfer 2 bytes
master: 00000000 slave: 0 (ACK)	Write Data byte 1	BFRAC (7)	Change bit rate to 1 bit every 16 cycles.
master: 00000000 slave: 0 (ACK)	Write Data byte 2	BRATE (8)	Change bit rate to 1 bit every 16 cycles. New Bit Rate in effect after this write.
master: 0 (start) master: 0000011_0 master: 1 (stop)	Register Address	PCTRL (3)	[7:1] Device Address [0] Write
master: 0 (start) master: 0001_0101 master: 1 (stop)	Transfer Count		Transfer 22 bytes
master: 0 (start) master: 111_11_01_1 master: 1 (stop)	Write Data byte 1	PCTRL (3)	[7:5] Status Flags Act as levels [4:3] Enable nCC (capture complete) [2:1] Enable nFRAME [0] Enable nROW
master: 0 (start) master: 00_00_00_00 master: 1 (stop)	Write Data byte 2	PDRV (4)	[7:6] Fastest switching speed for TxD [5:4] Fastest switching speed for Status Flags [3:2] Fastest switching speed for DRDY [1:0] Fastest switching speed for DATA
master: 0 (start) master: 0_10_0_00_1_0 master: 1 (stop)	Write Data byte 3	ICTRL (5)	[7] Do not use Horizontal Averaging [6:5] DSC: 2 cycle DATA valid before assert DRDY [4] No phase shift of DRDY/DATA [3:2] Normal 10 bit output without rounding etc. [1] Disable the device address for future serial commands. [0] Register Address automatically increments. (If this bit is set it must be last byte of the command)
master: 0 (start) master: 00_0_01_010 master: 1 (stop)	Write Data byte 4	ITMG (6)	[7:6] Reserved [5] Positive active DRDY [4:3] DHC: DATA still valid 1 cycle after DRDY de-asserts [2:0] RPC: DRDY high for 3 cycles. (note DATA driven for a total of 6 cycles DSC+RPC+DHC)
master: 0 (start) master: 00000000 master 1 (stop)	Write Data byte 5	BFRAC (7)	same as current value.
master: 0 (start) master: 00000000 master: 1 (stop)	Write Data byte 6	BRATE (8)	same as current value not matter.

Table 46. UART Setup Example

Transmitter: Bits	Command Type	Register Address	[Bit Positions] Notes
master: 0 (start) master: 0000_1010 master: 1 (stop)	Write Data byte 7	ADCCTRL (9)	[7:4] Reserved [3:0] 10 bit ADC resolution
master: 0 (start) master: 00000011 master: 1 (stop)	Write Data byte 8	FWROW (10)	[7:0] The HDCS Sensor tacks '00' on the LSB end of this number to get 00_0000_1100 (12). The first row in the viewing window is row 12. (this skips 8 dark pixels and 4 border pixels)
master: 0 (start) master: 00000011 master 1 (stop)	Write Data byte 9	FWCOL (11)	[7:0] The HDCS Sensor tacks '00' on the LSB end of this number to get 00_0000_1100 (12). The first column of the viewing window is 12. (this skips 8 dark pixels and 4 border pixels)
master: 0 (start) master: 01001010 master: 1 (stop)	Write Data by 10	LWROW (12)	[7:0] The HDCS Sensor tacks '11' on the LSB end of this number to get 01_0010_1011 (200). The last row of the viewing window is 299. A total of 288 rows for CIF.
master: 0 (start) master: 10010010 master: 1 (stop)	Write Data byte 11	LWCOL (13)	[7:0] The HDCS Sensor tacks '11' on the LSB end of this number to get 10_0100_1011 (363). The last column of the viewing window is 363. A total of 352 columns for CIF.
master: 0 (start) master: 0_00_00110 master: 1 (stop)	Write Data byte 12	TCTRL (14)	[7] Reserved [6:5] ASTRT = 2 cycles [4:0] PSMP = 6 cycles This sets the column timing. Number of cycles to process a column pair = SCC = PSMP + ASTRT + 4 = 12 cycles.
master: 0 (start) master: 0_0000101 master: 1 (stop)	Write Data byte 13	ERECPGA (15)	PGA gain for green pixels in green/red rows. This number should come from prior measurements.
master: 0 (start) master: 0_0000111 master: 1 (stop)	Write Data byte 14	EROCPGA (16)	PGA gain for red pixels. This number should come from prior measurements.
master: 0 (start) master: 0_0001010 master: 1 (stop)	Write Data byte 15	ORECPGA (17)	PGA gain for blue pixels. This number should come from prior measurements.
master: 0 (start) master: 0_0000101 master: 1 (stop)	Write Data byte 16	OROCPGA (18)	PGA gain for green pixels in green/blue rows. This number should come from prior measurements.
master: 0 (start) master: 0000_1000 master: 1 (stop)	Write Data byte 17	ROWEXPL (19)	Low Bits of Row Exposure. Integration lasts 8 whole rows.
master: 0 (start) master: 0000_0000 master: 1 (stop) master: 0 (start) master: 0100_1000 master: 1 (stop)	Write Data byte 18 Write Data byte 19	ROWEXPH (20) SROWEXPL (21)	High Bits of Row Exposure. Integration lasts 8 whole rows. Low Bits of Sub-row Exposure. Total of 2040 cycles as explained above.

Table 47. UART Setup Example

Transmitter: Bits	Command Type	Register Address	[Bit Positions] Notes
master: 0 (start) master: 1111_1000 master: 1 (stop)	Write Data byte 20	SROWEXPH (22)	High Bits of Sub-row Exposure. Total of 2040 cycles as explained above.
master: 0 (start) master: 00_00_11_00 master: 1 (stop)	Write Data byte 21	CONFIG (23)	[7:6] Reserved [5:4] No row or column sub-sampling. [3] Continuous frame capture [2] Stop when frame complete [1:0] Normal operation mode for integration/reset.
master: 0 (start) master: 00000_1_00 master: 1 (stop)	Write Data byte 22	CONTROL (24)	[2] RUN bit. Integration begins when this pin is turned on.
			nCC asserts as an active low level.

Table 48. UART Setup Example

5. Host System Interface

5.1 Overview of Host System Interface

The host system interface is comprised of two data paths and status flags. The serial data path is used to read and write to the HDCS sensor register set. The parallel data path is used to output up to 10 bit sensor array data along with a valid signal. The status signals are nROW, nFRAME_nSYNC, and nIRQ_nCC. The status signals operate in multiple modes and are described below.

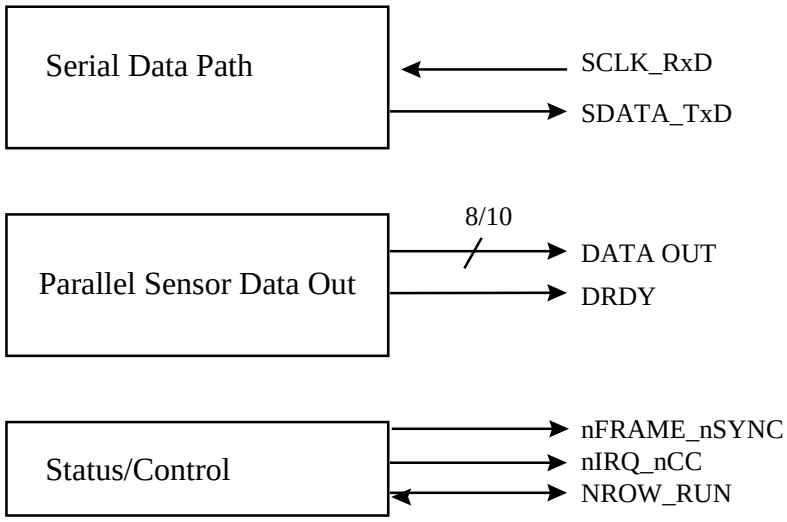

Figure 44. The HDCS Sensor Data Paths

5.2 The HDCS-2020 32 Pin Package Diagram

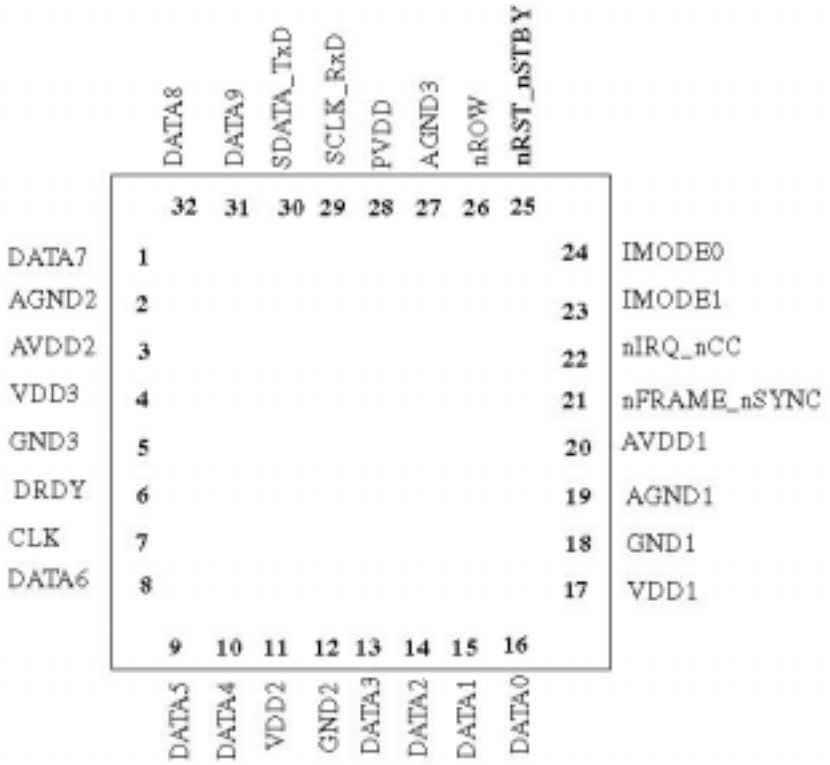

Figure 45. HDCS-2020 32 pin package diagram

5.2 The HDCS-1020 32 Pin Package Diagram

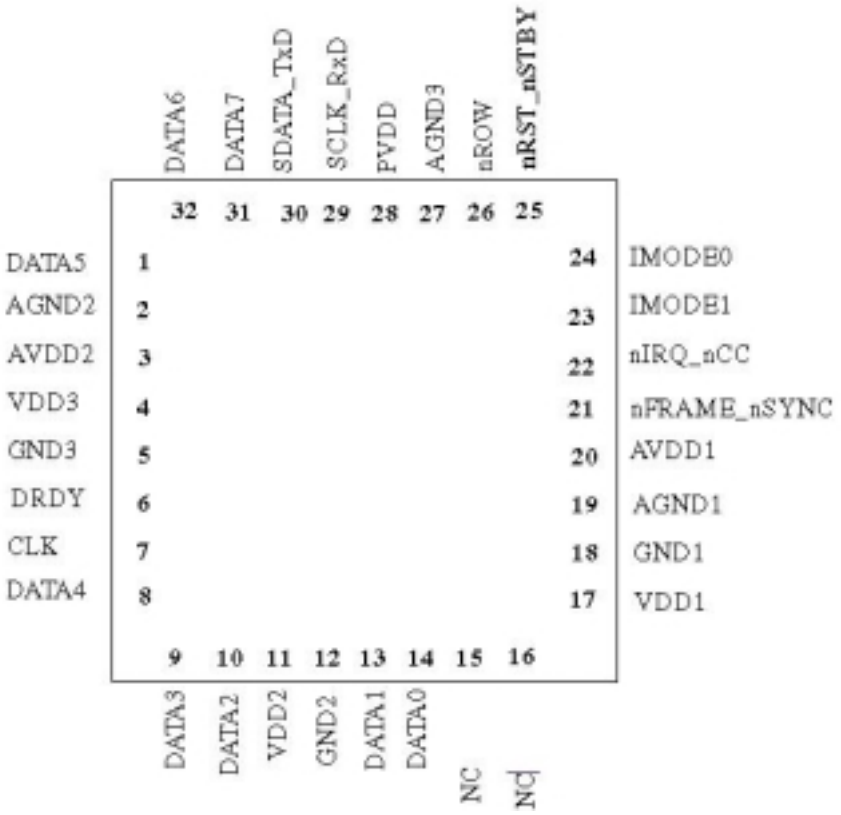

Figure 46. HDCS-1020 32 pin package diagram

5.3 HDCS-2020 Pin Description

Pkg Pins	Signal Name	Type	Value after System Reset
1	IMODE1	Input	
1	IMODE0	Input	
1	CLK	Input	
1	nRST_nSTBY	Input	
10	Data 9, Data 8, Data 7, Data 6, Data 5, Data 4, Data 3, Data 2, Data 1, Data 0	Output	"00_0000_0000"
1	DRDY	Output	"0"
1	SDATA_TxD	Input/output open drain	“1”
1	SCLK_RxD	Intput	
1	nFRAME_nSYNC	Output	"1"
1	nROW	Output	"1"
1	nIRQ_nCC	Output	"1"
3	VDD	VDD	Digital Power
3	GND	GND	Digital Ground
1	PVDD	PVDD	Array Power
2	AVDD	AVDD	Analog Power
3	AGND	AGND	Analog and Substrate Ground
0	NC	NC	No Connect
32			

Table 49. External Pin List for HDCS-2020

5.3 HDCS-1020 Pin Description

Pkg Pins	Signal Name	Type	Value after System Reset
1	IMODE1	Input	
1	IMODE0	Input	
1	CLK	Input	
1	nRST_nSTBY	Input	
8	Data 7, Data 6, Data 5, Data 4, Data 3, Data 2, Data 1, Data 0	Output	0000_0000"
1	DRDY	Output	"0"
1	SDATA_TxD	Input/output open drain	“1”
1	SCLK_RxD	Intput	
1	nFRAME_nSYNC	Output	"1"
1	nROW	Output	"1"
1	nIRQ_nCC	Output	"1"
3	VDD	VDD	Digital Power
3	GND	GND	Digital Ground
1	PVDD	PVDD	Array Power
2	AVDD	AVDD	Analog Power
3	AGND	AGND	Analog and Substrate Ground
2	NC	NC	No Connect
32			

Table 50. External Pin List for HDCS-1020

5.3.1 Pad Descriptions

5.3.1.1 Note for all PADS

When asserted low nRST_nSTBY performs a full system reset with the clock gating to all registers except the clock synchronization registers. When IMODE[1:0]=”11”, SCLK_RxD is used to tristate the output pins.

5.3.1.2 DRDY

- DESCRIPTION:

Data valid for parallel digitized pixel data out.

The timing of DRDY is controlled by the DSC field of the ICTRL register and by the RPC and DHC fields of the ITMG register

ICTRL/ITMG Field	# Bits	Meaning
ICTRL [DSC]	2	Number of cycles (0-3) DATA is valid before DRDY is asserted. "00" means 0 cycles, "01" means 1 cycles…
IFTMG [RPC]	3	Number of cycles (1-8) that DRDY is asserted. DATA is also driven during this time. "000" means 1 cycle, "001" means 2 cycles…
ICTRL [DHC]	2	Number of cycles (0-3) DATA is driven after DRDY is de-asserted. "00" means 0 cycles, "01" means 1 cycles…

Table 51. DRDY and DATA timing control

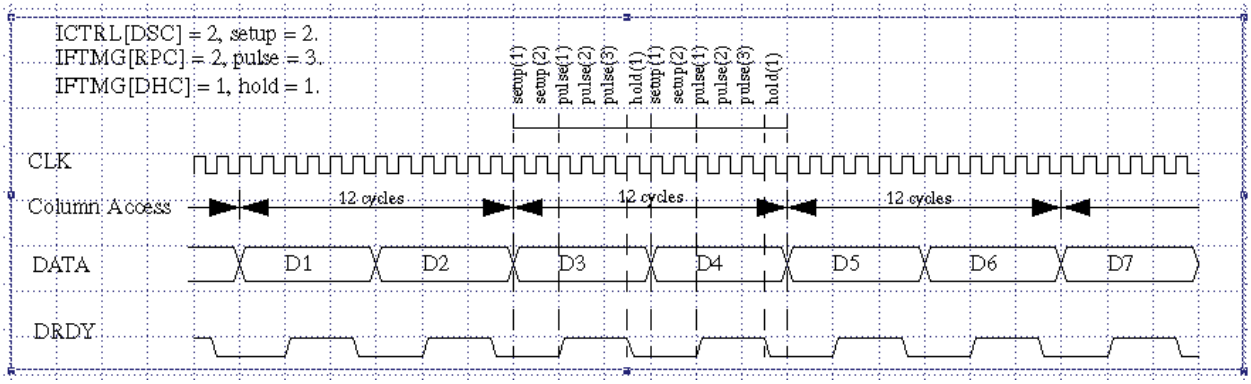

Figure 47. HDCS-2020 DRDY timing for 12 cycle column acces, DSC=2, RPC=2, DHC=1

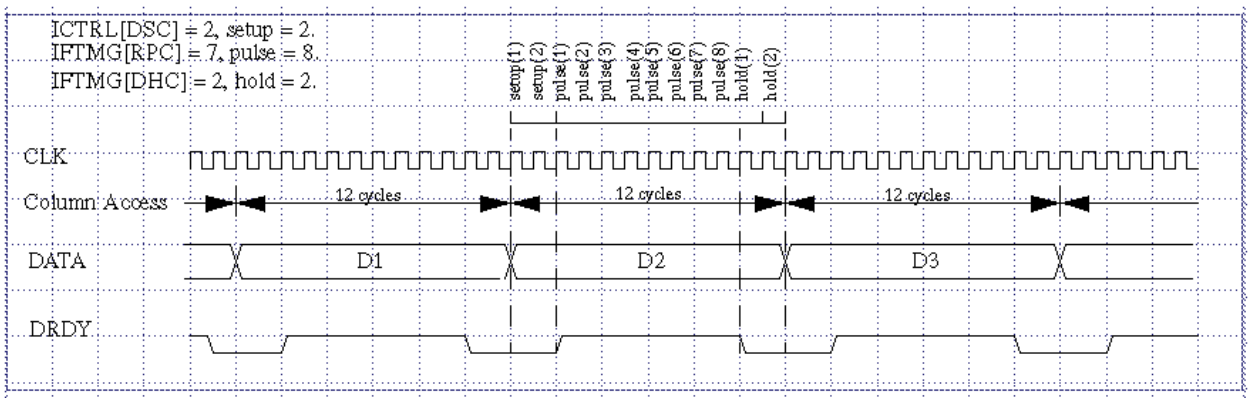

Figure 48. HDCS-1020 DRDY timing for 12 cycle column access, DSC=2, RPC=7, DHC=2

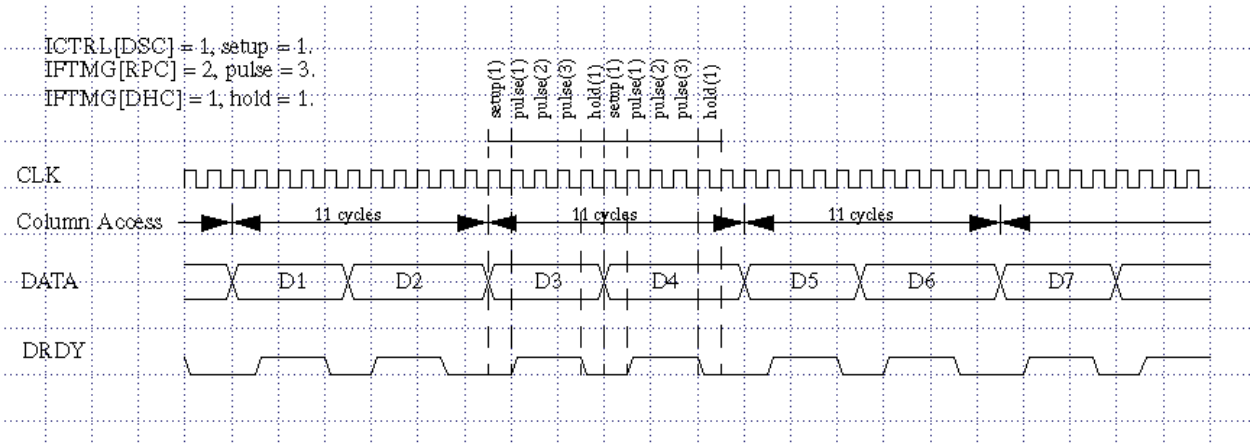

Figure 49. HDCS-2020 DRDY timing for 11 cycle column access, DSC=1, RPC=2, DHC=1

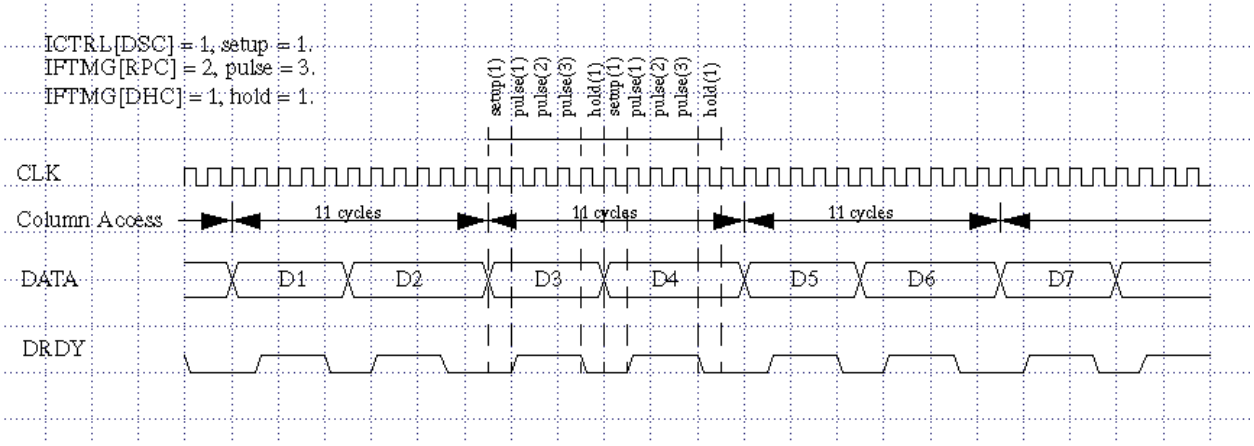

Figure 50. HDCS-1020 DRDY timing for 9 cycle column access, DSC=1, RPC=6, DHC=1

The DDO field of the ICTRL register controls the point in the cycle DRDY, nROW and nFRAME_nSYNC are driven. If DDO = ‘0’ DRDY, nROW and nFRAME_nSYNC begin driving when CLK makes a rising transition. If DDO == ‘1’, nROW and nFRAME_nSYNC begin driving when CLK makes a falling transition.

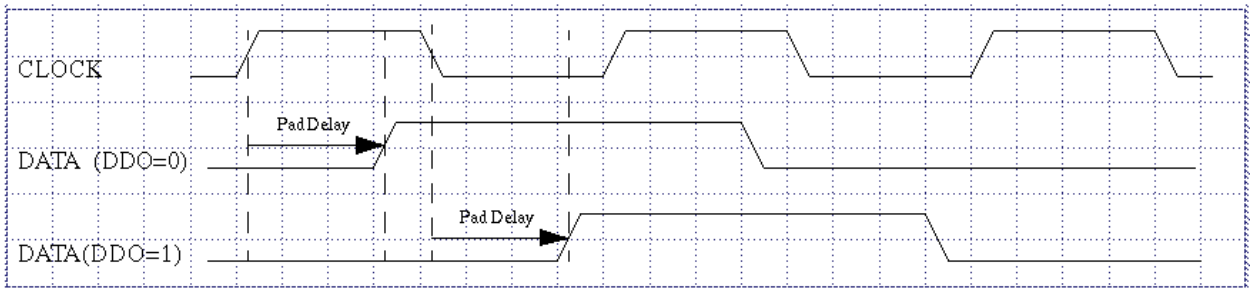

Figure 51. DATA timing altered by DDO bit of ICTRL register

The DRD field of the ITMG register controls the point in the cycle DRDY is driven. If DRD = '0' DRDY begins driving when CLK makes a rising transition. If DRD == '1' DRDY begin driving when CLK makes a falling transition.

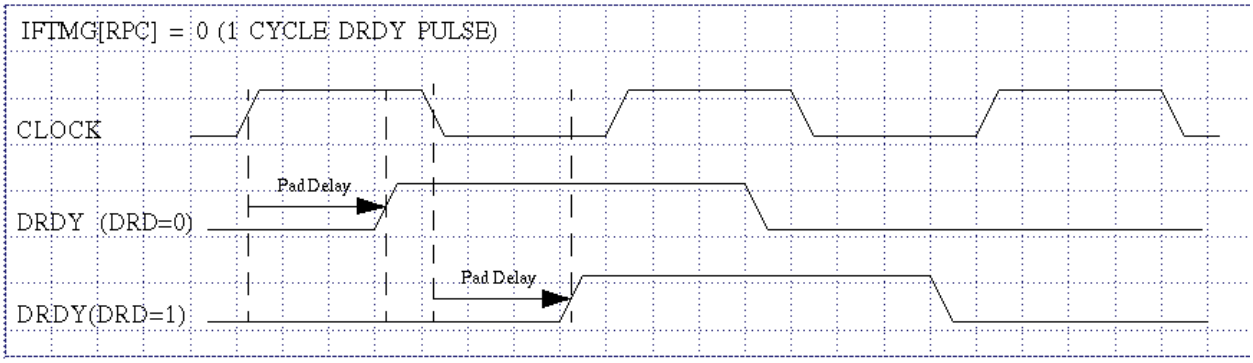

Figure 52. DRDY timing altered by DRD bit of ITMG register

- CONNECTION INFORMATION:
- PAD CONTROL:

  DRDY is controlled by the DOD(HDCS-2020 only), DDO, DSC, DHC and HAVG fields of the ICTRL register, the RPC and DPS fields of the ITMG register, and DRD of the ICTRL2 register. The RDYDRV field of the PDRV register controls the switching speed of DRDY.

5.3.1.3 DATA 9, DATA 8, DATA 7, … DATA 0

- DESCRIPTION:

  Parallel digitized pixel data out. DATA9, DATA8 not present in HDCS-1020

  The timing of DATA is defined in the DRDY pin description.

  The DOD field of the ICTRL register is only used in the HDCS-1020. It defines 4 modes of modifying 10 bit output. If the ADC's are programmed to output less than 10 bits, the MSB of the output is aligned to DATA[9].

DOD value	mode	DATA[9:0]
00	normal	DATA[9:0] = ADC_DATA[9:0];

01	rounding	if (ADC_DATA[9:2] = '1111_1111')
		ADC_rounded[9:0] = '11_1111_1111'
		else
		ADC_rounded[9:0] = ADC_DATA + '00_0000_0010'
		DATA[9:2] = ADC_rounded[9:2];
		DATA[1:0] = '00'

10	saturation	if {(ADC_DATA[9] = 1) or (ADC_DATA[8] = 1)}
		DATA[9:2] = '1111_1111'; //saturation
		else
		DATA[9:2] = ADC_DATA[7:0];
		DATA[1:0] = '00'

11	truncated saturation	if (ADC_DATA[9] = 1) DATA[9:2] = '1111_1111'; //saturation
		else
		DATA[9:2] = ADC_DATA[8:1];
		DATA[1:0] = '00'

Table 52. DOD bits of IFCTRL controlling DATA out

Number of ADC bits	DATA9 (MSB) - DATA0 (LSB)
10	ADC_DATA[9:0]
9	ADC_DATA[9:1], '0'
8	ADC_DATA[9:2], '00'

Table 53. Data Alignment of ADC output for DOD = '00'

The sequencing of data output from the sensor is influenced by the HAVG bit of the ICTRL register and by the CSS bit of the CONFIG register.

Assume Sampling Window from column 12 to column 19, nROW in level mode.

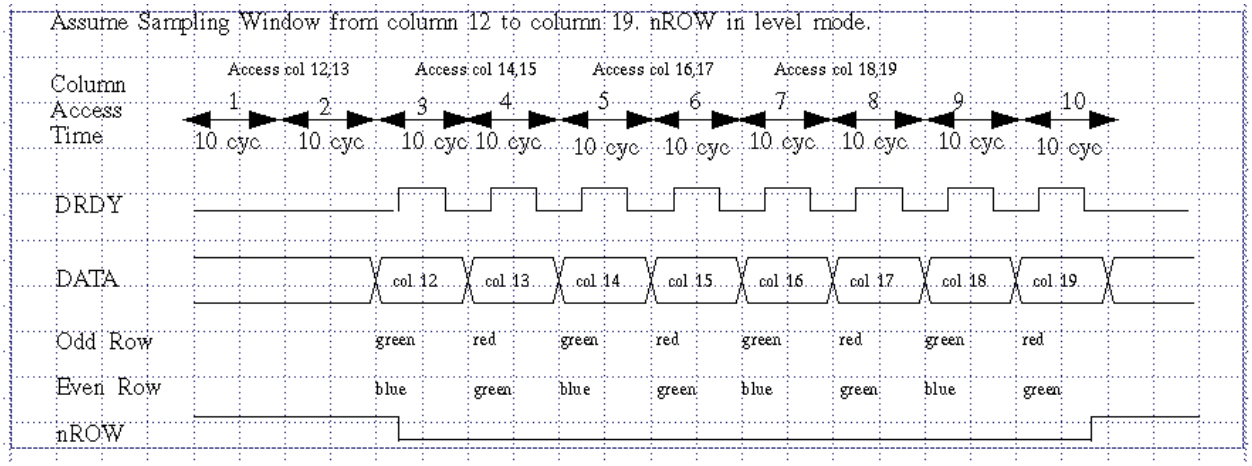

Figure 53. HDCS-1020(and 2020 single channel) DATA Sequencing: CONFIG[CSS] = '0', ICTRL[HAVG] = '0'

Assume Sampling Window from column 12 to column 19, nROW in level mode.

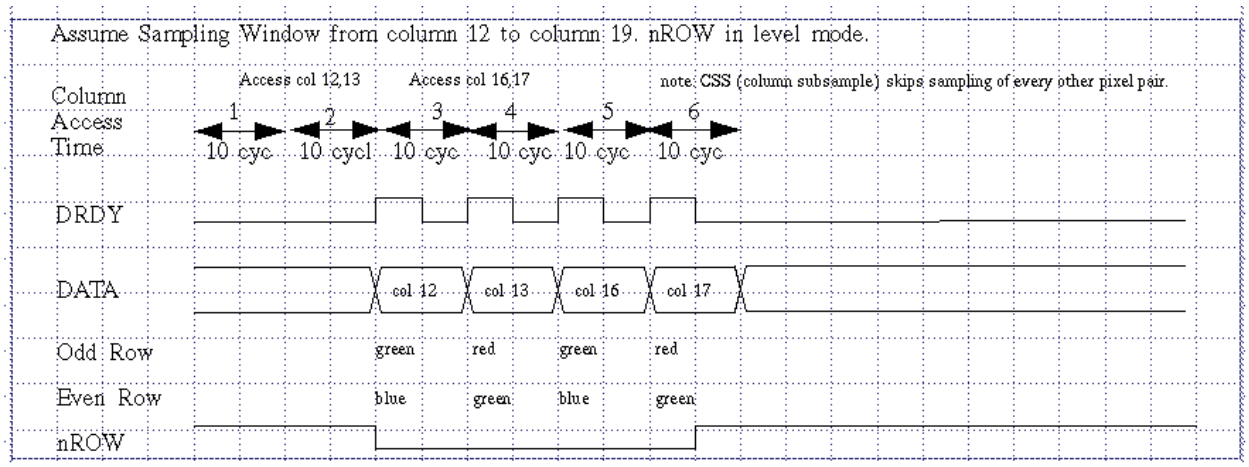

Figure 54. HDCS-1020(and 2020 single channel) DATA sequencing: CONFIG[CSS] = '1' ICTRL[HAVG] ; '0'

Assume Sampling Window from column 12 to column 19, nROW in level mode.

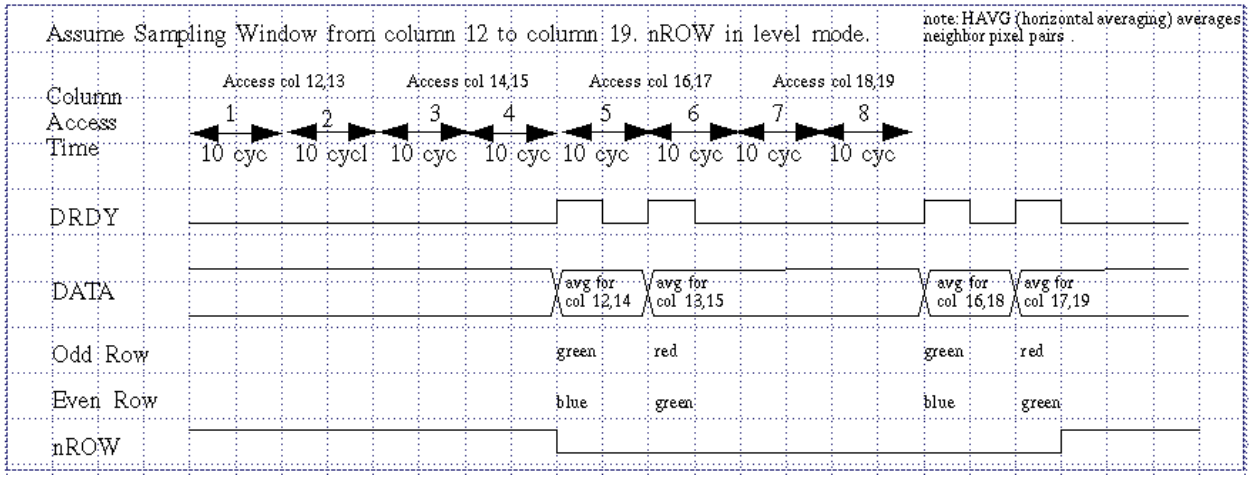

Figure 55. HDCS-1020(and 2020 single channel) DATA Sequencing: CONFIG[CSS] = '0', ICTRL[HAVG] = '1'

Assume Sampling Window from column 12 to column 19, nROW in level mode.

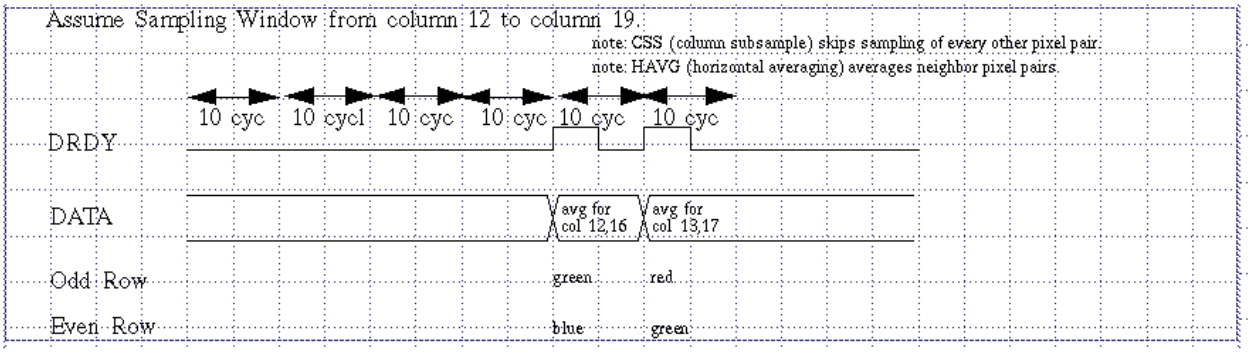

Figure 56. HDCS-1020(and 2020 single channel) DATA Sequencing: CONFIG[CSS] = '1', ICTRL[HAVG] = '1'

Assume Sampling Window from column 12 to column 19, nROW in level mode.

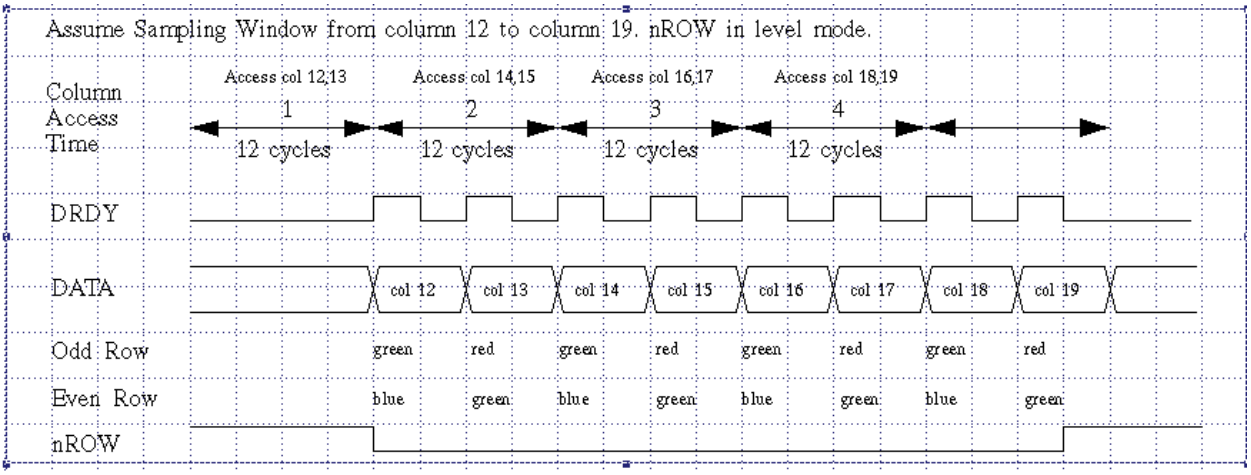

Figure 57. HDCS-2020 DATA Sequencing: CONFIG[CSS] = ‘0’, ICTRL[HAVG] = ‘0’

Assume Sampling Window from column 12 to column 19, nROW in level mode.

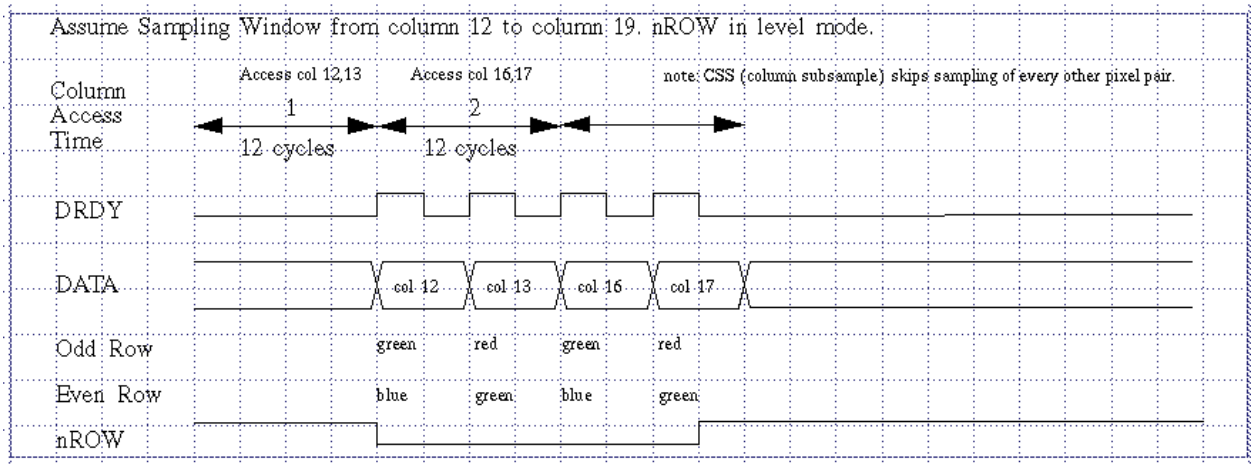

Figure 58. HDCS-2020DATA Sequencing: CONFIG[CSS] = ‘1’, ICTRL[HAVG] = ‘0’

Assume Sampling Window from column 12 to column 19, nROW in level mode.

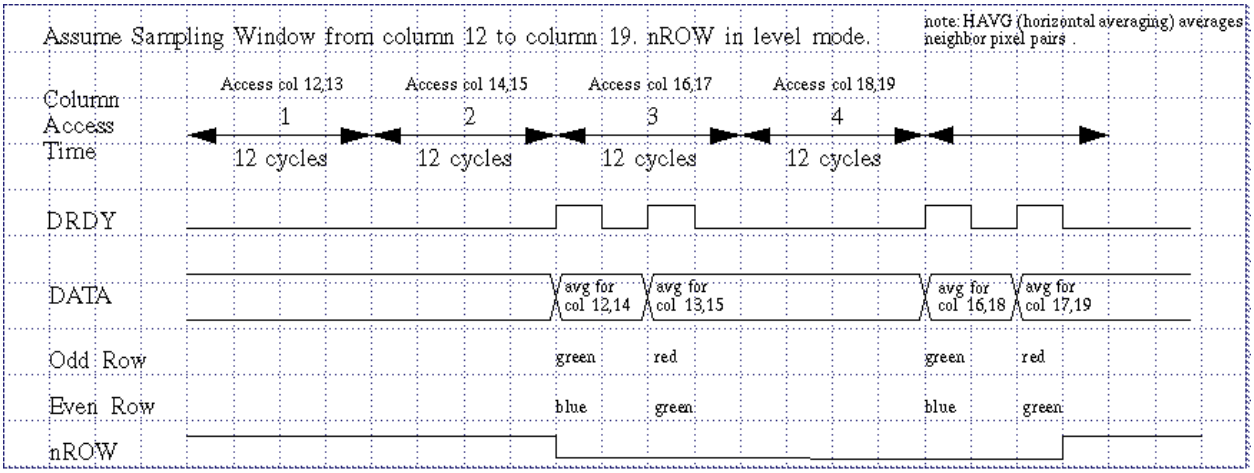

Figure 59. HDCS-2020 DATA Sequencing: CONFIG[CSS] = '0', ICTRL[HAVG] = '1'

Assume Sampling Window from column 12 to column 19, nROW in level mode.

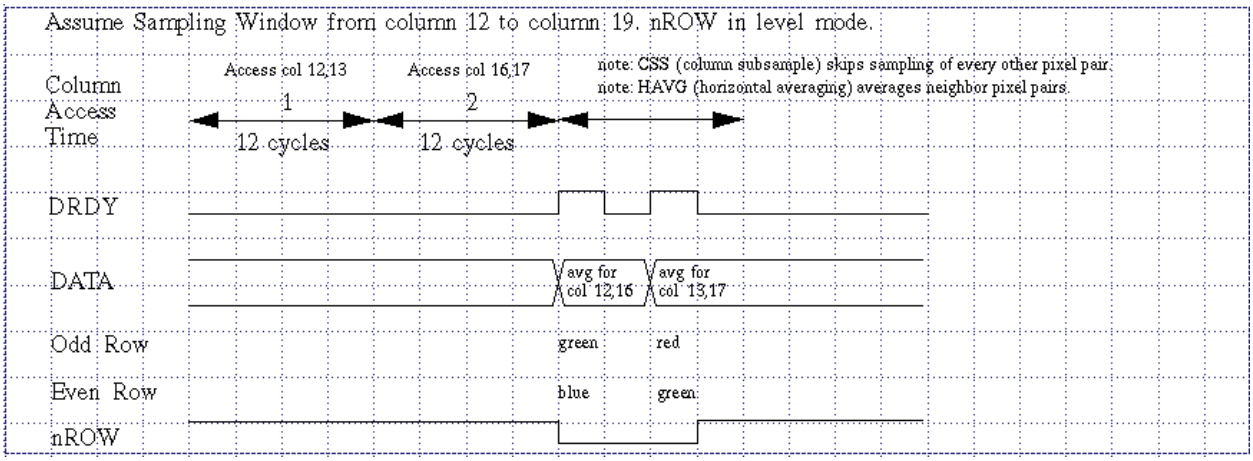

Figure 60. HDCS-2020DATA Sequencing: CONFIG[CSS] = '1', ICTRL[HAVG] = '1'

- CONNECTION INFORMATION:
- PAD CONTROL:

  DATA[9:0] is controlled by the DOD, DDO, DSC, and HAVG fields of the ICTRL fields of the ICTRL register, and by the RPC, DHC, and DPS fields of the ITMG register. The DATDRV field of the PDRV register controls the switching speed of DATA.

5.3.1.4 IMODE

- DESCRIPTION:
  The IMODE input defines the interface mode.

IMODE/TCLK	Interface Mode Description
IMODE == '00'	Synchronous Serial Slave Mode. • SCLK_RxD operates as the serial transfer clock. • SDATA_TxD] operates as the serial data.
IMODE == '10'	Half Duplex UART Slave Mode. • SCLK_RxD is the serial input data. • SDATA_TxD is the serial output data

Table 54. Interface Modes

5.3.1.5 SCLK_RxD

- DESCRIPTION:
  If IMODE[1]=='0', SCLK_RxD input is the transfer clock for synchronous serial mode.
  If IMODE[1]=='1', SCLK_RxD is the serial data input for the UART protocol.

5.3.1.6 SDATA_TxD

- DESCRIPTION:
  SDATA_TxD is the serial output data.
  If IMODE = '1' TxD follows the UART protocol, if IMODE = '0' TxD follows the Synchronous Serial protocol.

5.3.1.8 nFRAME_nSYNC

- DESCRIPTION:

FSE	FSS	LVF	DSYNC	FSM	FRMT	Mode: Notes
'0'	'x'	'x'	'0'	'x'	'0'	nFRAME_nSYNC is disabled. Drives a constant '1'.
'1'	'1'	'0'	'0'	'x'	'0'	nSYNC Pulse Mode. Assert 4 cycle active low pulse at the start of integration.
'1'	'1'	'1'	'x'	'x'	'0'	nSYNC Level Mode. Assert low at start of integration. De-assert on first DRDY leading edge.
'1'	'0'	'0'	'0'	'x'	'0'	nFRAME Pulse Mode. Assert low for 4 cycles after the trailing edge of last DRDY of frame. If CONFIG[SFC] (stop when frame complete) equals '0', if CONTROL[RUN] is de-asserted after at least one DRDY was asserted for the current frame, then nFRAME is asserted low for 4 cycles.
'1'	'0'	'1'	'0'	'x'	'0'	nFRAME Level Mode. Assert low on leading edge of first DRDY of the frame. De-assert on trailing edge of last DRDY of the frame. If CONFIG[SFC] (stop when frame complete) equals '0, nFRAME is de-asserted when CONTROL[RUN] is de-asserted.
'1'	'1'	'1'	'1'	'x'	'0'	nSYNC DSYNC Level Mode. Assert low at start of integration. De-assert on start of first DATA transfer.
'1'	'0'	'0'	'1'	'0'	'0'	nFRAME Start-of-Frame DSYNC Pulse Mode. Assert low when the first DATA of the frame is transferred. If CONFIG[SFC] (stop when frame complete) equals '0', if CONTROL[RUN] is de-asserted, no nFRAME or DRDY will be asserted.
'1'	'0'	'0'	'1'	'1'	'0'	nFRAME End-of-Frame DSYNC Pulse Mode. Assert low when the last DATA of the frame is transferred. If CONFIG[SFC] (stop when frame complete) equals '0', if CONTROL[RUN] is de-asserted after at least one DRDY was asserted for the current row, nFRAME asserts low for the duration of one DATA transfer. DRDY will be asserted as well.
'1'	'0'	'1'	'1'	'x'	'0'	nFRAME DSYNC Level Mode. Assert low when first data for a frame is transferred. De-assert after last data for a frame is transferred. If CONFIG[SFC] (stop when frame complete) equals '0, nFRAME is de-asserted when CONTROL[RUN] is de-asserted. DRDY will pulse after nFRAME has been deasserted as per during normal DATA transfer.
'x'	'x'	'x'	'x'	'x'	'1'	nFRAME is tristated.

Table 55. nFRAME_nSYNC Status Flag Control

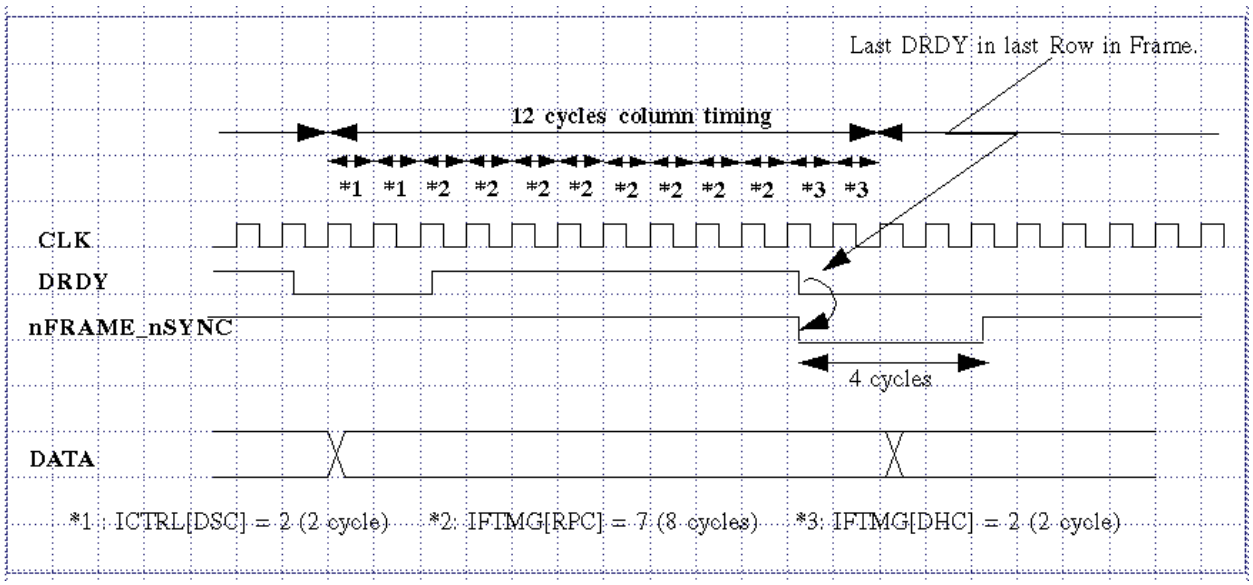

Figure 61. HDCS-1020(2020 single channel mode) nFRAME_nSYNC Timing in nFRAME Pulse Mode

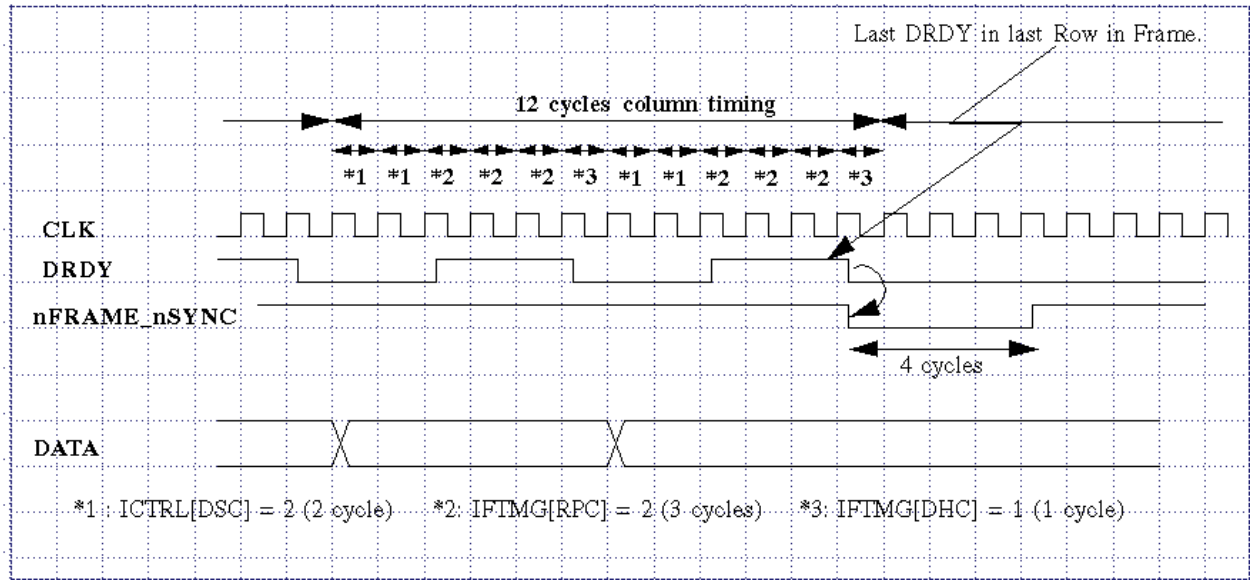

Figure 62. HDCS-2020 nFRAME_nSYNC Timing in nFRAME Pulse Mode

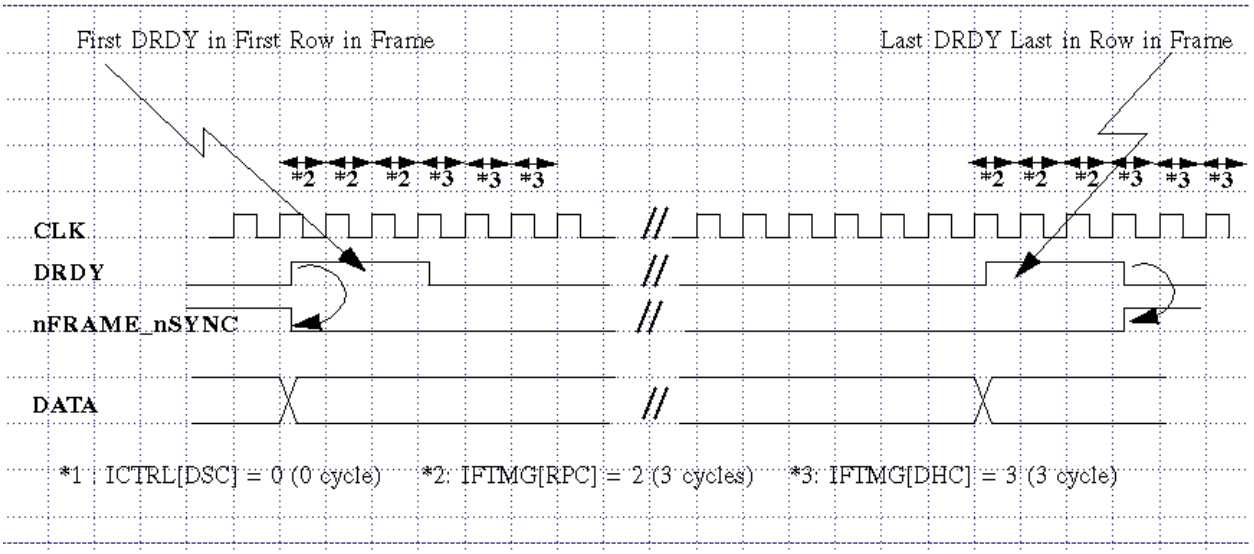

Figure 63. HDCS-1020(2020 in single channel mode) nFRAME_nSYNC Timing in nFRAME Level Mode

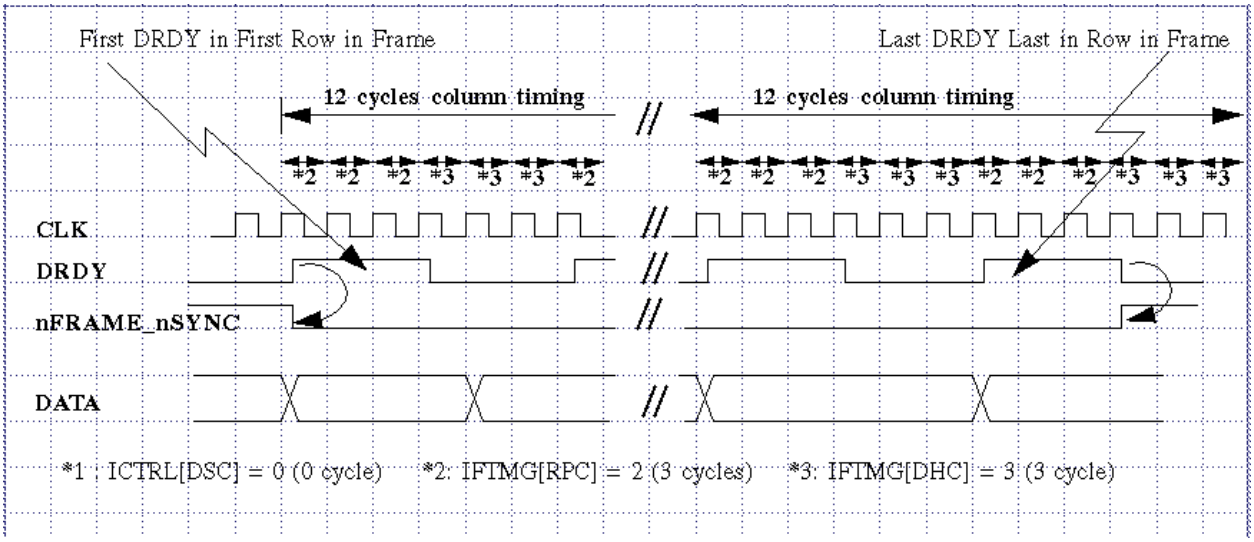

Figure 64. HDCS-2020 nFRAME_nSYNC Timing in nFRAME Level Mode

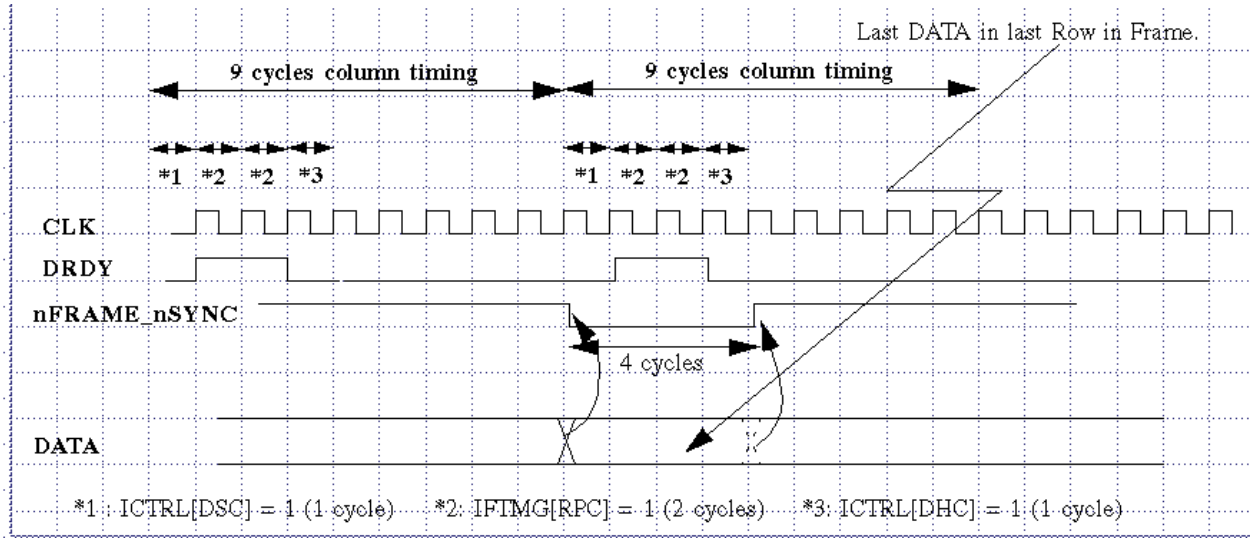

Figure 65. HDCS-1020(2020 in single channel mode) nFRAME_nSYNC Timing in end-of-frame DSYNC pulse Mode

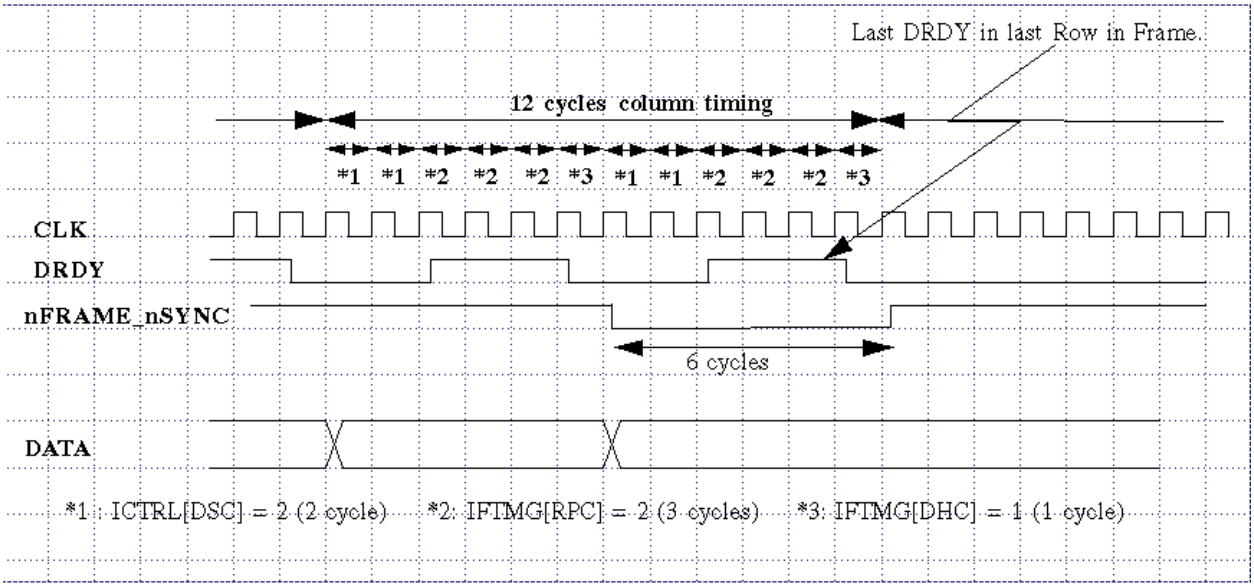

Figure 66. HDCS-2020 nFRAME_nSYNC Timing in end-of-frame DSYNC pulse Mode

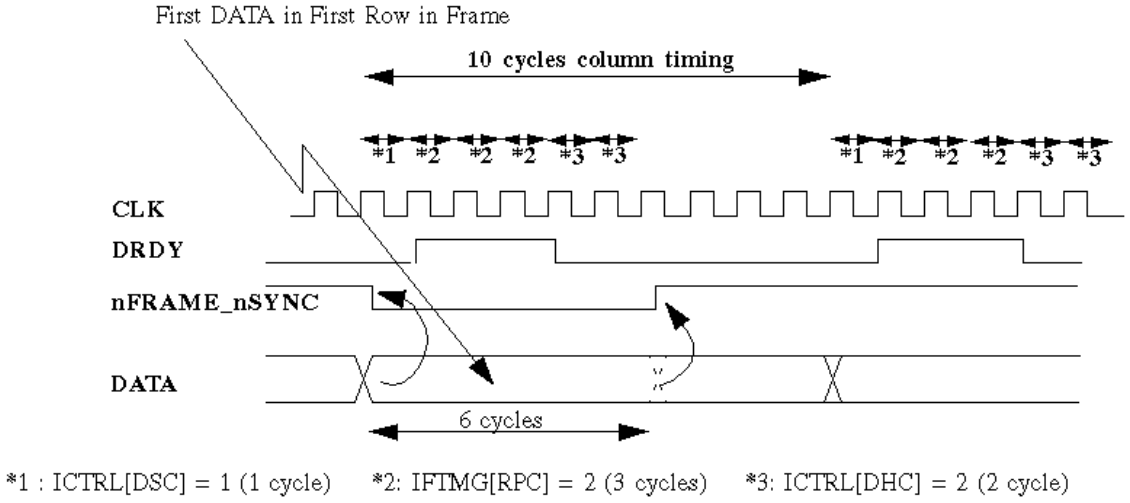

Figure 67. HDCS-1020(2020 in single channel mode) nFRAME_nSYNC Timing in start-of-frame DSYNC pulse Mode

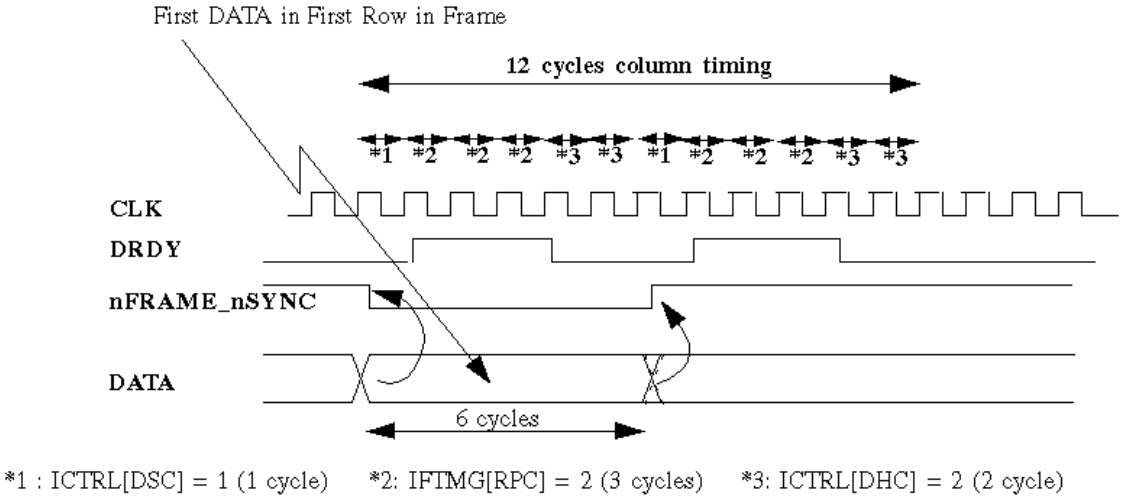

Figure 68. HDCS-2020 nFRAME_nSYNC Timing in start-of-frame DSYNC pulse Mode

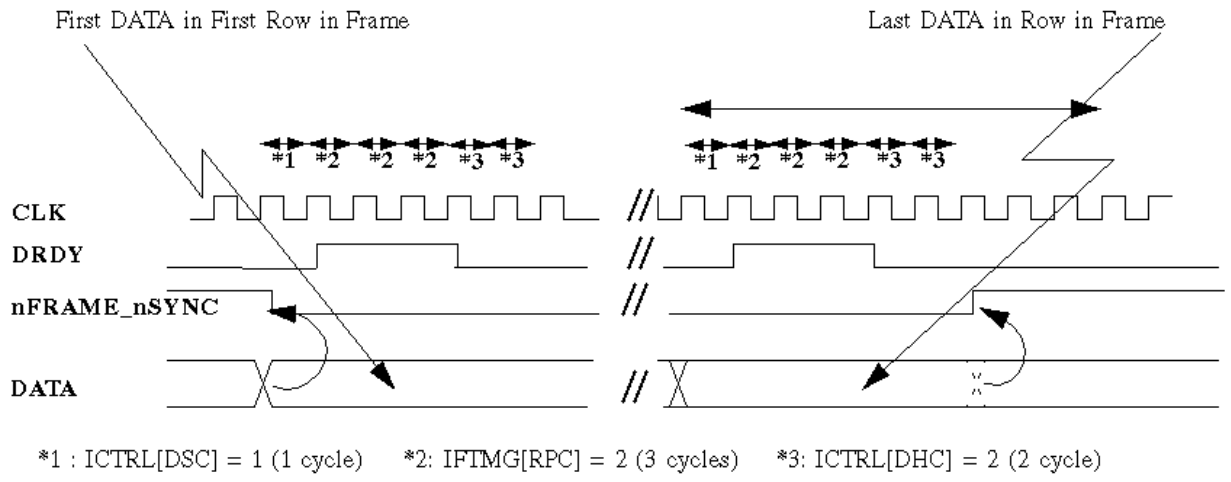

Figure 69. nFRAME_nSYNC Timing in DSYNC level Mode

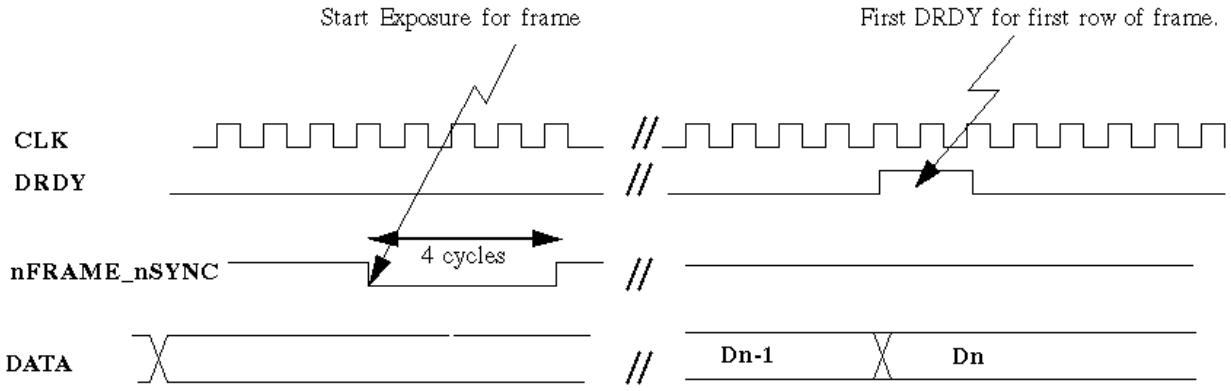

Figure 70. HDCS-2020 nFRAME_nSYNC Timing in shutter sync pulse Mode

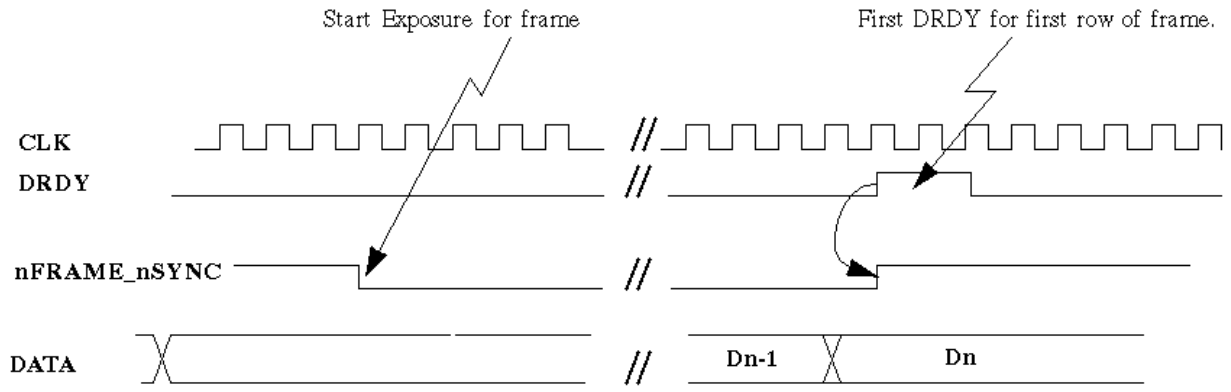

Figure 71. nFRAME_nSYNC Timing in Shutter Sync Level Mode

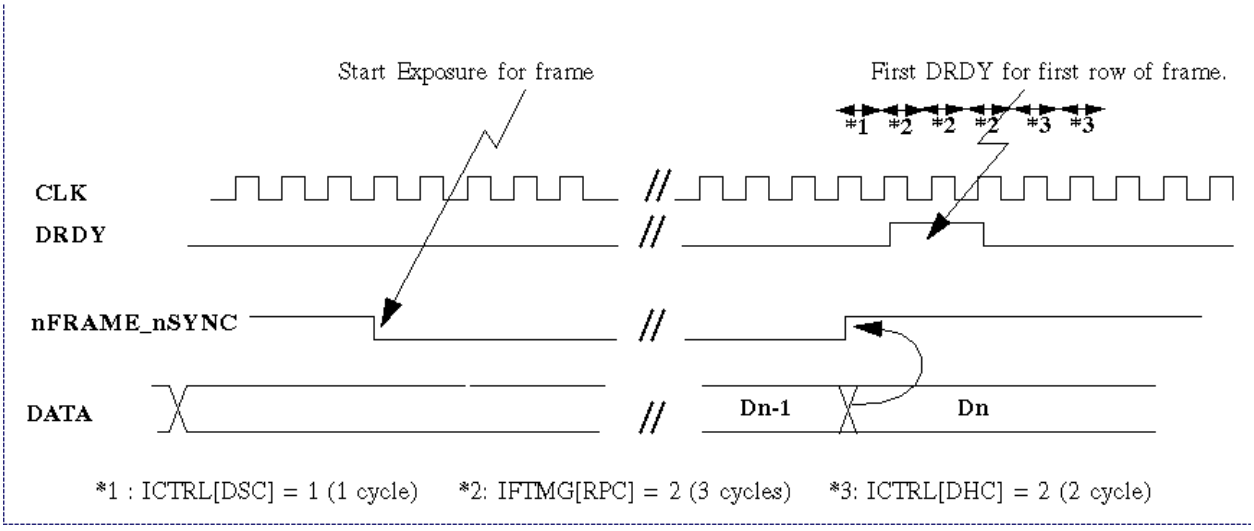

Figure 72. nFRAME_nSYNC Timing in Shutter DSYNC Level Mode

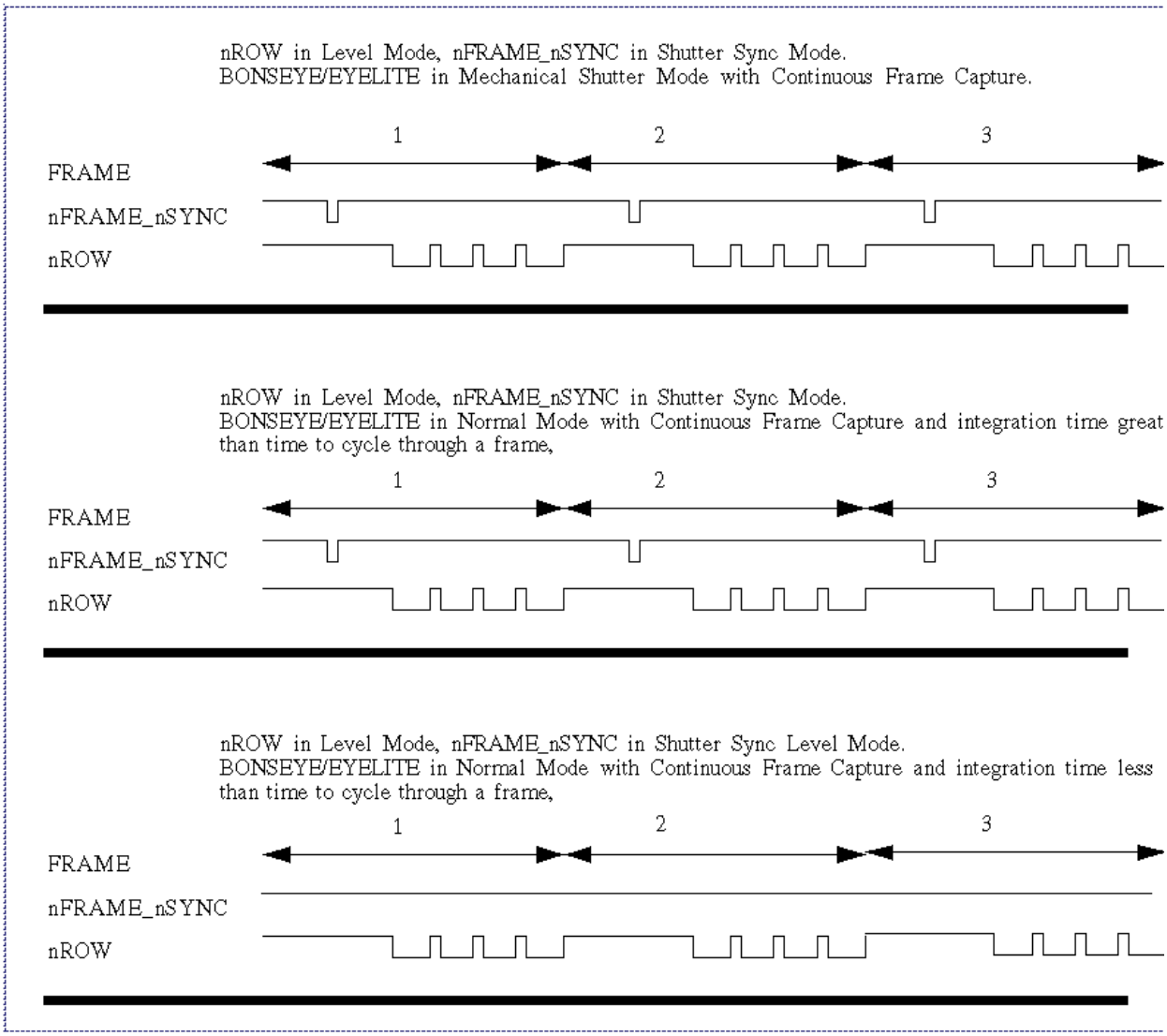

Figure 73. nFRAME_nSYNC in different operation modes

- CONNECTION INFORMATION:
  If nFRAME_nSYNC is unused, then do not connect it.

- PAD CONTROL:
  The STATDRV field of the PDRV register controls the switching speed.

5.3.1.9 nROW

- DESCRIPTION:

RCE	LVR	DSYNC	RSM	ROWT	Mode: Notes
'0'	'x'	'0'	'x'	'0'	nROW Disabled. Drives a constant '1'.
'1'	'0'	'0'	'x'	'0'	nROW pulse mode. Assert low for 4 cycles after trailing edge of last DRDY of sensor row is transferred. If CONFIG[SFC] (stop when frame complete) equals '0', if CONTROL[RUN] is de-asserted after at least one DRDY was asserted for the current row, then nROW is asserted low for 4 cycles.
'1'	'1'	'0'	'x'	'0'	nROW level mode. Assert low on leading edge of first DRDY of row. De-assert on trailing edge of last DRDY of row. If CONFIG[SFC] (stop when frame complete) equals '0, nROW is de-asserted when CONTROL[RUN] is de-asserted.
'1'	'0'	'1'	'0'	'0'	nROW Start-of-Row DSYNC pulse mode. Assert low when first DATA of the row is transferred. If CONFIG[SFC] (stop when frame complete) equals '0', if CONTROL[RUN] is de-asserted, no nROW or DRDY will be asserted.
'1'	'0'	'1'	'1'	'0'	nROW End-or-Row DSYNC pulse mode. Assert low when last DATA of the row is transferred. If CONFIG[SFC] (stop when frame complete) equals '0', if CONTROL[RUN] is de-asserted after at least one DRDY was asserted for the current row, nROW asserts low for the duration of one DATA transfer. DRDY will be asserted as well.
'1'	'1'	'1'	'x'	'0'	nROW DSYNC level mode. Assert low when first DATA of row is transferred. De-assert after last DATA of row is transferred. If CONFIG[SFC] (stop when frame complete) equals '0, nROW is de-asserted when CONTROL[RUN] is de-asserted. DRDY will pulse after nROW has been deasserted as per during normal DATA transfer.
'x'	'x'	'x'	'x'	'1'	nROW is tristated.

Table 56. nROW Status Flag Control

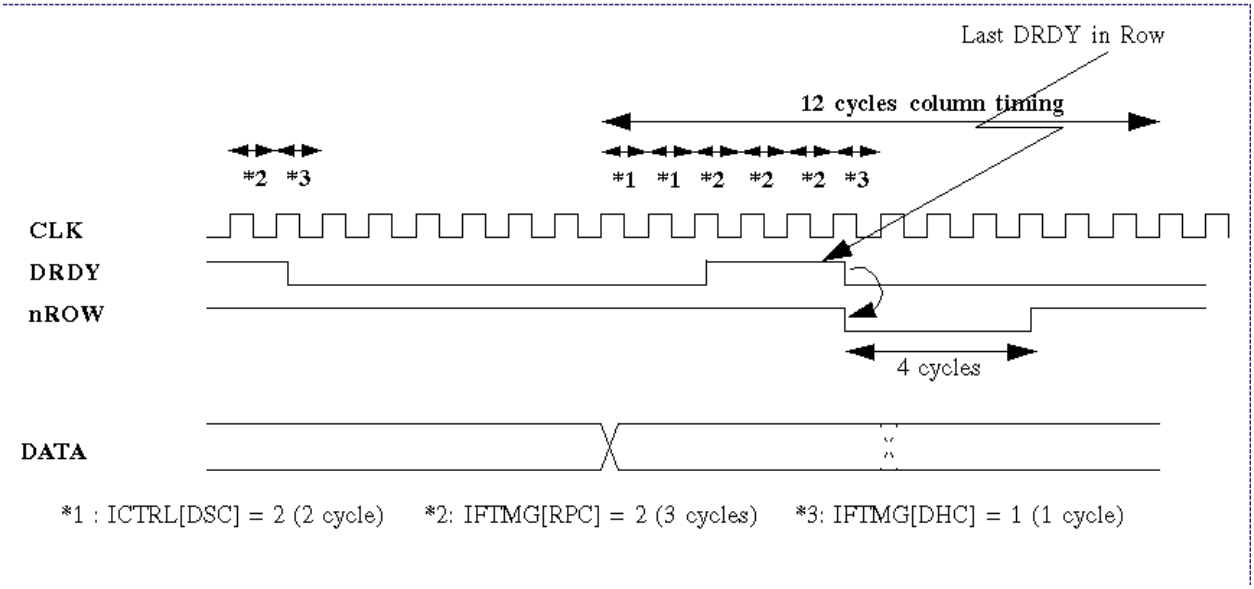

Figure 74. HDCS-1020(2020 in single channel mode) nROW Timing in Pulse Mode

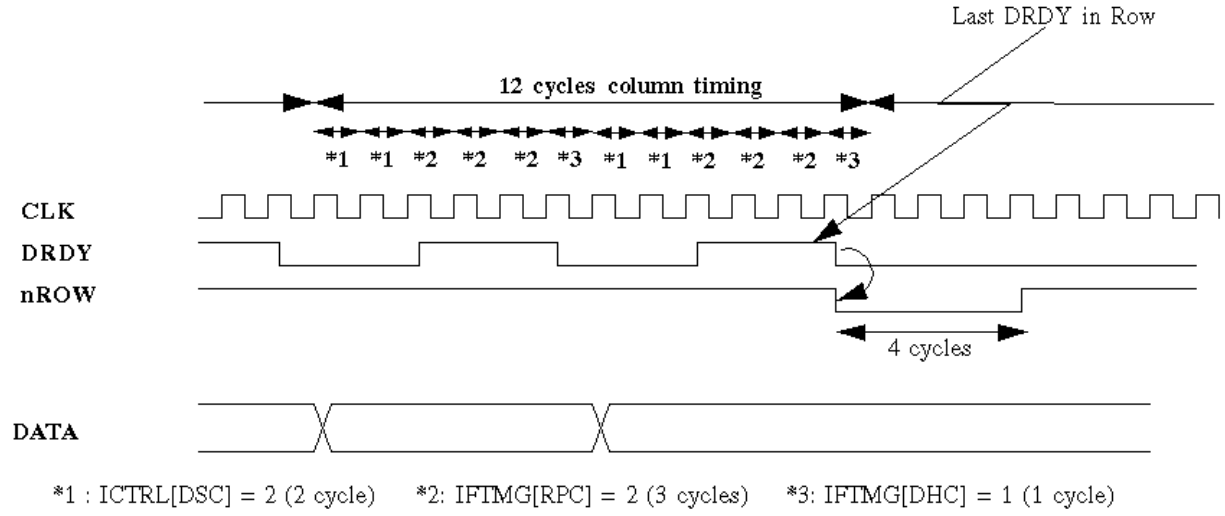

Figure 75. HDCS-2020 nROW Timing in Pulse Mode

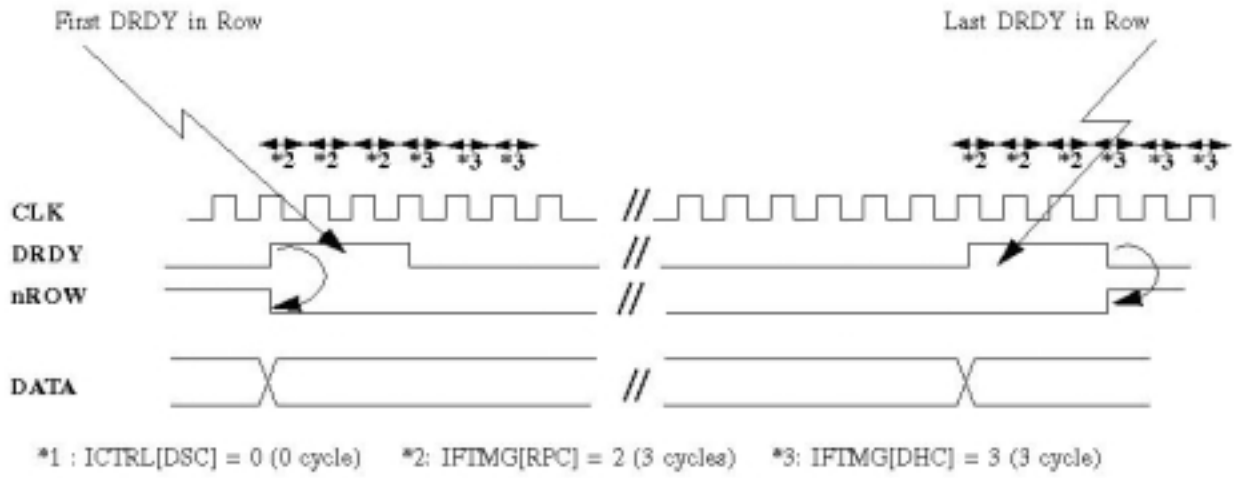

Figure 76. nROW Timing in level mode

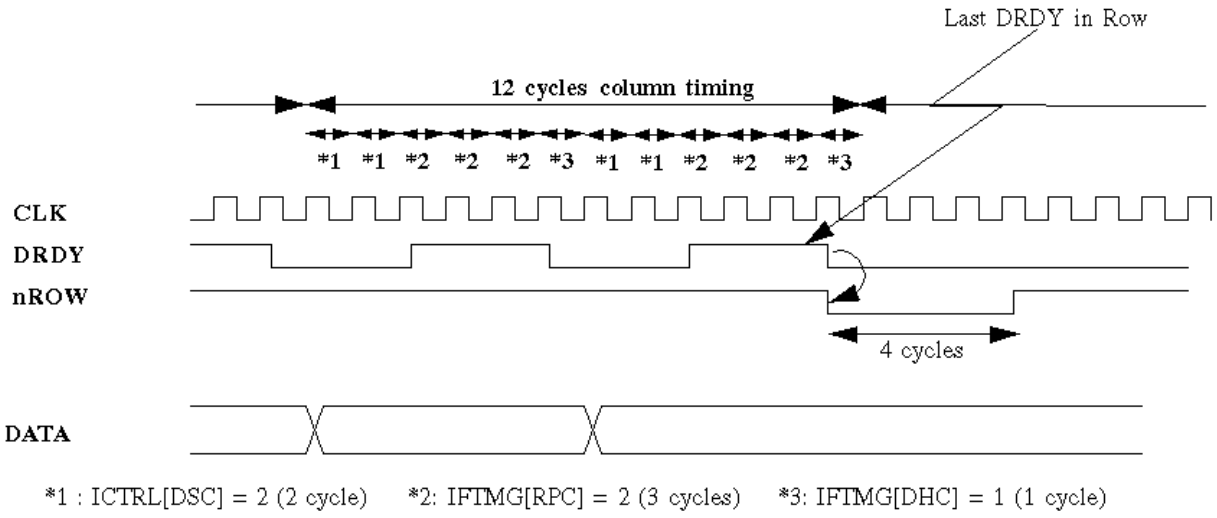

Figure 77. HDCS-1020(2020 in single channel mode) nROW Timing in End-of-Row DSYNC Pulse Mode

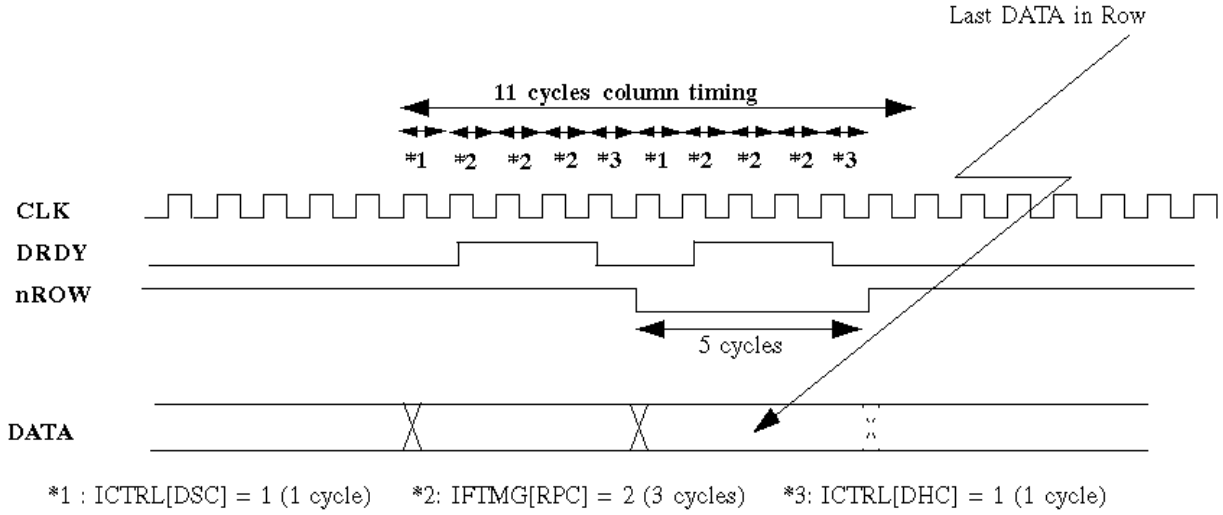

Figure 78. HDCS-2020 nROW Timing in End-of-Row DSYNC Pulse Mode

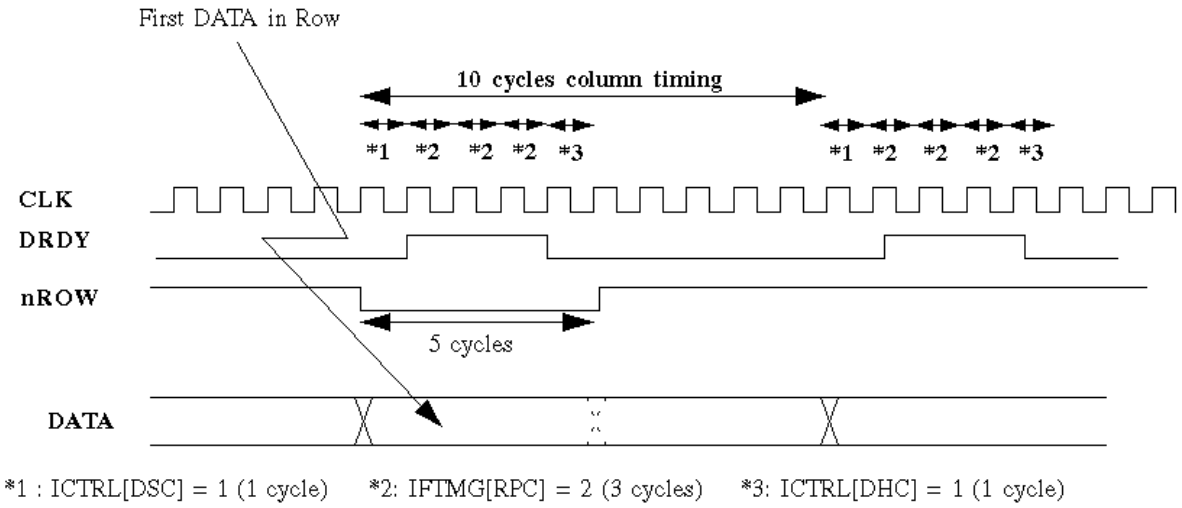

Figure 79. HDCS-1020(2020 in single channel mode) nROW Timing in Start-of-Row DSYNC Pulse Mode

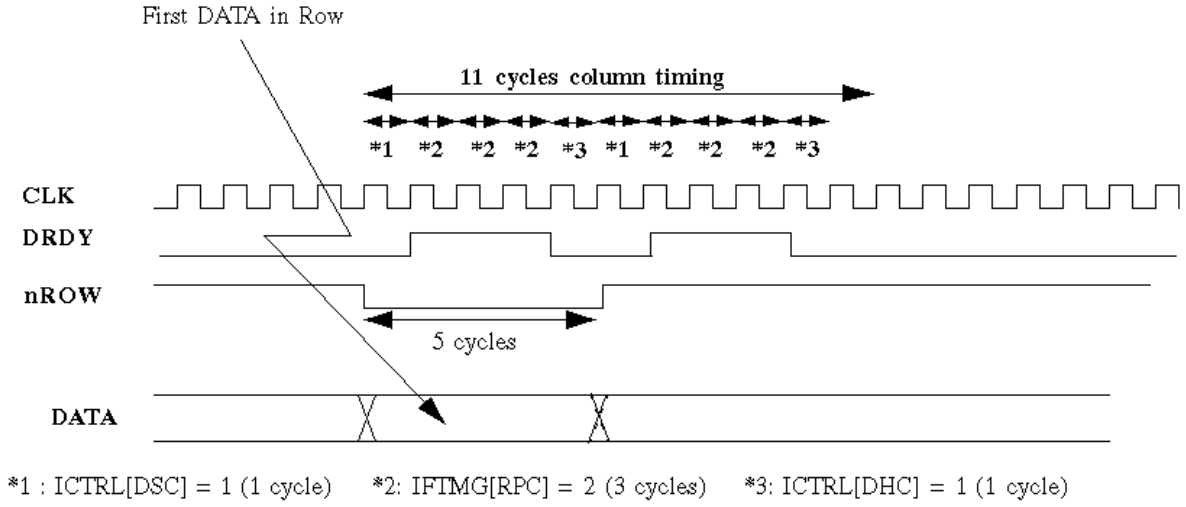

Figure 80. HDCS-2020 in nROW Timing in Start-of-Row DSYNC Pulse Mode

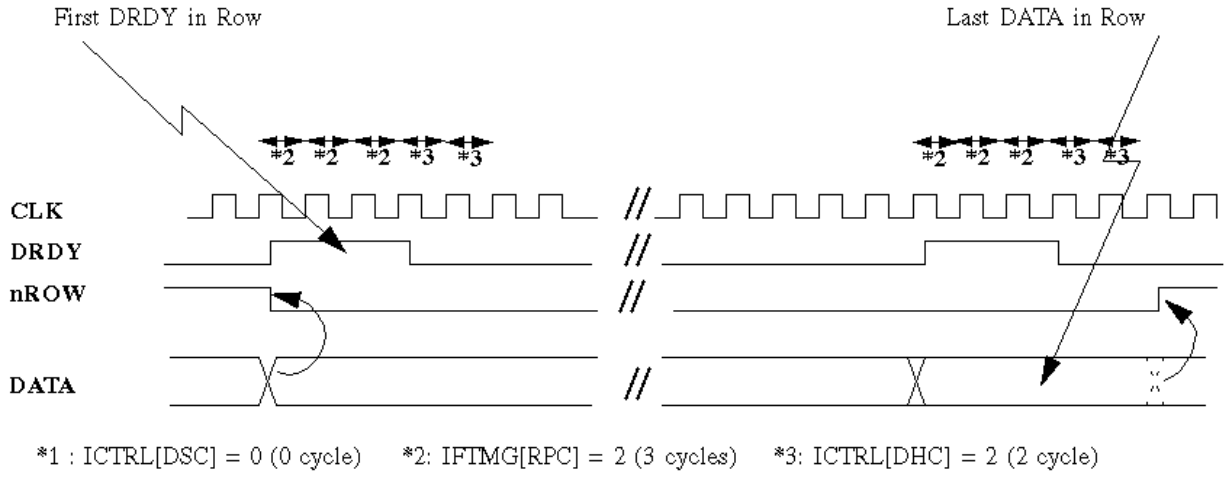

Figure 81. nROW Timing in DSYNC Level Mode

- CONNECTION INFORMATION:
  If nROW is unused, then do not connect it.
- PAD CONTROL:
  The STATDRV of the PDRV register controls the switching speed.

5.3.1.10 nIRQ_nCC

- DESCRIPTION:

ICE	IPD	LVC	DSYNC	Mode: Notes
'0'	'0'	'x'	'0'	Open Drain IRQ (interrupt request) with weak pull-up. Interrupt sources are in the STATUS register. Interrupt masks are in the IMASK register.
'0'	'1'	'x'	'0'	IRQ (interrupt request) driving to full high and low levels. Interrupt sources are in the STATUS register. Interrupt masks are in the IMASK register.
'1'	'x'	'0'	'0'	nCC (capture complete) pulse mode. Assert low for 4 cycles when the capture process completes. (After last DRDY trailing edge) If CONFIG[SFC] (stop when frame complete) equals '0', if CONTROL[RUN] is de-asserted, then nCC is asserted low for 4 cycles.
'1'	'x'	'1'	'0'	nCC (capture complete) level mode. Assert low when RUN bit is set. De-assert after capture completes. (After last DRDY trailing edge) If CONFIG[SFC] (stop when frame complete) equals '0', nCC is de-asserted when CONTROL[RUN] is de-asserted.
'1'	'x'	'0'	'0'	nCC (capture complete) DSYNC pulse mode. Assert low during last DATA of capture. If CONFIG[SFC] (stop when frame complete) equals '0', if CONTROL[RUN] is de-asserted, nCC asserts low for the duration of one DATA transfer. DRDY will be asserted as well.
'1'	'x'	'1'	'0'	nCC (capture complete) level mode. Assert low when RUN bit is set. De-assert after capture completes. (After last DRDY trailing edge) If CONFIG[SFC] (stop when frame complete) equals '0', nCC is de-asserted when CONTROL[RUN] is de-asserted. DRDY will pulse after nCC has been deasserted as per normal DATA transfer.

Table 57. nIRQ_nCC Status Flag Control

CONFIG[CFC] continuous frame capture	CONFIG[SFC] stop when frame complete	Capture Complete when…
'0'	'0'	At end of the first frame if CONTROL[RUN] is not de-asserted. Immediately after CONTROL[RUN] is de-asserted. If frame is stopped due to de-assertion of CONTROL[RUN] then: 1) If data has been transferred for current sensor row, then assert nROW if in nROW pulse mode. 2) If data has been transferred for current frame, then assert nFRAME if in FRAME pulse mode.
'0'	'1'	After last data is transferred for first frame is de-asserted in.
'1'	'0'	Immediately after CONTROL[RUN] is de-asserted. If frame is stopped due to de-assertion of CONTROL[RUN] then: 1) If data has been transferred for current sensor row, then assert nROW if in nROW pulse mode. 2) If data has been transferred for current frame, then assert nFRAME if in FRAME pulse mode.
'1'	'1'	After last data is transferred for frame that CONTROL[RUN] is de-asserted in.

Figure 58. Capture Complete Definition

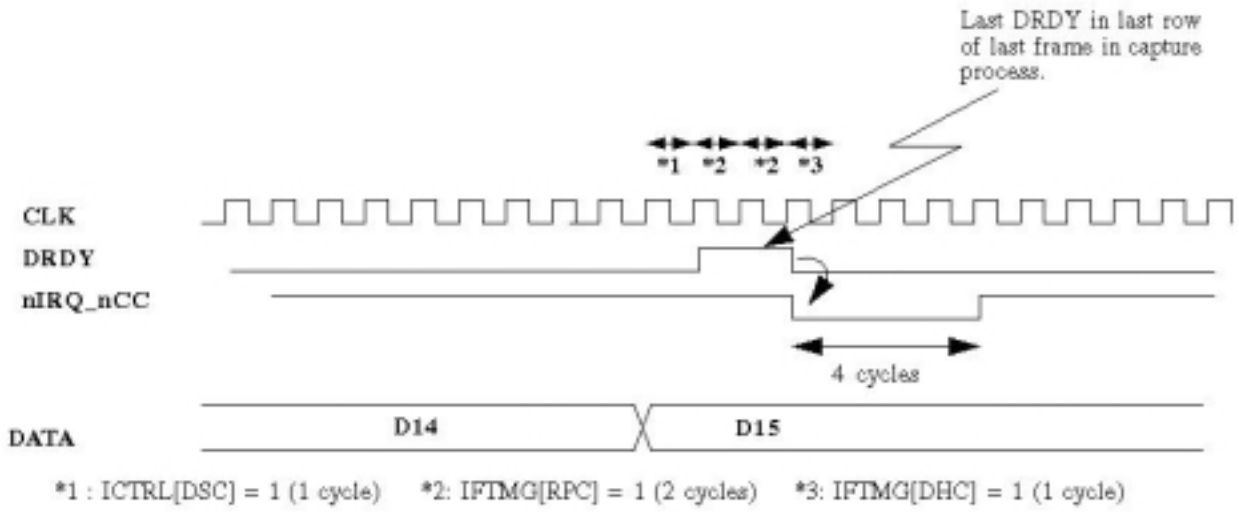

Figure 82. nIRQ_nCC Timing in Capture Complete Pulse Mode

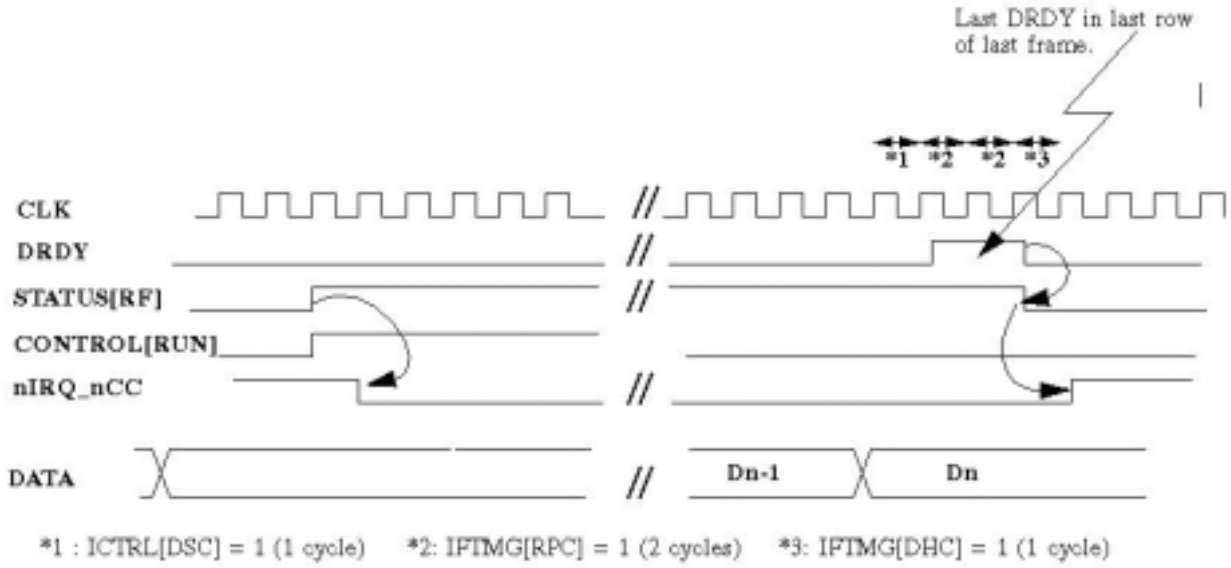

Figure 83. nIRQ_nCC Timing in Capture Complete Level Mode

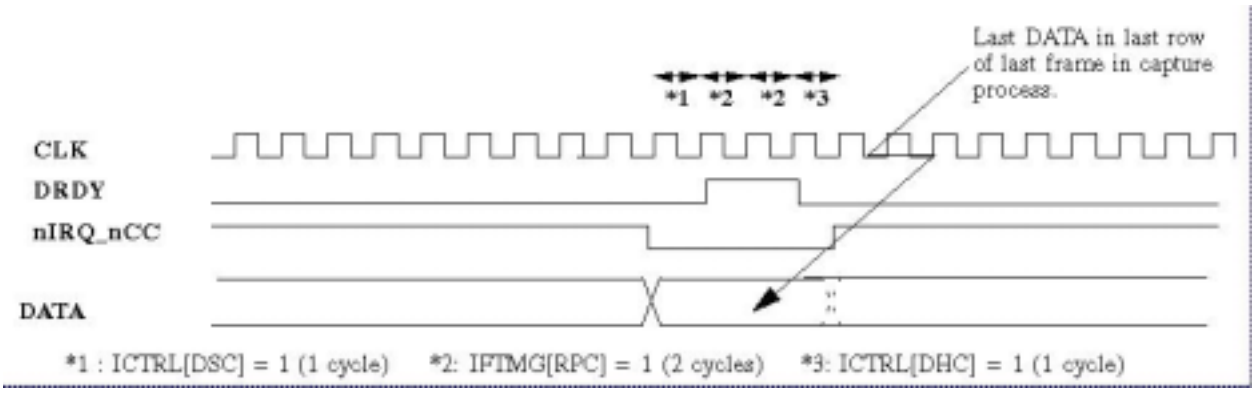

Figure 84. nIRQ_nCC Timing in Capture Complete DSYNC Pulse Mode

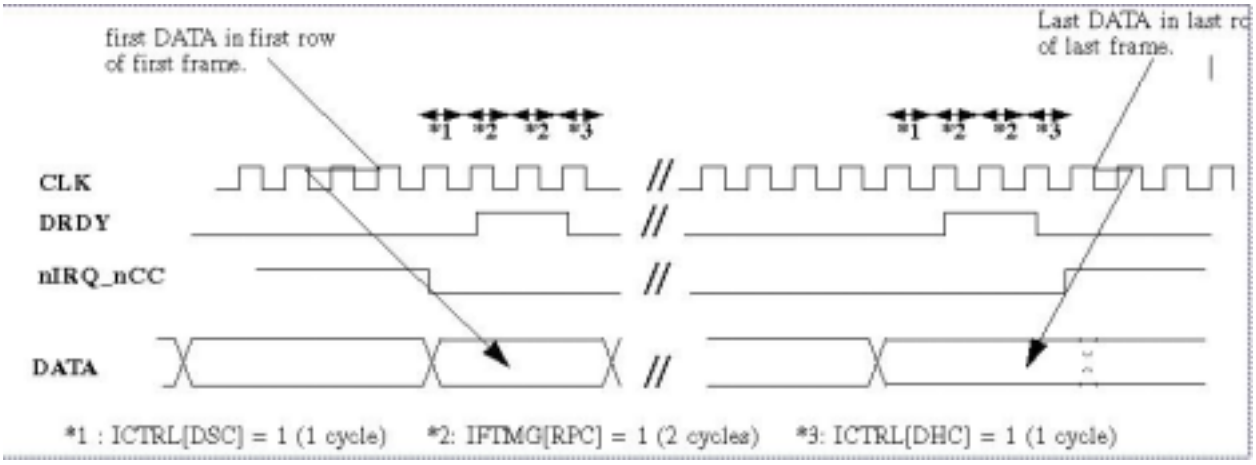

Figure 85. nIRQ_nCC Timing in Capture Complete DSYNC Level Mode

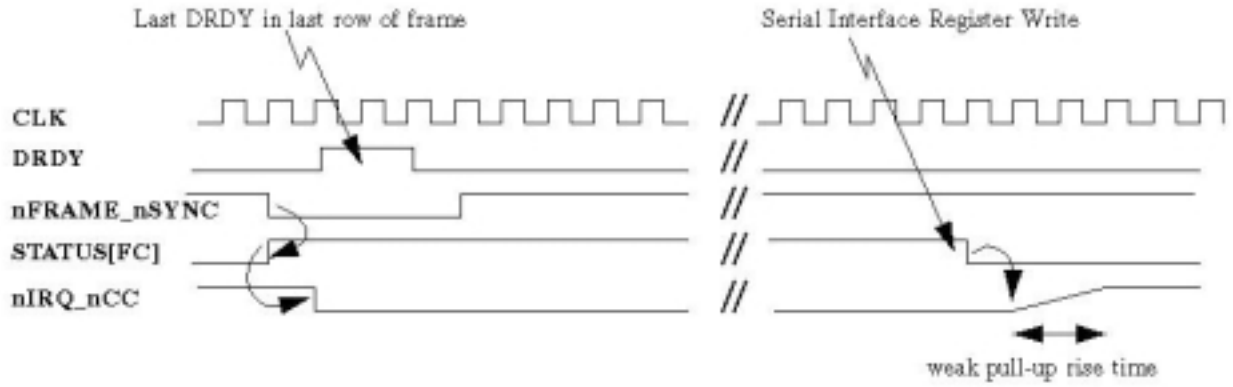

Figure 86. nIRQ_nCC Timing in Interrupt Request Mode with Open Drain. (interrupt on end of frame)

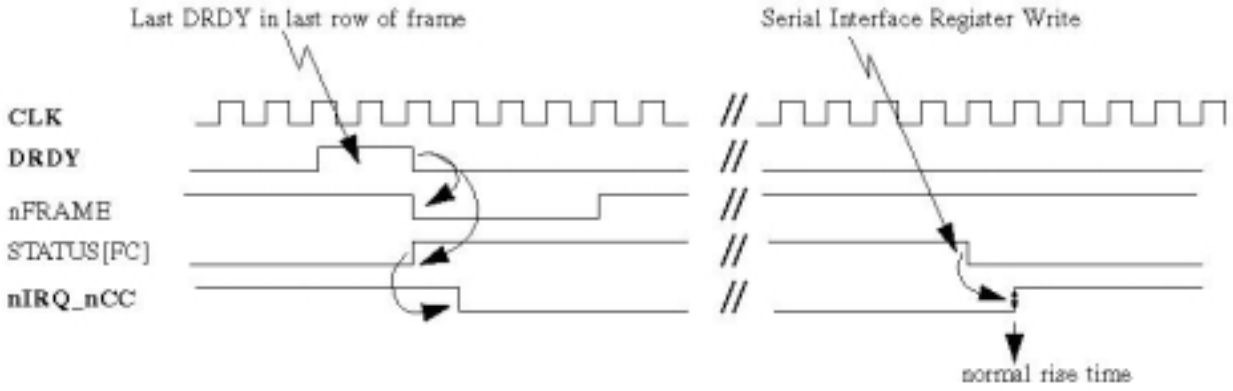

Figure 87. nIRQ_nCC Timing in Interrupt Request Mode without Open Drain. (interrupt on end of frame)

- CONNECTION INFORMATION:
  If nIRQ_nCC is unused, do not connect this pin.
- PAD CONTROL:
  The ICE field of the PCTRL register selects whether nIRQ-nCC functions as nIRQ or nCC. When functioning as nIRQ, the IPD field of the PCTRL register disables the weak internal pull up. When functioning as nIRQ, the IMASK register enables the events that cause nIRQ to assert low. The STATUS (interrupt status) register identifies the reason nIRQ was driven low. The STATDRV field of the PDRV register sets the switching speed for nIRQ_nCC. When ICE equals '1', the LVD field of the PCTRL register selects if nIRQ_nCC acts as a level or a pulse.

5.3.1.11 CLK

- DESCRIPTION:
  System Clock. The maximum frequency is 25 MHz for the HDCS-2020, 30 MHz for the HDCS-1020. The frame rate is related to frequency of CLK.
- CONNECTION INFORMATION:
  CLK must be connected for proper operation.
- PAD CONTROL:
  As a low power feature, CLK can be internally disabled by asserting nRST_nSTBY. The system will be in the reset state when nRST_nSTBY is de-asserted. The SLP bit of the CONFIG register also causes partial internal clock gating. The serial interface clocks are not disabled to allow turning SLP bit off. The system registers maintain their value while SLP is asserted, unless the RST bit of the CONFIG register is also asserted. See the Reset and Low Power section for more details.

5.3.1.13 nRST_nSTBY

- DESCRIPTION:
  Active low system reset input and stand-by mode input. Asserting nRST_nSTBY gates the system clock to save power and causes a system reset.
- CONNECTION INFORMATION:
  NRST_nSTBY must be connected.

5.3.1.14 VDD

- DESCRIPTION:
  Digital Power Supply.

5.3.1.15 GND

- DESCRIPTION:
  Digital Ground.

5.3.1.16 AVDD

- DESCRIPTION:
  Analog Power Supply.

5.3.1.17 AGND

- DESCRIPTION:
  Analog, Array, and Substrate Ground.

5.3.1.18 PVDD

- DESCRIPTION:
  Array Power Supply.

5.4 Serial Interface

The HDCS-1020 registers are initialized using the serial interface before operation begins..

The HDCS-1020 sensors function only as slaves, they do not initiate transfers.

IMODE0 Pin	IMODE1 Pin	
'0'	'0'	Synchronous serial slave
'0'	'1'	UART Half Duplex Slave

Figure 88. Serial Interface Modes

5.4.1 Synchronous Serial Slave Mode

Pin	Function
SCLK	Serial Transfer Clock (SCLK) synchronizes serial transmission of data bits on SDATA. SCLK is always driven by the master. The frequency of SCLK may vary throughout at transfer as long as its timing is greater than the minimum timing.
SDATA	Serial Data(SDATA) is used to send serial data bits in synchronization by SCLK. By default, SDATA is driven by the master. SDATA is driven by the slave in response to a request by the master. A response can be a single ACK bit, or a byte of data.

Figure 89. Synchronous slave pin definitions

Condition	Desc.
Data Bit	SDATA is stable while SCLK is high. SDATA transitions while SCLK is low.
Start bit	SDATA transitions High to Low while SCLK is high A start bit starts a new transfer
Stop bit	SDATA transitions Low to High while SCLK is high A stop bit terminates transfer.

Figure 90. Conditions Encoded by SCLK and SDATA

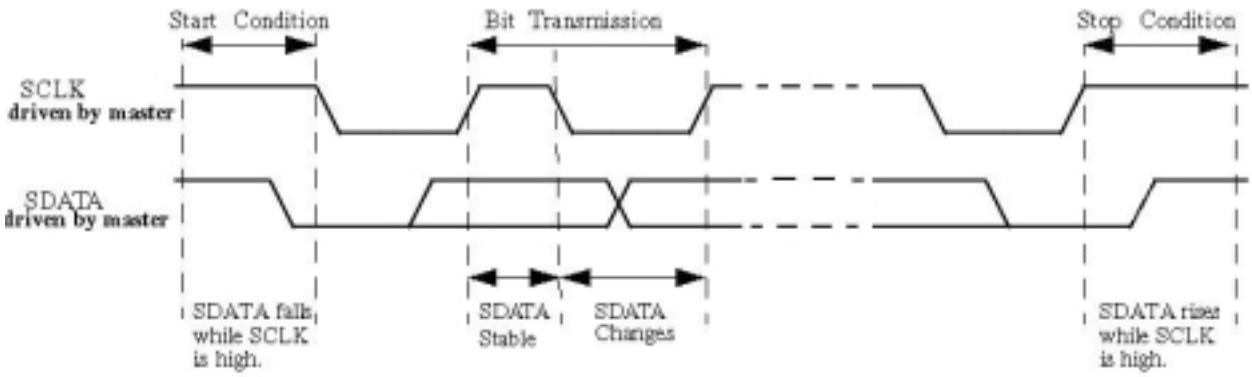

Figure 91. Synchronous serial bit timing

Pin	Function
Master Driven	Master Drives 8 data bits on SDATA. Slave responds by driving SDATA with a one bit acknowledge. ACK is defined as a '0'. It is an error condition if the slave does not acknowledge with ACK The first bit of the 8 data bits is the MSB [7]
Slave Driven	Slave Drives 8 data bits on SDATA. Master responds by driving SDATA with a one bit ACK or NACK. If ACK is defined as a '0', NACK is defined as a '1'. If Master responds with a ACK, the slave begins another slave driven packet on SDATA. If master responds with a NACK, the transfer ends. Control of SDATA is transferred to the master. The first bit of the 8 data bits is the MSB [7]

Figure 92. Synchronous Serial Types of packet transmissions

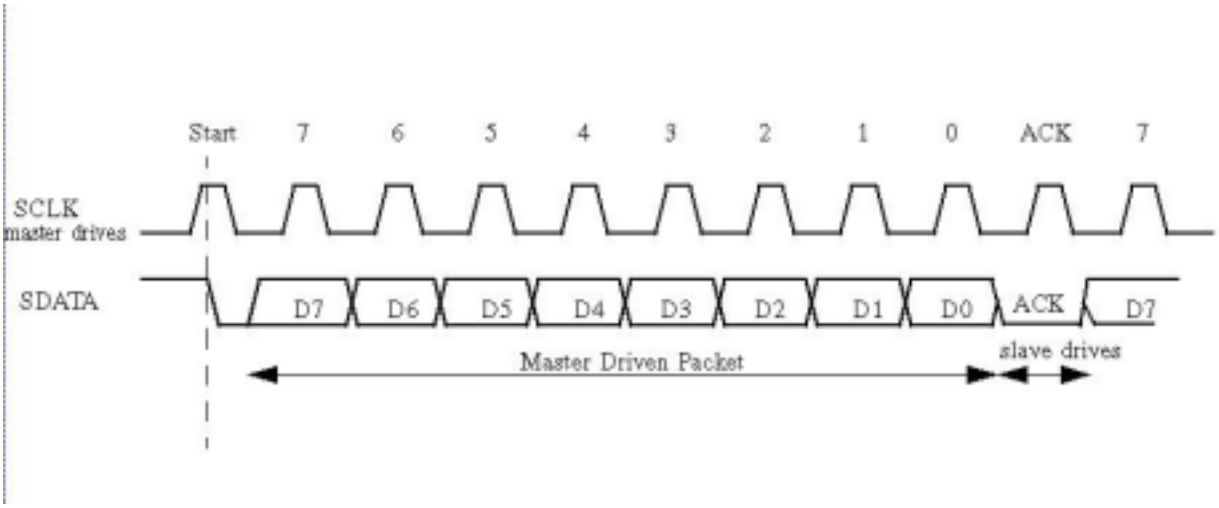

Figure 93. Master Driven Packet

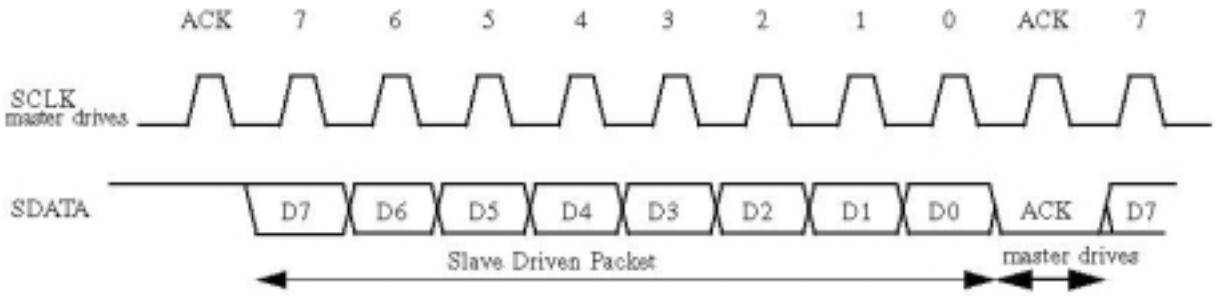

Figure 94. Slave Driven Packet

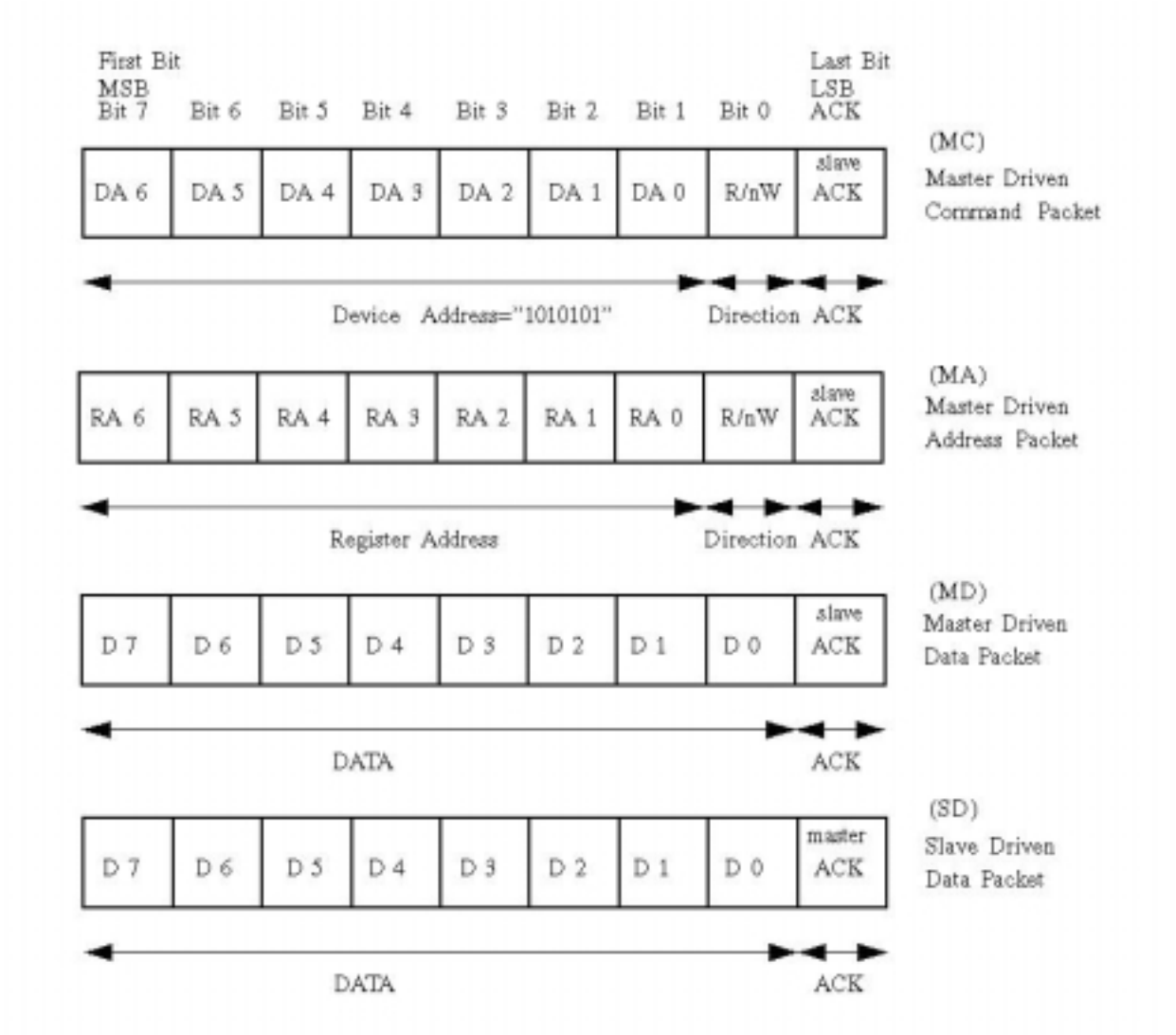

Figure 95. Synchronous Serial Packet Formats

The serial transfer sequence is initiated when the master issues a START condition. The transfer terminates at any point where the master issues a STOP condition, or where an ACK is not received.

Bit	Value	Description
ICTRL.DAD	"0"	Device Address is enabled. The first byte after a Start Bit is interpreted as a MC (master driven command) type. A slave will only respond if its device address matches the device address in the MC packet. The BONSEYE devise address is "1010101". After system reset ICTRL.DAD = "0".
	"1"	Device Address is disabled. The first byte after a Start Bit is interpreted as a MA (master driven address) type. This is intended for a point to point serial interface to save a byte in the protocol.
ICTRL.AAD	"0"	Auto Address Increment is enabled. The MA packet defines the starting register address for the next byte to be transferred. After each MD packet the register address is automatically incremented so the next MD packet will transfer the data for the next register. After system reset ICTRL.AAD = "0";
	"1"	Auto Address Increment is disabled. The MA packet defines the starting register address for the next byte to be transferred. Each subsequent MD packet will repeat the value of the same register defined by the MD packet. This is intended to provide a method of polling for the status regs.
SDA_HOLD		SDA_HOLD controls the number of cycles after SCL falls before BONSEYE/EYELITE stops driving data on SDA. HOLD_CYCLES = 2 + (SDA_HOLD * 2). VALUE AFTER RESET = "011" = 8 cycles. (320ns @ 25 MHz) (333nS @ 24MHz)
SDA_SETUP		When BONSEYE/EYELITE is driving a data bit, SDA_SETUP controls the number of cycles after SCL falls until data is driven on SDA. SETUP_CYCLES = 2 + (SDA_HOLD * 2) + (SDA_SETUP * 2) VALUE AFTER RESET = "1001" = 26 cycles (1040ns @ 25 MHz) (1080nS @ 24MHz)

Figure 96. Register Bits Affecting Synchronous Serial Transfer Sequence

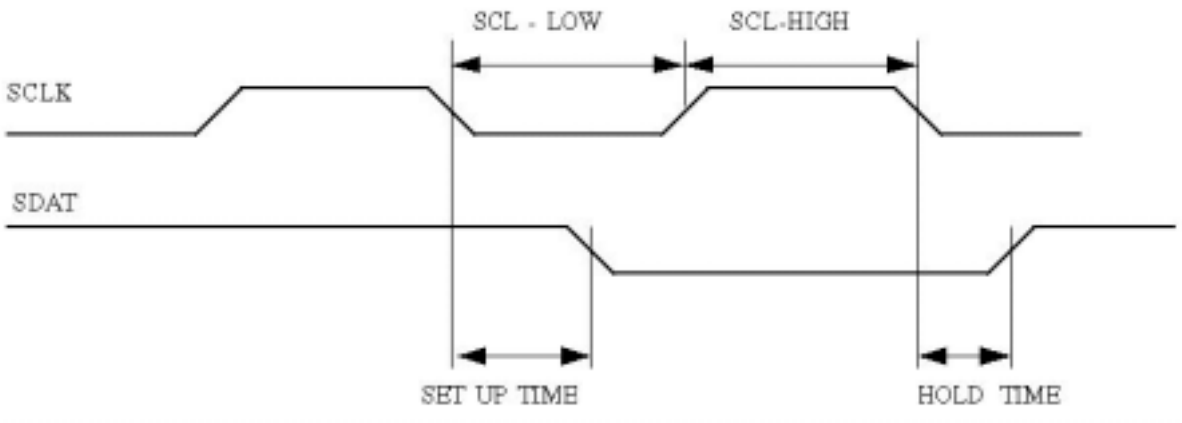

Figure 97. SCL-SDA Timing

Specification	Minimum number of cycles
CLOCK HIGH	4
CLOCK LOW	4 + (SDA_HOLD*2) + (SDA_SETUP*2)

Table 59. Minimum SCL Timing

Packet Number		1	2	3	4	5	6	
Packet Type		MC	MA	MD	MD	MD	MD	
Bit		7654_3210_A	7654_3210_A	7654_3210_A	7654_3210_A	7654_3210_A	7654_3210_A	
SDATA (master)	start	1010_1010_x	0001_1110_x	0001_0010_x	0011_0100_x	0101_0110_x	0111_1000_x	stop
SDATA (slave)	x	xxxx_xxxx_0	xxxx_xxxx_0	xxxx_xxxx_0	xxxx_xxxx_0	xxxx_xxxx_0	xxxx_xxxx_0	x
Register Address AAD=0	x	x	x	x0F	x10	x11	x12	x13
Register Address AAD=1	x	x	x	x0F	x0F	x0F	x0F	x0F

Write 4 registers (addresses x0F, x10, x11, x12) with data (x12, x34, x56, x78). ICTRL[DAD]='0'

Figure 98. Serial Synchronous N Byte Write using Device Address

Packet Number		1	2	3	4	5	
Packet Type		MA	MD	MD	MD	MD	
Bit		7654_3210_A	7654_3210_A	7654_3210_A	7654_3210_A	7654_3210_A	
SDATA (master)	start	0001_1110_x	0001_0010_x	0011_0100_x	0101_0110_x	0111_1000_x	stop
SDATA (slave)	x	xxxx_xxxx_0	xxxx_xxxx_0	xxxx_xxxx_0	xxxx_xxxx_0	xxxx_xxxx_0	x
Register Address AAD=0	x	x	x0F	x10	x11	x12	x13
Register Address AAD=1	x	x	x0F	x0F	x0F	x0F	x0F

Write 4 registers (addresses x0F, x10, x11, x12) with data (x12, x34, x56, x78). ICTRL[DAD]='1'

Figure 99. Serial Synchronous N Byte Write without Device Address

Packet Number		1	2	3	4	5	6	
Packet Type		MC	MA	MC	SD	SD	SD	
Bit		7654_3210_A	7654_3210_A	7654_3210_A	7654_3210_A	7654_3210_A	7654_3210_A	
SDATA (master)	start	1010_1010_x	0001_1110_x	start	1010_1011_x	xxxx_xxxx_0	xxxx_xxxx_0	xxxx_xxxx_1	stop
SDATA (slave)	start	xxxx_xxxx_0	xxxx_xxxx_0	x	xxxx_xxxx_0	0001_0010_x	0011_0010_x	0101_0110_x	x
AAD=0									
Register Address	x	x	x	x0F	x0F	x0F	x10	x11	x12
AAD=0									
SDATA (slave)	start	xxxx_xxxx_0	xxxx_xxxx_0	x	xxxx_xxxx_0	0001_0010_x	0001_0010_x	0001_0010_x	x
AAD=1									
Register Address	x	x	x	x0F	x0F	x0F	X0F	X0F	X0F
AAD=1									

Read 3 registers (addresses x0F, x10, x11) which contain data (x12, x34, x56).
ICTRL[DAD]=0
NOTE: When DAD = 0 a write sequence is used to setup the read address.

Figure 100. Serial Synchronous N Byte Read using device address

Packet Number		1	2	3	4	5	
Packet Type		MA	SD	SD	SD	SD	
Bit		7654_3210_A	7654_3210_A	7654_3210_A	7654_3210_A	7654_3210_A	
SDATA (master)	start	0001_1111_1	xxxx_xxxx_0	xxxx_xxxx_0	xxxx_xxxx_0	xxxx_xxxx_1	stop
SDATA (slave)	x	xxxx_xxxx_0	0001_0010_x	0011_0100_x	0101_0010_x	0111_1000_x	x
AAD=0							
Register Address	x	x	x0F	x10	x11	x12	x13
AAD=0							
SDATA (slave)	x	xxxx_xxxx_0	0001_0010_x	0001_0010_x	0001_0010_x	0001_0010_x	x
AAD=1							
Register Address	x	x	x0F	x0F	x0F	x0F	x0F
AAD=1							

Write 4 registers (addresses x0F, x10, x11, x12) with data (x12, x34, x56, x78). ICTRL[DAD]='1'

Figure 101. Serial Synchronous N Byte Read without Device Address

5.4.3 Serial Interface: UART Half-Duplex Slave Mode

UART Half-Duplex Slave Mode uses 2 pins: RxD (receive serial data) and TxD (transmit serial data). The RxD pin is driven by the master, and TxD is driven by the slave (the HDCS sensor).

Each serial bit is driven for a fixed time duration called the Bit Time. A Bit Time is 16 roll-overs of the Bit Time Counter. The number of system clocks required to increment the Bit Time Counter is determined by the BRATE and BFRAC registers. The value of a data bit is the majority vote of its value at the beginning of the 7^{th}, 8^{th}, and 9^{th} roll-overs of the Bit Time Counter.

Data is transmitted in 10 bit packets. The first bit of a packet is the start bit. The start bit (‘0’) is followed by 8 data bits. The first data bit is the LSB. The 8 data bits are followed by one stop bit (‘1’).

The default (idle) state of RxD and TxD is ‘1’. When RxD transitions low for the Start Bit, the HDCS sensor synchronizes by resetting its Bit Time Counter and starts the receiving process.

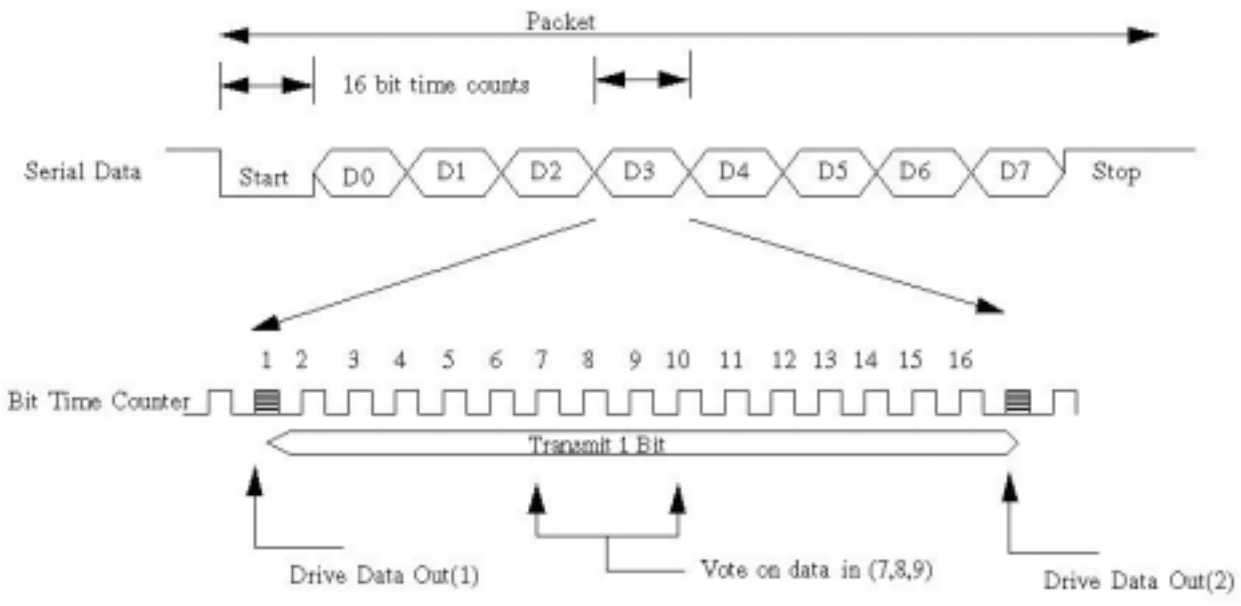

Figure 102. UART Bit Protocol

$$ClocksPerBitTime = (16 \times \{BRATE + 1\}) + (BFRAC)$$

$$BitTime = ClockPeriod \times ClocksPerBitTime$$

$$BaudRate = (ClockFrequency) / (ClocksPerBitTime)$$

Figure 103. Bit Rate Equations

BRATE = 155 BFRAC = 4

ClockFrequency = 24 MHz

ClockPeriod = $1/24 \times 10^{-6} = 41.67 \times 10^{-9}$ nS

BitTime = 104.17 uS = $2500 \times 41.67 \times 10^{-9}$ nS = $2500 \times 1/24 \times 10^{-6}$

ClocksPerBitTime = $2500 = (16 \times 156) + (4)$

BaudRate = 9600 Baud = $(24 \times 10^{6}) / (2500)$

Figure 104. Initial Bit Rate Setting

REGISTER[FIELD]	UART FUNCTION
BRATE	Sets the Baud Rate. (Full Baud rate is set by BRATE + BFRAC[BPF]) The new setting does not take effect until the end of the current transfer. Example: if there is an 8 byte write, and BRATE is the third byte written, the new BRATE value does not take effect until after the eight byte is written.
BFRAC[BPF]	Fractional part of the BAUD rate. (Full Baud rate is set by BRATE + BFRAC[BPF]) The new setting does not take effect until the end of the current transfer. Example: if there is an 8 byte write, and BFRAC is the third byte written, the new BFRAC[BPF] value does not take effect until after the eight byte is written.
BFRAC[SEND_DELAY]	Number of stop bits to delay when sending bytes. This applies to delay before sending the first byte, and delay between subsequent bytes. There is always 1 stop bit delay, and SEND_DELAY is the number of additional stop bits to delay.
ITMG[AAD]	Disables automatic increment of register address for multiple byte read/write. Useful for polling status register.

Table 60. System Registers Affecting UART Operation

BAUD RATE TARGET	BRATE	BFRAC	CYC/BIT IDEAL	CYC/BIT ACTUAL	%ERROR
5,838 (MINIMUM)	0xFF	0x0F	4111	4111	0.00%
9,600	0x9B	0x04	2500	2500	0.00%
19,200	0x4D	0x02	1250	1250	0.00%
28,800	0x33	0x01	833.33	833	0.04%
38,300	0x25	0x0A	618.56	618	0.09%
57,600	0x19	0x00	416.67	416	0.16%
115,200	0x0C	0x00	208.33	208	0.16%
1,500,000 (MAXIMUM)	0x00	0x00	16	16	0.00%

Table 61. BFRAC/BRATE Settings for common Baud Rates, 24 MHz Clock

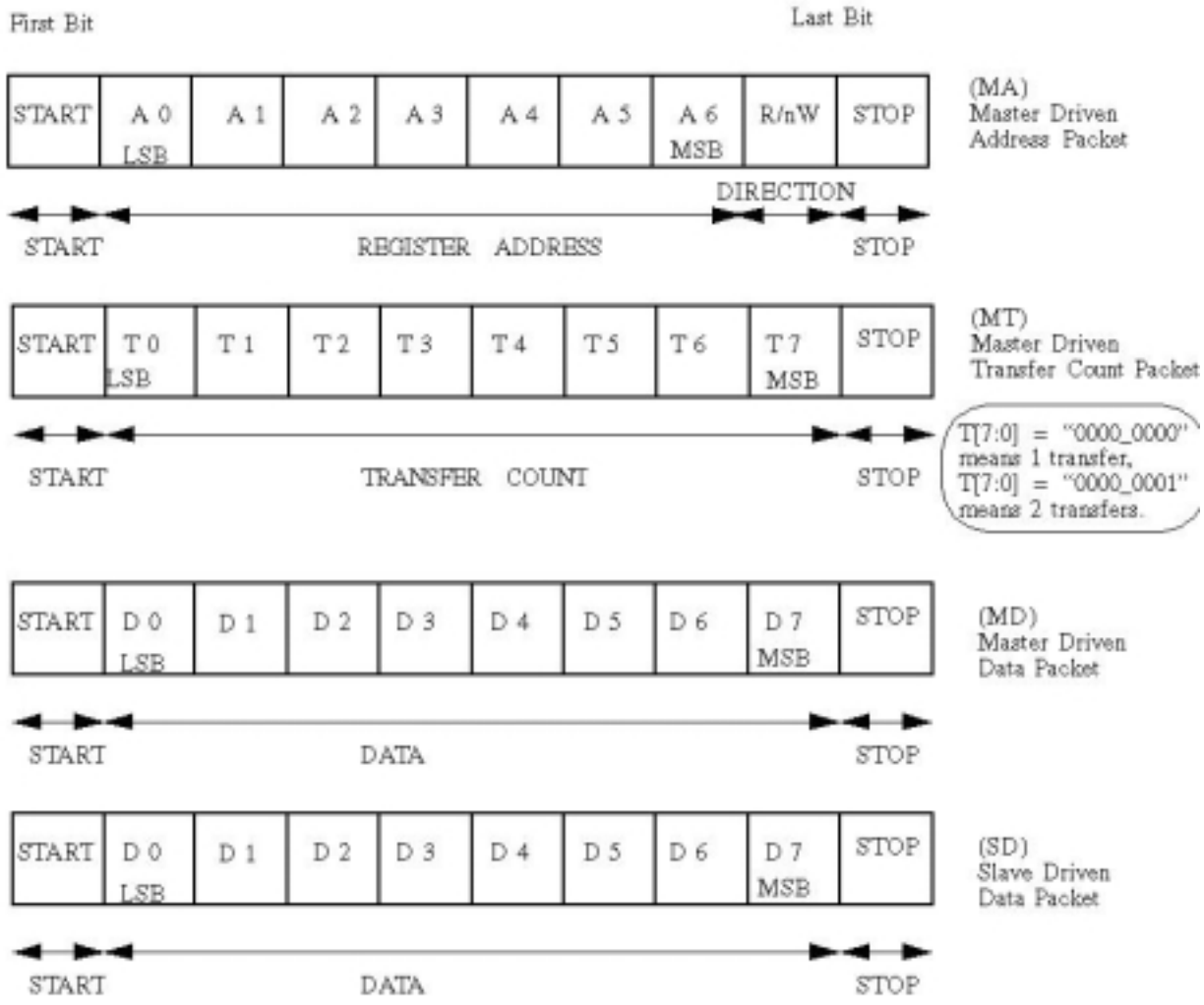

Figure 105. UART Packet Formats

The serial communication sequence is initiated when the master transmits a start bit on RxD. The master transmits the first 2 packets. The first packet (MA) indicates the starting register address and whether it is a read or a write sequence. The second packet (MT) indicates the number of bytes to be transferred. For a write sequence the master transmits the number of data packets (MD) on RxD equal to the transfer count. For a read sequence the slave transmits the number of data packets (SD) on TxD equal to the transfer count.

The AAD (automatic address increment disable) bit of the ICTRL register alters the behavior of the serial communication sequence. When AAD equals ‘0’, the register address is automatically incremented after each MD or SD packet. When AAD equals ‘1’, the register address does not increment after MD or SD packets. This is intended for use in register polling.

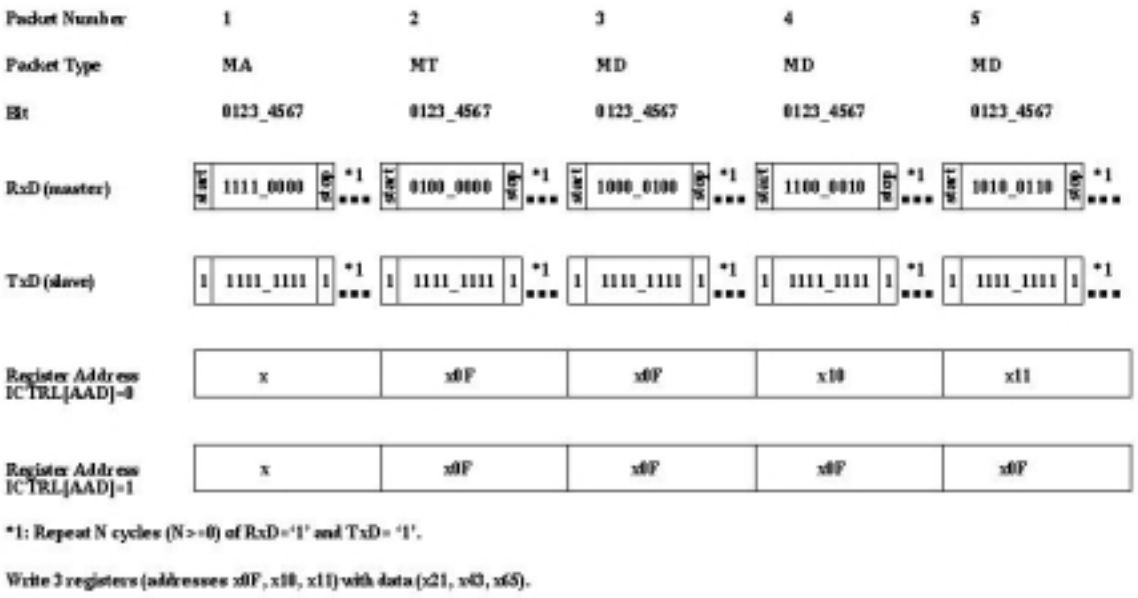

Figure 106. UART N Byte Write

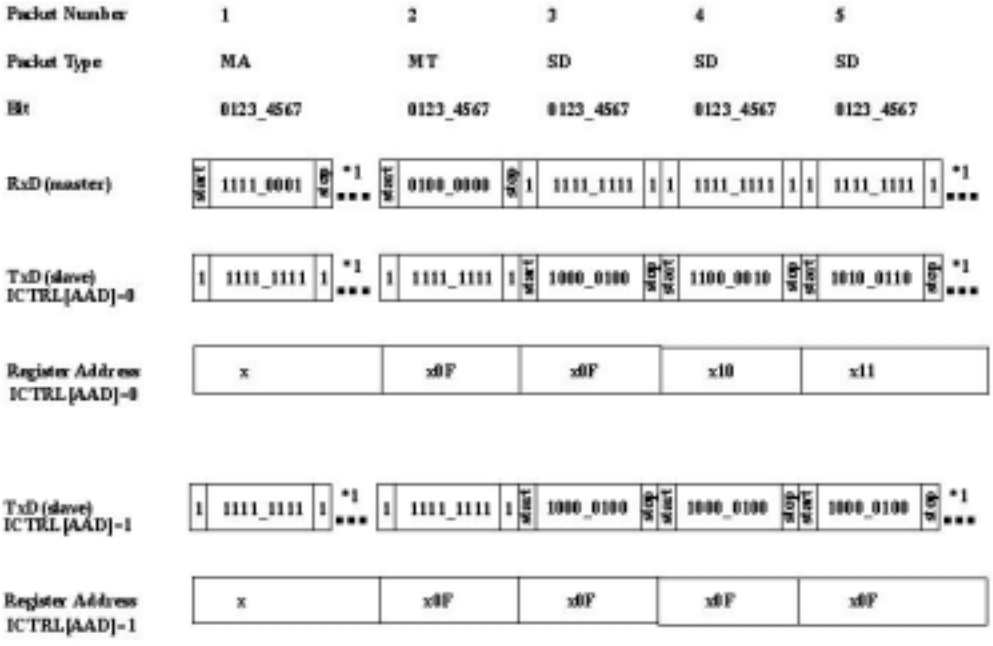

Figure 107. UART N Byte Read

5.4.4 UART Sequence Diagrams

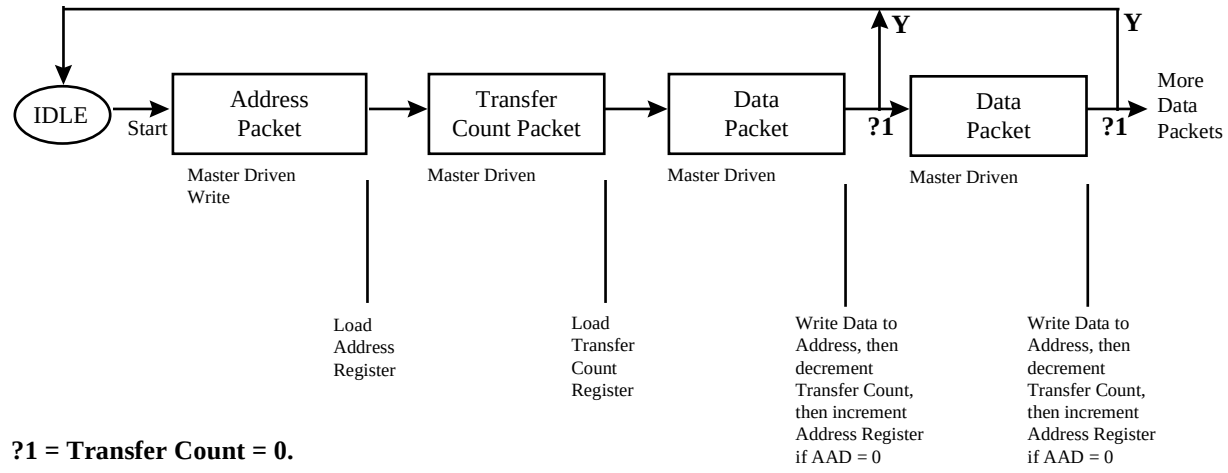

Figure 108. UART Write Sequence

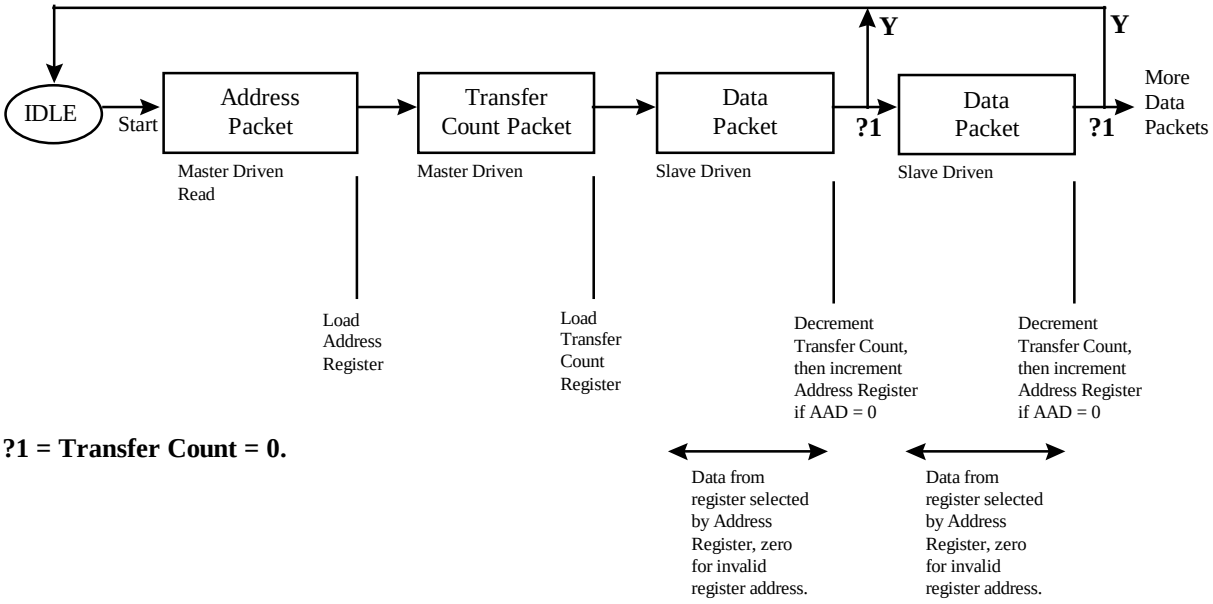

Figure 109. UART Read Sequence

6. System Reset and Low power modes

6.1 System Reset

A system hard reset is required before the HDCS sensor will function properly. The sensor may be reset by asserting the nRST_nSTBY pin (hard reset) for 40 cycles with the clock running. A partial reset may be done by setting the RST bit of the CONFIG register (soft reset), or by the SLP, PWR fields of the CONTROL register (soft sleep).

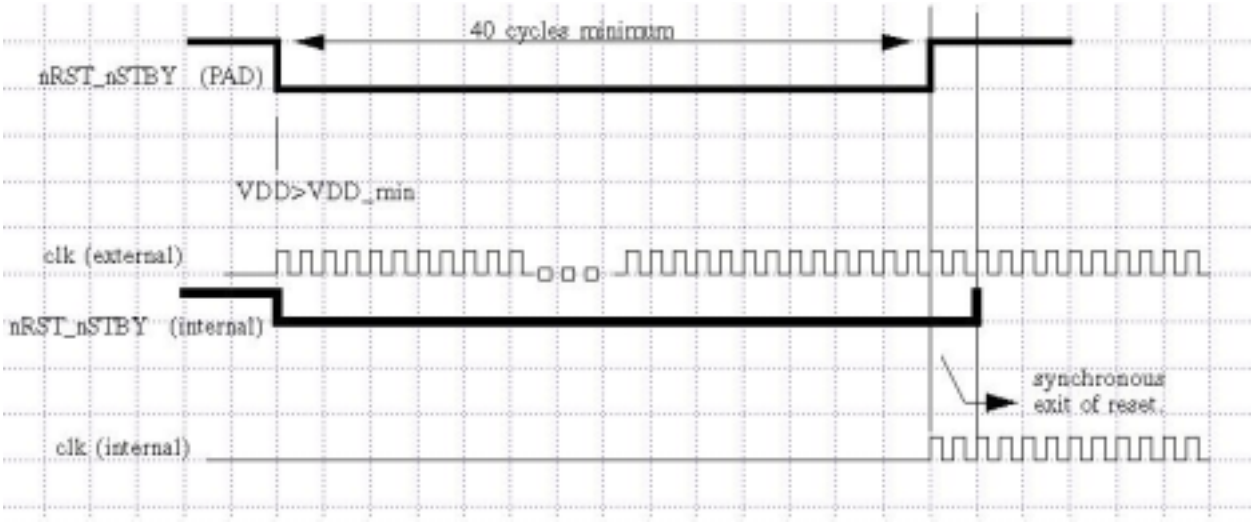

Figure 110. System Reset Using External nRST_nSTBY pin

RESET TYPE	HOW TO INVOKE	WHAT IS RESET	PWR/CLOCK STATUS
HARD	pin nRST_nSTBY = "0"	All registers, except : 1) clock synchronization flipflops.	Analog Power Disabled. All Clocks stopped, except: 1) clock synchronizing flipflops
SOFT-RESET	Control[Rst] = "1" Deactivate by write to Control reg.	All registers, except: 1)clock synchronization flipflops. 2) serial interface flipflops 3) Control register.	Analog Power Disabled. All Clocks running
SOFT-SLEEP	Control[Slp] = "10" Deactivate by write to Control reg.	All registers, except: 1)clock synchronization flipflops. 2) serial interface flipflops 3) All system registers.	Analog Power Disabled. All Clocks stopped, except: 1) clock synchronizing flipflops 2) Serial Interface 3) Control Register
LOW-POWER	Control[Pwr]= "1" AND Control[Run] = 0 Deactivate by write to Control reg or Turning off the RUN bit	All registers, except: 1)clock synchronization flipflops. 2) serial interface flipflops 3) All system registers.	Analog Power Disabled. All Clocks stopped, except: 1) clock synchronizing flipflops 2) Serial Interface 3) Control Register

Table 62. Reset Types and Clock Modes

6.2 Low Power / Clock Domains

The HDCS sensor provides 2 low power modes by: 1) turning off the analog DC currents and 2) gating clocks to the digital logic.

7. Packaging

7.1 General Package Specs

- # of Leads (package): 32 (8 per side) J-leads

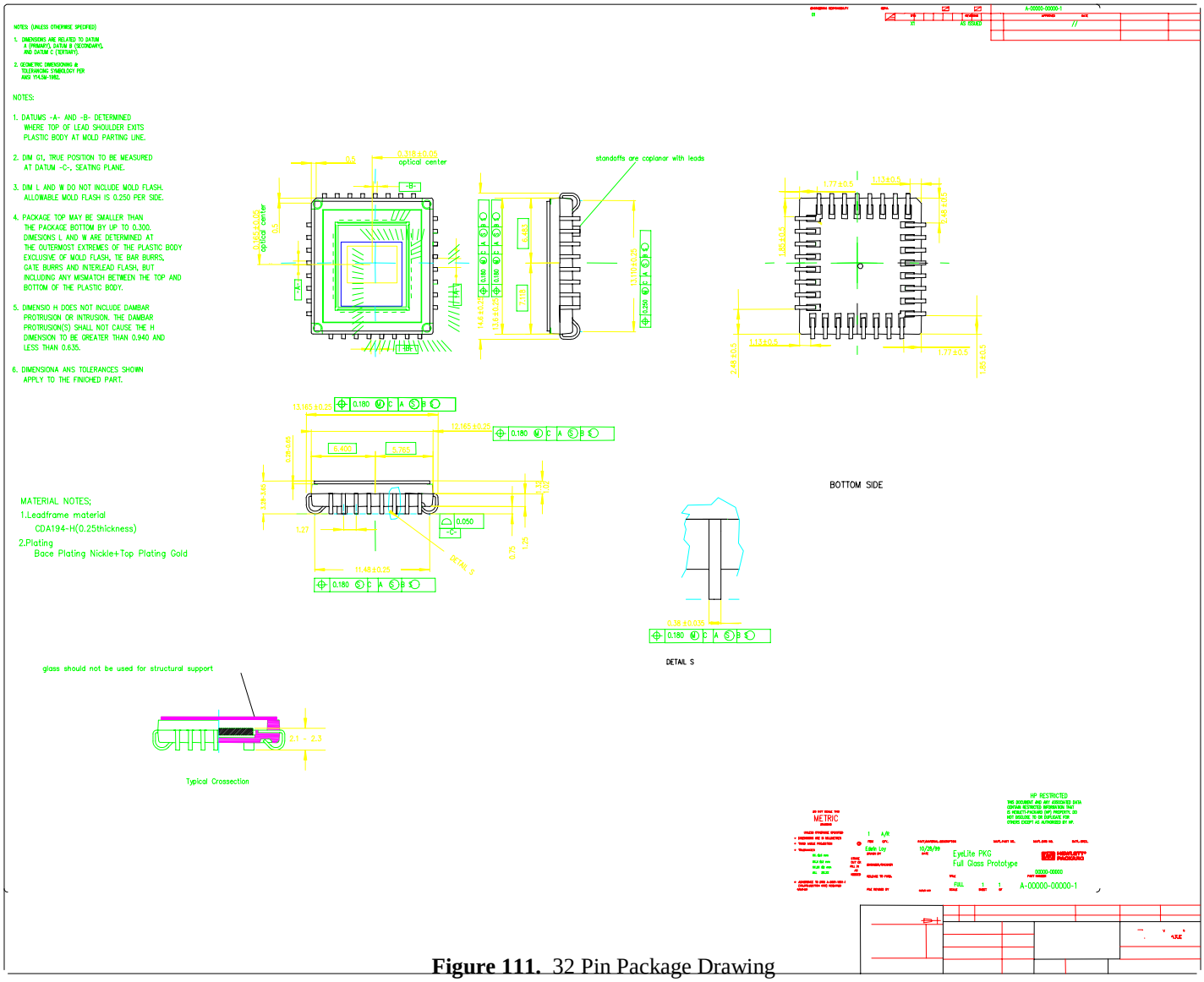

Figure 111. 32 Pin Package Drawing

7.2 HDCS-2020 Package Pin List

PIN No.	Pin Name	PIN No.	Pin Name	PIN No.	Pin Name
1	DATA7	12	GND	23	IMODE1
2	AGND	13	DATA3	24	IMODE0
3	AVDD	14	DATA2	25	NRST_nSTBY
4	VDD	15	DATA1	26	nROW
5	GND	16	DATA0	27	AGND
6	DRDY	17	VDD	28	PVDD
7	CLK	18	GND	29	SCLK_RxD
8	DATA6	19	AGND	30	SDATA_TxD
9	DATA5	20	AVDD	31	DATA9
10	DATA4	21	NFRAME_nSYNC	32	DATA8
11	VDD	22	NIRQ_nCC		

Table 63. HDCS-2020 Package Pin List

7.3 HDCS-1020 Package Pin List

PIN No.	Pin Name	PIN No.	Pin Name	PIN No.	Pin Name
1	DATA5	12	GND	23	IMODE1
2	AGND	13	DATA1	24	IMODE0
3	AVDD	14	DATA0	25	NRST_nSTBY
4	VDD	15	NC	26	nROW
5	GND	16	NC	27	AGND
6	DRDY	17	VDD	28	PVDD
7	CLK	18	GND	29	SCLK_RxD
8	DATA4	19	AGND	30	SDATA_TxD
9	DATA3	20	AVDD	31	DATA7
10	DATA2	21	NFRAME_nSYNC	32	DATA6
11	VDD	22	NIRQ_nCC		

Table 64. HDCS-1020 Package Pin List

8. Electrical and Power Specifications

8.1 Electrical Specifications

This section covers the electrical and power specifications of the HDCS Image Sensor.

8.2 Absolute Maximum Ratings

Specification	Description	Min	Max	Units
VDD	Power supply voltage		3.6	V
V_{port}	DC input voltage at any port		3.6	V
Tj	Junction temperature	0	110	C

Table 65. Absolute Maximum Rating

8.1.2 DC Power Specifications

Specification	Description	Conditions	Min	Typ	Max	Units
VDD	Operating Power Supply Voltage		3.0	3.3	3.6	V
IDDp	Power Down Supply Current	f=0MHz		TBD		uA
IDDs	Standby Current	f=0MHz		29		mA
IDDd	Dynamic Operating Current	f=20MHz		79		mA

Table 66. DC Specifications

8.1.3 Pin Capacitance

Specification	Description	Max	Units
CinCLK	CLK Input Port Capacitance	2	pF
Cin	All Other Input Port Capacitances	1	pF

Table 67. Pin Capacitance

9. Glossary

ADC Acronym for “analog to digital converter”.

APS Acronym for “Active Pixel Sensor”.

CIF Acronym for “Common Intermediate Format”. Commonly used to define a pixel array of 352 columns by 288 rows.

Column Processing Refers to the portion of the row processing time that is used to perform an analog to digital conversion on the previously sampled pixel information for all of the pixels in one row of the selected image window.

Exposure Duration of time that transpires from when a pixel is reset until it is subsequently sampled. Used synonymously with integration time.

fps Acronym for “frames per second”.

Image Capture Process Sequence of operations executed to expose, sample, convert, and output image sensor data. May be one or more frames.

Image Window Rectangular region of the image sensor array that is sampled, converted, and output during an image capture process. The window coordinates are defined by the FWROW, FWCOL, LWROW, and LWCOL registers.

PGA Acronym for “programmable gain amplifier”.

Pre-Integration Period The period of time starting when an image capture process is initiated and ending when the first row in the image window is sampled. Essentially equivalent in duration to the exposure duration, but it only occurs prior to sampling the first frame sampled during each image capture process.

Row Processing Refers to the sequence of operations required to sample one row of pixels in the selected image window, convert the analog information to digital format and output it.

Timing Controller Start Overhead Number of clock cycles required for the internal timing controller to begin operating after the internal assertion of the RUN bit of the CONTROL register.

VGA Acronym for “video graphics adapter”. Commonly used to define a pixel array of 640 columns by 640 rows.