Photobit®
Behind Every Great Digital Image™

PB-0100 / PB-0101
1/5-Inch CMOS Active-Pixel Digital Image Sensors

©2000 Photobit Corporation. All rights reserved.

Photobit, the wave and binary symbol, and Behind Every Great Digital Image are registered trademarks, and TrueBit, TrueColor, Fully Flexible Open Architecture, Serial Host Interface Port, and Leading the Active Pixel Revolution are trademarks, of Photobit Corporation in the United States and other countries. I2C is a proprietary interface bus and trademark of Philips Semiconductors. Other trademarks referenced are the property of their respective owners and are used to identify specific products or services.

Photobit products are protected under U.S. Patents 5,471,515; 5,793,322; 5,841,126; 5,880,691; 5,886,659; 5,887,049; 5,909,026; 5,949,483; 5,952,645; and 5,990,506. Other U.S. and foreign patents are pending. Photobit conveys no license under its patents, copyrights, or mask work rights, or any rights of others; nor does Photobit represent that products shown or described herein are free from patent infringement or from any third-party right. Photobit assumes no obligation to correct any errors contained herein or to advise any user of this text of any correction, if such be made. Photobit will not assume any liability for the accuracy or correctness of any engineering or software support or assistance provided to a user.

Photobit products are not intended for use in medical radiography or life support appliances, devices, or systems. Use of a Photobit product in such applications without the written consent of Photobit is prohibited.

Written and designed at Photobit Corporation, 135 North Los Robles Avenue, 7th Floor, Pasadena, California 91101, U.S.A.
Telephone (626) 683-2200. Fax (626) 683-2220. WWW.PHOTOBIT.COM

Printed in the United States of America.

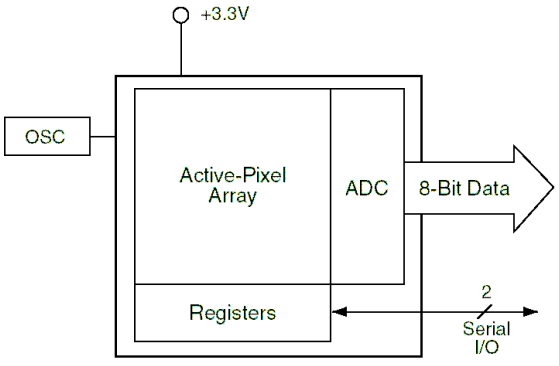
Photobit®
Behind Every Great Digital Image™

PB-0100 / PB-0101
1/5-Inch CMOS Active-Pixel Digital Image Sensors

March 2000 (Version 3.0)

Product Specification

Contents



1.0 Introduction

- Digital 'camera-on-a-chip'
- 360H x 296V resolution
- 7.9-µm pixels in a 1/5-inch optical format
- On-chip control logic
- On-chip analog-to-digital converter (ADC)
- Simple digital interface and control
- Default or user-programmable modes
- 3.3V operation
- Power consumption of <100 mW
- Color and monochrome versions
- Master clock speed of 24 MHz

1.1 Features

The PB-0100 and PB-0101 are 1/5-inch CMOS active-pixel digital image sensors, available in monochrome or color. They perform sophisticated camera functions on-chip, consume little power, and are programmable through a simple two-wire I²C interface. The image format is CIF (352H x 288V), with four extra boundary pixels along each edge, for an optical array format of 360H x 296V. Eight optically opaque pixel rows that adjust black level bring the total pixel count to 109,440, or 360H x 304V.

The sensors can be operated in default mode or programmed by the user for frame size, exposure, and other parameters. Default mode produces a CIF-size image at 30 frames per second, with on-chip auto-exposure enabled. An on-chip 8-bit analog-to-digital converter (ADC) provides one digital byte per pixel. The output format is nibble-wide in the 28-pin package **(PB-0100)** and either nibble- or byte-wide in the 44-pin package **(PB-0101*)**. Frame- and line-valid signals are encoded into the data stream and are output on dedicated pins, along with a pixel clock that is synchronous with valid data.

*PRODUCT NUMBERS: *Reference is made throughout to the PB-0100; the two sensors are identical, except for packaging.*

1.2 Top-Level Specification

Array Format	Total: 360H x 304V (109,440 pixels) Optical: 360H x 296V (106,560 pixels) CIF ref.: 352H x 288V (101,376 pixels)
Pixel Size and Type	7.9 µm x 7.9 µm active-pixel photodiode
Optical Format	1/5-inch
Frame Rate	0–33 frames per second
Maximum Data Rate	6 megabytes per second (master clock 24 MHz)
Power	100 mW at maximum data rate
Digital SNR @ 1 lux	>20 dB (10:1) for green pixels, faceplate illuminance at 30 Hz
Responsivity	for Green pixels from "Illuminant A" light source, passed through an infrared cut-off filter $\lambda_{0.5}$=[400÷710]nm Typical: 3.5 Vpix/µJ/cm^2 (corresponds to 1.7 Vpix/lux-sec)
Internal Intra-Scene Dynamic Range	64 dB
Supply Voltage	+3.3V
Supply Current	30 mA (nominal)
Operating Temperature	-5°C to +70°C
Storage Temperature	-40°C to +125°C
Output	8-bit color (SRGB) or monochrome digital video
Shutter	Electronic rolling snap (ERS)
Correlated Double Sampling	On-chip
Color Filter Array	Bayer: Pattern 2G
Color Channel Programmable Gain Range	1-32 (8-bit resolution)
Peak Quantum Efficiency (RGB)	19%, 17%, 13%
ADC	On-chip 8-bit serial
Auto-Exposure	On-chip, with manual override
Package	28- or 44-pin CLCC
Timing and Control	On-chip
Programmable Controls	• Window size and location • Signal gain • Exposure parameters • Auto-exposure parameters • ADC reference • Frame rate • DAC biases

2.0 Electrical

The chip layout consists of five (5) main blocks: the digital logic block, which takes up the left portion of the chip; the pixel array, in the top right corner; the column-parallel gain and readout circuitry, below the pixel array; the 8-bit flash ADC, in the bottom center of the chip; and the biasing DACs, along the right side.

The digital I/O pins take up the left half of the top side, and all of the left and bottom sides of the die. The analog I/O pins are on the right side and the right half of the top side of the die. All of the analog biases are generated on-chip; the analog pins are bonded out principally for de-coupling and testing.

Power is applied to the PB-0100 through three (3) sources. VDD and DGND are the digital power supply and ground pins. VAA and AGND are the analog power supply and ground pins. VAA_PIX supplies analog power to the sensor array, and is referenced to AGND. VDD, VAA, and VAA_PIX are electrically isolated from each other. Although DGND and AGND are never directly connected with a metal trace on-chip, they are connected through the substrate of the die. Thus, care should be taken to avoid a voltage drop from developing across these two ground pins, which would lead to large substrate currents and potential latch-up problems.

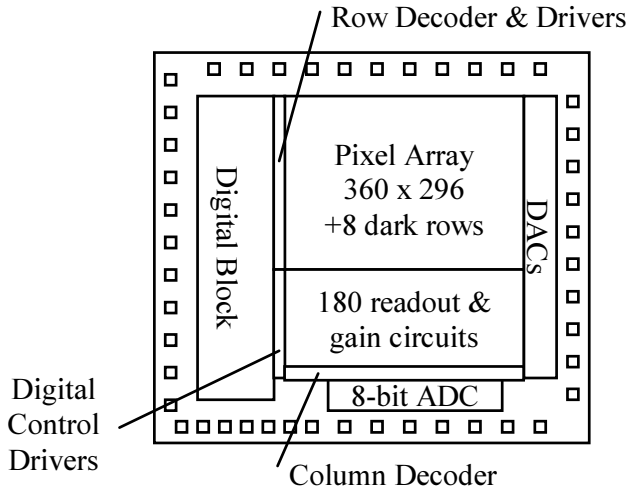
Digital inputs to the chip are as follows: CLK_IN is the input master clock (nominally 24 MHz); RESET_BAR is an active-low reset pin; STANDBY is, by default, an active high signal that powers-down most of the analog circuitry (and it can be changed to an active low signal by clearing bit 2 of register 39); SADDR selects the I^2C address of the PB-0100 and changes the default data output mode (described below); SCLK is the I^2C clock pin input; and SDATA is the I^2C data pin. The only two output states of the SDATA pin are 'pulled down' and 'high-impedance.' An external pull-up resistor is required, as per standard I^2C design.

Digital outputs from the chip are as follows: CLK_OUT is a buffered copy of the master clock; FRAME_VALID is an active high signal that surrounds each image frame output from the chip (during vertical blanking FRAME_VALID is low); LINE_VALID is an active high signal that is on when valid pixel data is being output on the data lines (during horizontal and vertical blanking LINE_VALID is low); PIXCLK is the pixel clock output (one pixel is output during each pixel clock period when LINE_VALID is high, and PIXCLK is always running, even during blanking periods); and DOUTLSB and DOUT0 through DOUT7 are the data lines (DOUTLSB is reserved for a future 10-bit ADC and is currently tied to DGND, while DOUT0 through DOUT7 output the 8-bit pixel data).

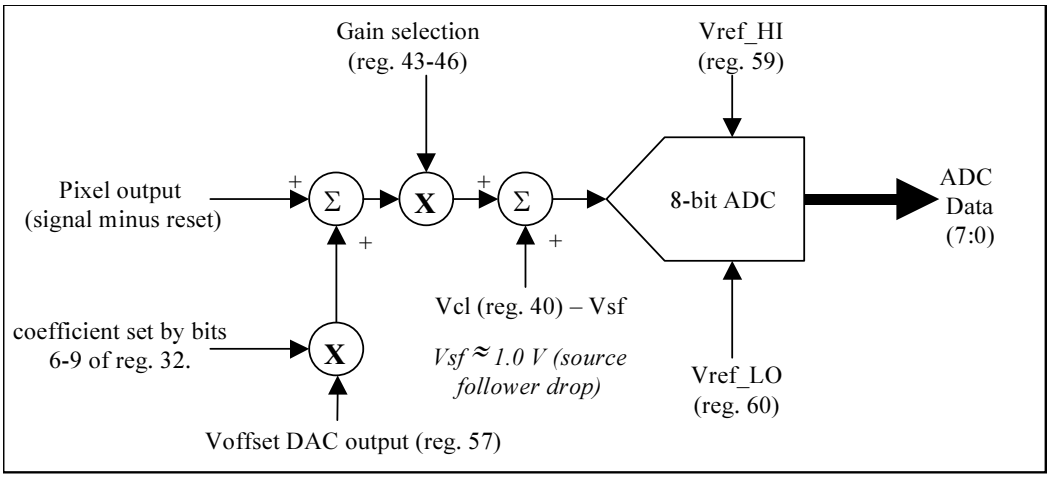
When the data output mode is in byte mode, the 8-bit data is valid for an entire PIXCLK period. When the data output mode is in nibble mode, the 8-bit data is multiplexed onto DOUT4 through DOUT7. While PIXCLK is high, the top nibble is output on DOUT4 through DOUT7, and when PIXCLK is low, the bottom nibble is output on DOUT4 through DOUT7. This mode allows only four (4) data lines to be bonded out, thus reducing the pin count and package size.

The analog input VADC_TEST_IN is used for testing. The analog outputs are VLN_FLASH, VLN_INT, DAC_TEST, VLN, VLP, VREF_HI, VREF_LO, and VCL. These are all generated on-chip and can be left disconnected or connected to de-coupling capacitors. Not all of these pins will be bonded out in all packages. Applications that require external control of the ADC references (i.e., VREF_HI and VREF_LO) can override the on-chip DACs by forcing these pins and setting bit 1 of register 39.

2.1 Functional Block Diagram



2.2 Signal Path



Signal Path

Offset Coefficient Selection
(from Register 32)

Bit 2	Bit 9	Bit 8	Bit 7	Bit 6	Relative Offset Coefficient
0	X	X	X	X	0
1	0	0	0	0	0
1	0	0	0	1	+1
1	0	0	1	0	+2
1	0	0	1	1	+3
1	0	1	0	0	-1
1	0	1	0	1	0
1	0	1	1	0	+1
1	0	1	1	1	+2
1	1	0	0	0	-2
1	1	0	0	1	-1
1	1	0	1	0	0
1	1	0	1	1	+1
1	1	1	0	0	-3
1	1	1	0	1	-2
1	1	1	1	0	-1
1	1	1	1	1	0

Actual offset coefficient is the relative offset coefficient multiplied by a constant attenuation factor.

Byte/Nibble Mode Selection

SADDR	Bit 13 of Reg. 7	I^2C Address (Read/Write)	Data Output Mode
0 V	0	0x93/0x92	Byte
0 V	1	0x93/0x92	Nibble
3.3 V	0	0xBB/0xBA	Nibble
3.3 V	1	0xBB/0xBA	Byte

Nibble mode is required to capture all 8 bits of pixel data for the 28-pin CLCC package, as only 4 data lines are bonded out to pins. If an I^2C address of 0x93/0x92 is desired with the 28-pin CLCC package, then after reset the host system must write a 1 to bit 13 of Register 7 to put the chip into nibble data output mode.

Standby Mode Selection

Standby Pin	Bit 2 of Reg 39	Analog Circuitry
0 V	0	Standby
0 V	1	Active
3.3 V	0	Active
3.3 V	1	Standby

Note that the default of bit 2 of Register 39 is 1, making Standby an active high signal by default.

2.3 I²C Description

Registers are written to and read from the PB-0100 through the I²C bus. The PB-0100 is an I²C slave. The PB-0100 is controlled by the I²C clock (SCLK), which is driven by the I²C master. Data is transferred into and out of the PB-0100 through the I²C data (SDATA) line. The SDATA line is pulled up to 3.3V off-chip by a 1.5Kohm resistor. Either the slave or master device can pull the SDATA line down; the I²C protocol determines which device is allowed to pull the SDATA line down at any given time.

Protocol
The I²C bus defines several different transmission codes, as follows:

- a start bit
- the slave device 8-bit address
- an (no) acknowledge bit
- an 8-bit message
- a stop bit

Sequence
A typical read or write sequence begins by the master sending a start bit. After the start bit, the master sends the slave device's 8-bit address. The last bit of the address determines if the request will be a read or a write, where a '0' indicates a write and a '1' indicates a read. The slave device acknowledges its address by sending an acknowledge bit back to the master.

If the request was a write, the master then transfers the 8-bit register address to which a write should take place. The slave sends an acknowledge bit to indicate that the register address has been received. The master then transfers the data 8 bits at a time, with the slave sending an acknowledge bit after each 8 bits. The PB-0100 uses 16-bit data for its internal registers, thus requiring two 8-bit transfers to write to one register. After 16 bits are transferred, the register address is automatically incremented, so that the next 16 bits are written to the next register address. The master stops writing by sending a start or stop bit.

A typical read sequence is executed as follows. First the master sends the write-mode slave address and 8-bit register address just as in the write request. The master then sends a start bit and the read-mode slave address. The master then clocks out the register data 8 bits at a time. The master sends an acknowledge bit after each 8-bit transfer. The register address is auto-incremented after every 16 bits is transferred. The data transfer is stopped when the master sends a no-acknowledge bit.

Bus Idle State
The bus is idle when both the data and clock lines are HIGH. Control of the bus is initiated with a Start bit, and the bus is released with a Stop bit. Only the master can generate the start and stop bits.

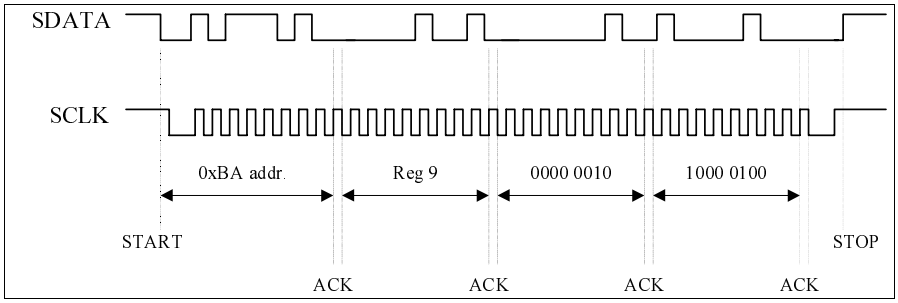
Start Bit and Stop Bit
The start bit is defined as a HIGH to LOW transition of the data line while the clock line is HIGH. The stop bit is defined as a LOW to HIGH transition of the data line while the clock line is HIGH.

Slave Address
The 8-bit address of an I²C device consists of 7 bits of address and 1 bit of direction. A '0' in the LSB of the address indicates write-mode, and a '1' indicates read-mode.

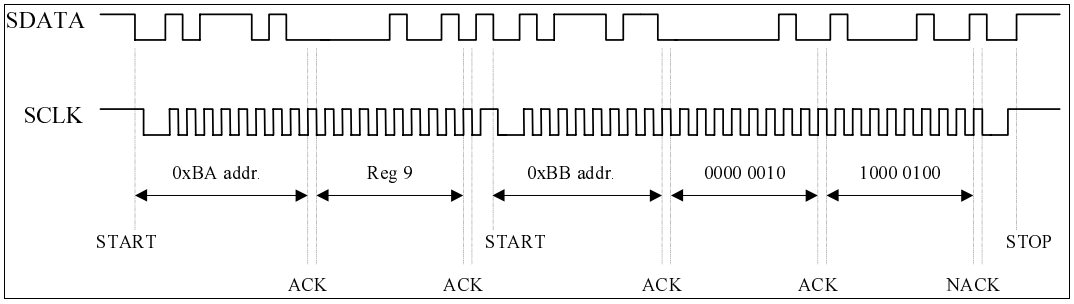
Data Bit Transfer
One data bit is transferred during each clock pulse. The I²C clock pulse is provided by the master. The data must be stable during the HIGH period of the I²C clock . It can change only when the I²C clock is LOW. Data is transferred 8 bits at a time, followed by an acknowledge bit.

Acknowledge and No-Acknowledge Bit
The master generates the acknowledge clock pulse. The transmitter (which is the master when writing, or the slave when reading) releases the data line, and the receiver indicates an acknowledge bit by pulling the data line low during the acknowledge clock pulse. The no-acknowledge bit is generated when the data line is not pulled down by the receiver during the acknowledge clock pulse. A no-acknowledge bit is used to terminate a read sequence.

2.3 I²C Description (continued)



Timing Diagram Showing a Write to I²C Register 9 (integration time/row unit count) with the value 644. PB-0100 drives the SDATA line low during the acknowledge clock pulses (ACK).



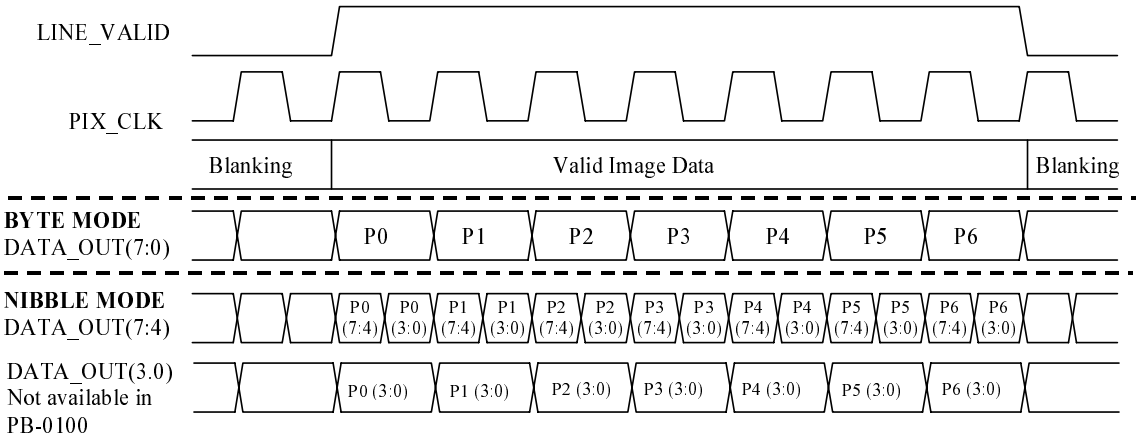
Timing Diagram Showing a Read from I²C Register 9 (integration time/row unit count), which returns the value of 644. PB-0100 drives the SDATA line low during the first three acknowledge clock pulses (ACK). SDATA is driven low by the master during the fourth acknowledgement clock pulse. The fifth acknowledgement clock pulse is a no-acknowledge (NACK) from the master (SDATA is not driven low).

2.4 Pin Descriptions

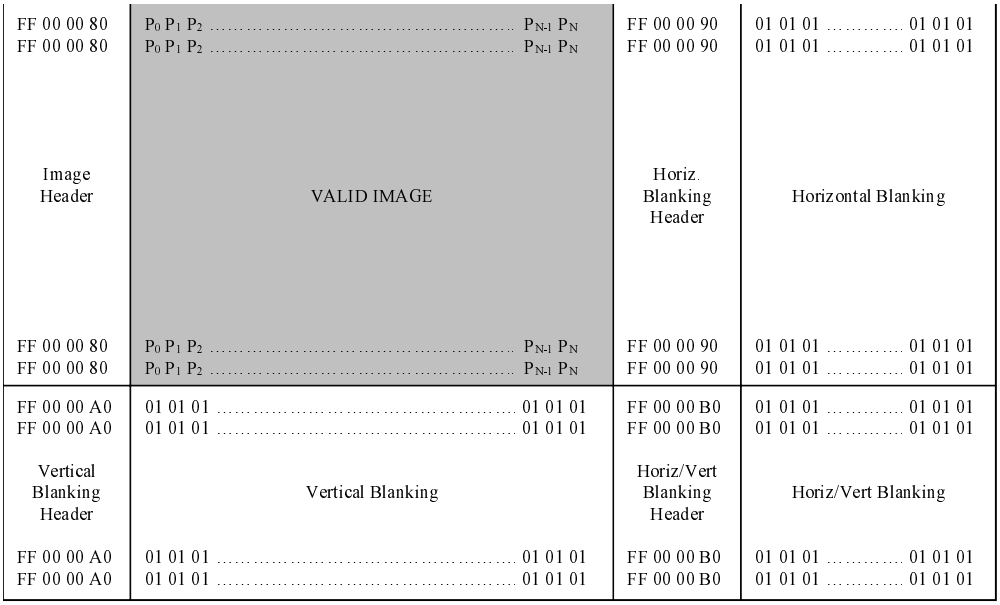
NAME	I/O	DESCRIPTION	PB-0100 28-Pin CLCC	PB-0101 44-Pin CLCC
VAA	Power	3.3V analog power supply	14, 17	1, 5
AGND	Power	Analog ground	15, 18	2, 6
VLN	Output	Bias voltage		3
VREF_HI	Output	ADC Top reference	16	4
VLP	Output	Bias voltage		7
DAC_TEST	Output	DAC test output	19	8
VLN_INT	Output	Bias voltage		9
VLN_FLASH	Output	Bias voltage		10
VAA_PIX	Power	3.3V Pixel power supply	20	11
VADC_TEST_IN	Input	Test input voltage to ADC	21	12
NC1		Leave unconnected		13
LINE_VALID	Output	Active high when image data on data output bus	22	14
SDATA	BiDir	I2C data	23	15
SCLK	Input	I2C clock	24	16
PIXCLK	Output	Pixel clock - continuously running (except during reset)	25	17
CLK_OUT	Output	Buffered copy of master clock		18
CLK_IN	Input	Master clock, 24 MHz	26	19
DGND	Power	Digital ground	6, 27	20, 26, 34, 40
VDD	Power	3.3V Digital power supply	7, 28	21, 27, 35, 41
DOUT4	Output	Data output. In nibble mode, D4 when PIXCLK=1, D0 when PIXCLK=0	1	22
DOUT5	Output	Data output. In nibble mode, D5 when PIXCLK=1, D1 when PIXCLK=0	2	23
DOUT6	Output	Data output. In nibble mode, D6 when PIXCLK=1, D2 when PIXCLK=0	3	24
NC2		Leave unconnected	8	25
DOUT7	Output	Data output. In nibble mode, D7 when PIXCLK=1, D3 when PIXCLK=0	4	28
DOUTLSB	Output	Always 0 (for future 10-bit image sensors)	5	29
DOUT0	Output	Data output.		30
DOUT1	Output	Data output.		31
DOUT2	Output	Data output.		32
DOUT3	Output	Data output.		33
RESET_BAR	Input	Active low asynchronous reset, returns sensor to default setup.	8	36
FRAME_VALID	Output	Active high during entire image frame processing	9	37
STANDBY	Input	When 3.3V, turns off analog bias circuitry for power saving mode. Can be made active low by programming bit 2 of Reg. 39.	10	38
SADDR	Input	Hardwired device address pin for I2C. SADDR = 3.3V: write ADDR. = 0xBA, read ADDR. = 0xBB SADDR = 0V: write ADDR. = 0x92, read ADDR. = 0x93 SADDR = 3.3V defaults to nibble wide output mode SADDR = 0V defaults to byte wide output mode	11	39
NC4		Unconnected		42
VREF_LO	Output	ADC Bottom reference	12	43
VCL	Output	Clamp voltage	13	44

2.5 Output Format and Timing

The data output of the PB-0100 is synchronized with the PIX_CLK output. When LINE_VALID is high, one 8-bit pixel datum is output every PIX_CLK period, where the PIX_CLK period is between rising edges. In nibble mode, the top 4 bits are output while PIX_CLK is high, and the bottom 4 bits are output while PIX_CLK is low.

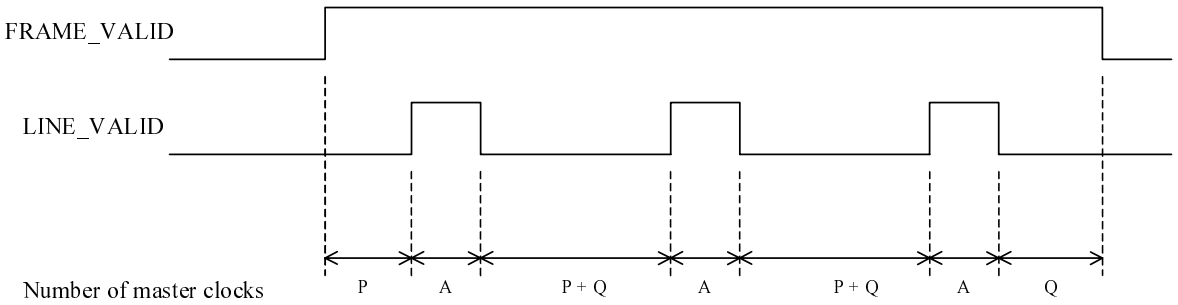


Timing Example of 7 Pixel Row Size
Pixel data is P0 through P6.



Spatial Illustration of Image Readout
LINE_VALID is high during the shaded region of the figure.

2.5 Output Format and Timing (continued)



Row Timing and FRAME_VALID/LINE_VALID Signals

Effect of Register 10 on timing. All quantities are in number of master clock cycles.

Speed	Bits 5-4	A	Q
Nominal rate	10	4 x (Reg. 4 + 1)	4 x (Reg. 5 - 3) + 3
2/3 rate	01	6 x (Reg. 4 + 1)	6 x (Reg. 5 - 3) + 3
1/2 rate	00	8 x (Reg. 4 + 1)	8 x (Reg. 5 - 3) + 3

Bits 3-2	Bits 1-0	P (Nominal Rate)	P (2/3 Rate)	P (1/2 Rate)
00	00	3977	3987	3997
00	01	3473	3483	3493
00	10	3217	3227	3237
00	11	3089	3099	3109
01	00	2509	2523	2533
01	01	2005	2019	2029
01	10	1749	1763	1773
01	11	1621	1635	1645
10	00	1781	1791	1805
10	01	1277	1287	1301
10	10	1021	1031	1045
10	11	893	903	917
11	00	1413	1425	1437
11	01	909	921	933
11	10	653	665	677
11	11	525	537	549

2.6 Registers

2.6.1 Register Start-Up Sequence

This section assumes the PB-0100 is powered at 3.3V with a 24 MHz master clock.

Upon powering up the PB-0100, the sensor should be reset by bringing the RESET_BAR pin low for at least 200 nsec. This will initialize all of the registers to their default values. Upon the release of reset, the sensor will begin pixel integration, and the first row of pixel data will be output 8.3 msec later. The default frame size is CIF (352x288 pixels), with a frame rate of approximately 30 fps. The pixel data is output at 6 Mpixel/sec. (master clock / 4) data output. A new row of pixel data is output every 104 µsec. Actual pixel data is output for 58.7 µsec (56.4%) of the 104 µsec row time, during which time LINE_VALID is high. The remaining 45.3 µsec (43.6%) of the 104 µsec row time is horizontal blanking time, during which time LINE_VALID is low. After all 288 active image rows have been output, the sensor will output 35 lines (3.64 msec) of vertical blanking. FRAME_VALID goes low during the vertical blanking time to indicate the end of the current frame and the beginning of the next frame.

By default, the sensor has the internal auto-exposure enabled. The following register programming sequence is suggested after reset to produce high quality images.

Programming	Explanation
R60 (VREF_LO) set to 3 decimal (3 hex)	Sets the low reference of the ADC to produce a good black level.
R32 (Pixel Read Control Mode) set to 5120 decimal (1400 hex)	Enable Global Gain changes through R53.
R52 (Minimum Gain) set to 16 decimal (10 hex)	Set the minimum gain used by the auto-exposure to 16 (2.0 analog) to avoid pixel saturation.
R53 (Global Gain) set to 16 decimal (10 hex)	Set the gain to 16 (2.0 analog) to avoid pixel saturation.
R14 (Exposure Gain Command) set to 17 decimal (11 hex)	Allow auto-exposure to change the gain.
R23 (Update Interval) set to 2 decimal (2 hex)	Speed up the auto-exposure routine.
R5 (Column Fill-In) set to 14 decimal (E hex)	Set frame rate to 30.01 fps (default is 29.77 fps).

2.6.2 Register Programming Reference

This section groups registers according to functionality.

Reset
R13. This register is used to reset the sensor to its default, power-up state. To reset the PB-0100, first write a 1 into bit 0 of this register to put the PB-0100 in reset mode, then write a 0 into bit 0 to resume operation.

Window Location and Size
R1, R2, R3, R4. These registers control the location and size of the active imaging window. Only pixels within the active imaging window are read-out. The default size is CIF (352 x 288) pixels, with the top right corner at pixel (4,12) and the bottom left corner at pixel (355, 299).

Pixel Integration Control
R8, R9. These two registers control the integration time of the pixels. R8 is the number of frames of integration time, and R9 is the number of rows of integration time. The actual total integration time, Tint, is:

$$Tint = [(R8 * R15) + R9] * Trow$$

where Trow is the processing time for one pixel row. R15 sets the number of rows in a frame, and is described in the auto-exposure section. Typically, R8 is set to 0, and the maximum value of R9 is limited to the number of rows per frame (which includes vertical blanking rows), such that the frame rate is unaffected by the integration time. An additional constraint is that Tint must be adjusted to avoid banding in the image from light flicker. Under 60 Hz flicker, this means Tint must be a multiple of 1/120 of a second. Under 50 Hz flicker, Tint must be a multiple of 1/100 of a second.

Frame Rate Control
R5, R6, R10. These registers control the blanking time in a row (called column fill-in or horizontal blanking) and between frames (vertical blanking). This allows the frame rate to be adjusted when other imager parameters change.

For example, if the active image size is reduced in the x-dimension through R4, the processing time for one pixel row gets shorter, leading to an increase in the frame rate. To keep the same frame rate, R5 can be programmed with the difference between the old and new values of R4. This adds blanking time equivalent to the time used for the previously read-out pixels, maintaining the total row time and thus the frame rate.

Similarly, if the active image size is reduced in the y-dimension through R3, the number of rows in the frame is reduced, also leading to an increase in the frame rate. This can be compensated for with R6, which controls the addition of blank rows at the end of every frame.

Note that R5 is only one component of the horizontal blanking time. The other two components of the horizontal blanking (the pixel read time and the pixel gain time) are fixed by R10. Please see the row timing section for detailed timing information on R10. The default/power-up mode has a horizontal blanking time of 43.6% of the total row time.

Gain Settings
R43, R44, R45, R46, R53. These registers control the electrical gain applied to the pixel signal after read-out. The gain is programmed in steps of 0.125, or $1/8^{th}$, i.e. a programmed gain value of 8 corresponds to an electrical gain of 1, and a programmed gain value of 255 corresponds to an electrical gain of 31.875. The gain is individually controllable for each color in the Bayer pattern. R53 can be used to set all four gains at once, if bit 10 of R32 is on (enable global gain setting).

ADC Reference Settings
R59, R60. These two registers control the top and bottom reference levels for the ADC. R60 sets the black level of the image. If the image is washed out (all blacks are gray) then R60 should be increased. If the image is too black (dark gray is black), the R60 should be decreased. R60 is typically between 1 and 6.

R59 can be used to set the white level of the image. Smaller values of R59 lead to whiter images, and larger values of R59 lead to darker images. R59 is typically between 11 and 16. Note that other ways to brighten the image are by increasing the integration time and by changing the gain.

Auto-Exposure Settings
R14, R15, R16, R17, R18, R19, R20, R21, R22, R23, R24, R25, R26, R27, R28, R51, R52, R54, R55. Please see the auto-exposure section concerning the use of these registers.

Imager Mode Controls
R7, R32. These two registers control the CMOS image sensor's operating modes.

Bias Settings
R33, R34, R35, R36, R37, R38, R39, R40, R41, R57. These registers control the bias settings, which should not require any modification during normal operation.

2.6.3 Register Programming Examples

This section contains programming examples for different frame rates.

~30 fps CIF Default. Default values produce slightly less than 30 fps, which may result in banding in the image when used with 60 Hz illumination. For 30.009 fps, change Register 5 to 14.

Parameter	Value	Result	Value
CLK Clock Freq. (MHz)	24	Clocks per PIXCLK	4
Reg. 1 Row Window Start	12	Active Data Time	58.667 µsec
Reg. 2 Column Window Start	4	+ Horizontal Blank Time	45.333 µsec
Reg. 3 Row Window Size	287	= Total Row Time	104 µsec
Reg. 4 Column Window Size	351	Vertical Blank Time	3640 µsec
Reg. 5 Column Fill In	19	Pixel Integration Time	33.488 msec
Reg. 6 Vertical Blank Count	34	Frame Rate	29.769 fps
Reg. 8 Int. Time Frame Count	0		
Reg. 9 Int. Time Row Count	322		
Reg. 10 Row Speed Control	42		

30 fps, 1 Row Vertical Blanking, CIF + 4 Extra Rows and Columns on Each Side for Color Correction. If using auto-exposure, Registers 15, 16 and 17 should be set to 296, 148, and 74 respectively.

Parameter	Value	Result	Value
CLK Clock Freq. (MHz)	24	Clocks per PIXCLK	4
Reg. 1 Row Window Start	8	Active Data Time	60.000 µsec
Reg. 2 Column Window Start	0	+ Horizontal Blank Time	52.167 µsec
Reg. 3 Row Window Size	295	= Total Row Time	112.167 µsec
Reg. 4 Column Window Size	359	Vertical Blank Time	112.167 µsec
Reg. 5 Column Fill In	60	Pixel Integration Time	33.201 msec
Reg. 6 Vertical Blank Count	0	Frame Rate	30.018 fps
Reg. 8 Int. Time Frame Count	0		
Reg. 9 Int. Time Row Count	296		
Reg. 10 Row Speed Control	42		

2.6.3 Register Programming Examples (continued)

60 fps, 1 Row Vertical Blanking, QCIF Window in Center of Array. If using auto-exposure, Registers 15, 16 and 17 should be set to 144, 72, and 36 respectively.

Parameter	Value	Result	Value
CLK Clock Freq. (MHz)	24	Clocks per PIXCLK	4
Reg. 1 Row Window Start	82	Active Data Time	29.333 µsec
Reg. 2 Column Window Start	90	+ Horizontal Blank Time	85.5 µsec
Reg. 3 Row Window Size	143	= Total Row Time	114.833 µsec
Reg. 4 Column Window Size	175	Vertical Blank Time	114.833 µsec
Reg. 5 Column Fill In	260	Pixel Integration Time	16.651 msec
Reg. 6 Vertical Blank Count	0	Frame Rate	60.057 fps
Reg. 8 Int. Time Frame Count	0		
Reg. 9 Int. Time Row Count	144		
Reg. 10 Row Speed Control	42		

25 fps, 1 Row Vertical Blanking, CIF + 4 Extra Rows and Columns on Each Side for Color Correction. If using auto-exposure, Registers 15, 16 and 17 should be set to 296, 148, and 74 respectively.

Parameter	Value	Result	Value
CLK Clock Freq. (MHz)	24	Clocks per PIXCLK	4
Reg. 1 Row Window Start	8	Active Data Time	60.000 µsec
Reg. 2 Column Window Start	0	+ Horizontal Blank Time	74.667 µsec
Reg. 3 Row Window Size	295	= Total Row Time	134.667 µsec
Reg. 4 Column Window Size	359	Vertical Blank Time	134.667 µsec
Reg. 5 Column Fill In	195	Pixel Integration Time	39.861 msec
Reg. 6 Vertical Blank Count	0	Frame Rate	25.003 fps
Reg. 8 Int. Time Frame Count	0		
Reg. 9 Int. Time Row Count	296		
Reg. 10 Row Speed Control	42		

2.6.3 Register Programming Examples (continued)

15 fps, 3 MHz Pixel Output, 1 Row Vertical Blanking, CIF + Extra 4 Rows and Columns on Each Side. If using auto-exposure, Registers 15, 16 and 17 should be set to 296, 148, and 74 respectively.

Parameter	Value	Result	Value
CLK Clock Freq. (MHz)	24	Clocks per PIXCLK	8
Reg. 1 Row Window Start	8	Active Data Time	120.000 µsec
Reg. 2 Column Window Start	0	+ Horizontal Blank Time	104.333 µsec
Reg. 3 Row Window Size	295	= Total Row Time	224.333 µsec
Reg. 4 Column Window Size	359	Vertical Blank Time	224.333 µsec
Reg. 5 Column Fill In	185	Pixel Integration Time	66.403 msec
Reg. 6 Vertical Blank Count	0	Frame Rate	15.009 fps
Reg. 8 Int. Time Frame Count	0		
Reg. 9 Int. Time Row Count	296		
Reg. 10 Row Speed Control	10		

12.5 fps, 3 MHz Pixel Output, 1 Row Vertical Blanking, CIF + Extra 4 Rows and Columns on Each Side. If using auto-exposure, Registers 15, 16 and 17 should be set to 296, 148, and 74 respectively.

Parameter	Value	Result	Value
CLK Clock Freq. (MHz)	24	Clocks per PIXCLK	8
Reg. 1 Row Window Start	8	Active Data Time	120.000 µsec
Reg. 2 Column Window Start	0	+ Horizontal Blank Time	149.333 µsec
Reg. 3 Row Window Size	295	= Total Row Time	269.333 µsec
Reg. 4 Column Window Size	359	Vertical Blank Time	269.333 µsec
Reg. 5 Column Fill In	320	Pixel Integration Time	12.501 msec
Reg. 6 Vertical Blank Count	0	Frame Rate	12.501 fps
Reg. 8 Int. Time Frame Count	0		
Reg. 9 Int. Time Row Count	296		
Reg. 10 Row Speed Control	10		

2.6.4 Complete Register Descriptions

This section contains the complete lists of user registers.

Register Address	Register Name	Function	Read/Write Control
00 hex (0 decimal)	R0	Chip Version	R

Default Contents = 6403 hex, 25603 decimal:

bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0	1	1	0	0	1	0	0	0	0	0	0	0	0	1	1

Description:
Version 0.3 of PB-0100 timing engine. Read-only register. (16 bits)

Notes:
The bottom byte of this register (currently 3) may change to reflect the version number of future releases of the PB-0100. The top byte will always be 64 hex (100 dec) to uniquely identify the PB-0100.

Limits:
Minimum = N/A
Maximum = N/A

2.6.4 Complete Register Descriptions (continued)

Register Address	Register Name	Function	Read/Write Control
01 hex (1 decimal)	R1	Row Window Start	RW

Default Contents = 000C hex, 12 decimal:

bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
x	x	x	x	x	x	x	0	0	0	0	0	1	1	0	0

Description:
Row start address. Sets the first row of the active image window. Effect on image data output is delayed by one frame. (9 bits)

Limits:
Minimum = 0 (first row of array)
Maximum = 303 (last row of array)
Default = 12

2.6.4 Complete Register Descriptions (continued)

Register Address	Register Name	Function	Read/Write Control
02 hex (2 decimal)	R2	Column Window Start	RW

Default Contents = 0004 hex, 4 decimal:

bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
x	x	x	x	x	x	x	0	0	0	0	0	0	1	0	0

Description:
Column start address. Sets the first column of the active image window. Effect on image data output is delayed by one frame. (9 bits)

Limits:
Minimum = 0 (first column of array)
Maximum = 359 (last column of array)
Default = 4

2.6.4 Complete Register Descriptions (continued)

Register Address	Register Name	Function	Read/Write Control
03 hex (3 decimal)	R3	Row Window Size	RW

Default Contents = 011F hex, 287 decimal:

bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
x	x	x	x	x	x	x	1	0	0	0	1	1	1	1	1

Description:
Vertical window size in number of rows, minus 1. Effect on image data output is delayed by one frame. (9 bits)

Limits:
Minimum = 0
Maximum = 303
Default = 287

2.6.4 Complete Register Descriptions (continued)

Register Address	Register Name	Function	Read/Write Control
04 hex (4 decimal)	R4	Column Window Size	RW

Default Contents = 015F hex, 351 decimal:

bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
x	x	x	x	x	x	x	1	0	1	0	1	1	1	1	1

Description:
Horizontal window size in number of columns, minus 1. Effect on image data output is delayed by one frame. (9 bits)

Limits:
Minimum = 0
Maximum = 359
Default = 351

2.6.4 Complete Register Descriptions (continued)

Register Address	Register Name	Function	Read/Write Control
05 hex (5 decimal)	R5	Column Fill-In	RW

Default Contents = 0013 hex, 19 decimal:

bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
x	x	x	x	x	x	x	0	0	0	0	1	0	0	1	1

Description:
Horizontal blanking time, programmed in terms of blank columns. To maintain a constant row time, the sum of Registers 4 and 5 should remain constant. Effect on image data output is delayed by one frame. (9 bits)

Limits:
Minimum = 0
Maximum = 511
Default = 19

2.6.4 Complete Register Descriptions (continued)

Register Address	Register Name	Function	Read/Write Control
06 hex (6 decimal)	R6	Vertical Blank Count	RW

Default Contents = 0022 hex, 34 decimal:

bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
x	x	x	x	0	0	0	0	0	0	1	0	0	0	1	0

Description:
Vertical blanking time, programmed in terms of row times, minus 1. Effect on image data output is delayed by one frame. (12 bits).

Limits:
Minimum = 0
Maximum = 4095
Default = 34

2.6.4 Complete Register Descriptions (continued)

Register Address	Register Name	Function	Read/Write Control
07 hex (7 decimal)	R7	Control Mode	RW

Default Contents = 002A hex, 42 decimal:

bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0	0	0	0	0	0	0	0	0	0	1	0	1	0	1	0

Description:
Sets imager mode settings.
Bits 15, 14 = Not used, set to 0.
Bit 13 = When set to 1, switches byte/nibble output mode default set by SADDR.
Bit 12 = Reserved.
Bits 11, 10, 9, 8 = Not used, set to 0.
Bit 7 = Disable CCIR digital format.
Bit 6 = Use test data from Reg. 50, if set.
Bit 5, 4 = Part code = 10, for PB-0100. (Read-only bits.)
Bit 3 = 1, photodiode pixels. (Read-only bit.)
Bit 2 = ADC test mode, if set.
Bit 1 = CE (chip enable), stops video output at end of current frame when set to 0.
Bit 0 = Reserved, set to 0.

Limits:
Minimum = N/A
Maximum = N/A

2.6.4 Complete Register Descriptions (continued)

Register Address	Register Name	Function	Read/Write Control
08 hex (8 decimal)	R8	Integration Time/ Frame Unit Count	RW

Default Contents = 0000 hex, 0 decimal:

bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
x	x	x	x	x	x	x	x	x	x	x	x	0	0	0	0

Description:
Number of frame times in integration time. This register allows the integration time to be programmed in multiples of the Expose0 shutter width, R15. Effect on image data output is delayed by one frame. (4 bits)

Limits:
Minimum = 0
Maximum = 15
Default = 0

Register Address	Register Name	Function	Read/Write Control
09 hex (9 decimal)	R9	Integration Time/ Row Unit Count	RW

Default Contents = 0050 hex, 80 decimal:

bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
x	x	0	0	0	0	0	0	0	1	0	1	0	0	0	0

Description:
Number of row times in integration time. Effect on output is delayed by one frame. Can exceed the window row size. Rows beyond the window row size (Reg. 3) + vertical blanking (Reg. 6) act as additional vertical blanking in the output. (14 bits)

Limits:
Minimum = 1
Maximum = 16,383
Default = 80

2.6.4 Complete Register Descriptions (continued)

Register Address	Register Name	Function	Read/Write Control
0A hex (10 decimal)	R10	Row Speed Control	RW

Default Contents = 002A hex, 42 decimal:

bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
x	x	x	x	x	x	x	x	0	0	1	0	1	0	1	0

Description:
Controls row-processing clock speed to adjust row time and frame rate. Three row-processing functions can be controlled individually: the data transfer speed, the gain processing speed and the row read speed. Effect on image data output is delayed by one frame. (8 bits)

Bits 7, 6 = Set to 0.
Bits 5, 4 = Data transfer speed.

11	reserved
10	nominal speed (6 MHz PIX_CLK)
01	two-thirds speed (4 MHz PIX_CLK)
00	half speed (3 MHz PIX_CLK)

Settings for data transfer speed

Bits 3, 2 = Gain processing speed.
Bits 1, 0 = Row read speed.

11	double speed
10	nominal speed
01	half speed
00	quarter speed

Settings for gain processing and row read speed

Limits:
Minimum = N/A
Maximum = N/A

2.6.4 Complete Register Descriptions (continued)

Register Address	Register Name	Function	Read/Write Control
0B hex (11 decimal)	R11	Abort Frame	RW

Default Contents = 0000 hex, 0 decimal:

bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	0

Description:
Restarts the shutter and read pointers immediately after the current row finishes. This bit is cleared when the restart has been initiated. Setting it causes the current frame to be abandoned, and a new frame becomes available after the programmed integration time elapses. (1 bit)

Limits:
Minimum = N/A
Maximum = N/A

2.6.4 Complete Register Descriptions (continued)

Register Address	Register Name	Function	Read/Write Control
0C hex (12 decimal)	R12	Reserved	R

Default Contents = 0000 hex, 0 decimal:

bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

Description:
Reserved.

Limits:
Minimum = N/A
Maximum = N/A

Register Address	Register Name	Function	Read/Write Control
0D hex (13 decimal)	R13	Reset	RW

Default Contents = 0000 hex, 0 decimal:

bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	0

Description:
Reset the control logic. Performs a hard reset, including loading all defaults, on all digital modules except the I^2C controller. Logic remains in reset until a 0 is written into this register. (1 bit)

Limits:
Minimum = N/A
Maximum = N/A

2.6.4 Complete Register Descriptions (continued)

Register Address	Register Name	Function	Read/Write Control
0E hex (14 decimal)	R14	Exposure Gain Command	RW

Default Contents = 0001 hex, 1 decimal:

bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
x	x	x	x	x	x	x	x	x	0	0	0	0	0	0	1

Description:
Auto-exposure control settings. Auto-exposure is enabled by default. (7 bits)
Bit 6 = Enable linear exposure change.
Bit 5 = Enable multiple frame (defined by Expose0, R15) integration times.
Bit 4 = Enable changing of Gain.
Bits 3, 2 = Not used.
Bit 1 = Hold current exposure setting.
Bit 0 = Enable auto-exposure.

Limits:
Minimum = N/A
Maximum = N/A

2.6.4 Complete Register Descriptions (continued)

Register Address	Register Name	Function	Read/Write Control
0F hex (15 decimal)	R15	Expose0	RW

Default Contents = 0142 hex, 322 decimal:

bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
x	x	x	x	x	x	x	1	0	1	0	0	0	0	1	0

Description:
Longest shutter width value for auto-exposure. Typically set for 1/30th (or 1/25th) of a second integration time, to avoid banding in the image due to 60 Hz (or 50 Hz) light flicker. (9 bits)

Notes:
This register defines the size of a frame in rows for R8 (Integration Time/Frame Unit Count). Typically this register should be set to the sum of R3 (Row Window Size) and R6 (Vertical Blank Count), plus one.

Limits:
Minimum = 1
Maximum = 511
Default = 322

2.6.4 Complete Register Descriptions (continued)

Register Address	Register Name	Function	Read/Write Control
10 hex (16 decimal)	R16	Expose1	RW

Default Contents = 00A1 hex, 161 decimal:

bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
x	x	x	x	x	x	x	0	1	0	1	0	0	0	0	1

Description:
Medium shutter width value for auto-exposure. Typically set for 1/60th (or 1/50th) of a second integration time, to avoid banding in the image due to 60 Hz (or 50 Hz) light flicker. (9 bits)

Limits:
Minimum = 1
Maximum = 511
Default = 161

2.6.4 Complete Register Descriptions (continued)

Register Address	Register Name	Function	Read/Write Control
11 hex (17 decimal)	R17	Expose2	RW

Default Contents = 0050 hex, 80 decimal:

bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
x	x	x	x	x	x	x	0	0	1	0	1	0	0	0	0

Description:
Shortest shutter width value for auto-exposure. Typically set for 1/120th (or 1/100th) of a second integration time, to avoid banding in the image due to 60 Hz (or 50 Hz) light flicker. (9 bits)

Limits:
Minimum = 1
Maximum = 511
Default = 80

2.6.4 Complete Register Descriptions (continued)

Register Address	Register Name	Function	Read/Write Control
12 hex (18 decimal)	R18	Low0_DAC	RW

Default Contents = 0008 hex, 8 decimal:

bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
x	x	x	x	x	x	x	x	x	x	x	0	1	0	0	0

Description:
Smallest ADC VREF_HI value allowed when using Expose0 shutter width. (5 bits)

Limits:
Minimum = 0
Maximum = 31
Default = 8

Register Address	Register Name	Function	Read/Write Control
13 hex (19 decimal)	R19	Low1_DAC	RW

Default Contents = 0008 hex, 8 decimal:

bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
x	x	x	x	x	x	x	x	x	x	x	0	1	0	0	0

Description:
Smallest ADC VREF_HI value allowed when using Expose1 shutter width. (5 bits)

Limits:
Minimum = 0
Maximum = 31
Default = 8

2.6.4 Complete Register Descriptions (continued)

Register Address	Register Name	Function	Read/Write Control
14 hex (20 decimal)	R20	Low2_DAC	RW

Default Contents = 0008 hex, 8 decimal:

bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
x	x	x	x	x	x	x	x	x	x	x	0	1	0	0	0

Description:
Smallest ADC VREF_HI value allowed when using Expose2 shutter width. (5 bits)

Limits:
Minimum = 0
Maximum = 31
Default = 8

2.6.4 Complete Register Descriptions (continued)

Register Address	Register Name	Function	Read/Write Control
15 hex (21 decimal)	R21	Threshold11	R* W

Default Contents = 01DC hex, 476 decimal:

bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
x	x	x	x	0	0	0	1	1	1	0	1	1	1	0	0

Description:
Bright pixel threshold for changing exposure/range setting. The threshold is the limit for the number of pixels with a "11" in the upper MSBs. Default is 476 pixels = 30% of samples from the default window size. (12 bits)

*Reads from this register return the actual count of "11xxxxxx" pixels in the image, instead of the programmed Threshold11 value.

Limits:
Minimum = 0
Maximum = 4095
Default = 476

2.6.4 Complete Register Descriptions (continued)

Register Address	Register Name	Function	Read/Write Control
16 hex (22 decimal)	R22	Threshold0x	R* W

Default Contents = 04A4 hex, 1188 decimal:

bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
x	x	x	x	0	1	0	0	1	0	1	0	0	1	0	0

Description:
Dark pixel threshold for changing exposure/range setting. The threshold is the limit for the number of pixels with a "0" in its MSB. Default is 1188 pixels = 75% of samples from the default window size. (12 bits).

*Reads from this register return the actual count of "0xxxxxxx" pixels in the image, instead of the programmed Threshold11 value.

Limits:
Minimum = 0
Maximum = 4095
Default = 1188

Register Address	Register Name	Function	Read/Write Control
17 hex (23 decimal)	R23	Update Interval	RW

Default Contents = 0008 hex, 8 decimal:

bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
x	x	x	x	x	x	x	x	x	x	0	0	1	0	0	0

Description:
Auto-exposure update interval, in number of frames. This register controls the speed of the auto-exposure routine. The auto-exposure will skip this number of frames before collecting statistics and attempting to adjust the brightness of the image. (6 bits)

Limits:
Minimum = 1
Maximum = 63
Default = 8

2.6.4 Complete Register Descriptions (continued)

Register Address	Register Name	Function	Read/Write Control
18 hex (24 decimal)	R24	High_DAC	RW

Default Contents = 0010 hex, 16 decimal:

bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
x	x	x	x	x	x	x	x	x	x	x	1	0	0	0	0

Description:
Largest ADC VREF_HI value allowed for any of the three shutter widths. (5 bits)

Limits:
Minimum = 0
Maximum = 31
Default = 16

2.6.4 Complete Register Descriptions (continued)

Register Address	Register Name	Function	Read/Write Control
19 hex (25 decimal)	R25	Trans0H	RW

Default Contents = 000C hex, 12 decimal:

bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
x	x	x	x	x	x	x	x	x	x	x	0	1	1	0	0

Description:
ADC VREF_HI new setting for a transition from the Expose1 to the Expose0 setting. (5 bits)

Limits:
Minimum = 0
Maximum = 31
Default = 12

2.6.4 Complete Register Descriptions (continued)

Register Address	Register Name	Function	Read/Write Control
1A hex (26 decimal)	R26	Trans1L	RW

Default Contents = 000C hex, 12 decimal:

bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
x	x	x	x	x	x	x	x	x	x	x	0	1	1	0	0

Description:
ADC VREF_HI new setting for a transition from the Expose0 to the Expose1 setting. (5 bits)

Limits:
Minimum = 0
Maximum = 31
Default = 12

2.6.4 Complete Register Descriptions (continued)

Register Address	Register Name	Function	Read/Write Control
1B hex (27 decimal)	R27	Trans1H	RW

Default Contents = 000C hex, 12 decimal:

bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
x	x	x	x	x	x	x	x	x	x	x	0	1	1	0	0

Description:
ADC VREF_HI new setting for a transition from the Expose2 to the Expose1 setting. (5 bits)

Limits:
Minimum = 0
Maximum = 31
Default = 12

2.6.4 Complete Register Descriptions (continued)

Register Address	Register Name	Function	Read/Write Control
1C hex (28 decimal)	R28	Trans2L	RW

Default Contents = 000C hex, 12 decimal:

bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
x	x	x	x	x	x	x	x	x	x	x	0	1	1	0	0

Description:
ADC VREF_HI new setting for a transition from the Expose1 to the Expose2 setting. (5 bits)

Limits:
Minimum = 0
Maximum = 31
Default = 12

Register Address	Register Name	Function	Read/Write Control
1D hex (29 decimal)	R29	Reserved	R

Default Contents = 0000 hex, 0 decimal:

bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

Description:
Reserved.

Limits:
Minimum = N/A
Maximum = N/A

2.6.4 Complete Register Descriptions (continued)

Register Address	Register Name	Function	Read/Write Control
1E hex (30 decimal)	R30	Reserved	R

Default Contents = 0000 hex, 0 decimal:

bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

Description:
Reserved.

Limits:
Minimum = N/A
Maximum = N/A

Register Address	Register Name	Function	Read/Write Control
1F hex (31 decimal)	R31	Wait to Read	RW

Default Contents = 0000 hex, 0 decimal:

bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	0

Description:
When set to 1, sensor pauses after the shutter is initialized to allow for externally controlled integration times. Data output starts when this bit is then cleared. (1 bit)

Limits:
Minimum = N/A
Maximum = N/A

2.6.4 Complete Register Descriptions (continued)

Register Address	Register Name	Function	Read/Write Control
20 hex (32 decimal)	R32	Pixel Read Control Mode	RW

Default Contents = 1000 hex, 4096 decimal:

bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0

Description:
Pixel read control mode. (15 bits)
Bit 15 = Reserved, set to 0.
Bit 14 = Reverse column output order. Mirrors image when set.
Bit 13 = Reserved, set to 0.
Bit 12 = Reserved, set to 1.
Bit 11 = Reserved, set to 0.
Bit 10 = Enable global Gain changes.
Bit 9 = Large offset switch initial.
Bit 8 = Small offset switch initial.
Bit 7 = Large offset switch final.
Bit 6 = Small offset switch final.
Bits 5, 4, 3 = Not used, set to 0.
Bit 2 = Enable input offset.
Bit 1 = Non-destructive read if 1.
Bit 0 = Reserved, set to 0.

Limits:
Minimum = N/A
Maximum = N/A

Register Address	Register Name	Function	Read/Write Control
21 hex (33 decimal)	R33	IREF_VLN	RW

Default Contents = 0020 hex, 32 decimal:

bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
x	x	x	x	x	x	0	0	0	0	1	0	0	0	0	0

Description:
Internal current reference. (10 bits)

Limits:
Minimum = N/A
Maximum = N/A

2.6.4 Complete Register Descriptions (continued)

Register Address	Register Name	Function	Read/Write Control
22 hex (34 decimal)	R34	IREF_VLP	RW

Default Contents = 0020 hex, 32 decimal:

bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
x	x	x	x	x	x	0	0	0	0	1	0	0	0	0	0

Description:
Internal current reference. (10 bits)

Limits:
Minimum = N/A
Maximum = N/A

Register Address	Register Name	Function	Read/Write Control
23 hex (35 decimal)	R35	IREF_VLN_INTEG	RW

Default Contents = 0320 hex, 800 decimal:

bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
x	x	x	x	x	x	1	1	0	0	1	0	0	0	0	0

Description:
Internal current reference. (10 bits)

Limits:
Minimum = N/A
Maximum = N/A

2.6.4 Complete Register Descriptions (continued)

Register Address	Register Name	Function	Read/Write Control
24 hex (36 decimal)	R36	IREF_MASTER	RW

Default Contents = 0020 hex, 32 decimal:

bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
x	x	x	x	x	x	0	0	0	0	1	0	0	0	0	0

Description:
Master current reference. (10 bits)

Limits:
Minimum = N/A
Maximum = N/A

2.6.4 Complete Register Descriptions (continued)

Register Address	Register Name	Function	Read/Write Control
25 hex (37 decimal)	R37	IDACP	RW

Default Contents = 0020 hex, 32 decimal:

bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
x	x	x	x	x	x	0	0	0	0	1	0	0	0	0	0

Description:
Internal current reference. (10 bits)

Limits:
Minimum = N/A
Maximum = N/A

2.6.4 Complete Register Descriptions (continued)

Register Address	Register Name	Function	Read/Write Control
26 hex (38 decimal)	R38	IDACN	RW

Default Contents = 0048 hex, 72 decimal:

bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
x	x	x	x	x	x	0	0	0	1	0	0	1	0	0	0

Description:
Internal current reference. (10 bits)

Limits:
Minimum = N/A
Maximum = N/A

Register Address	Register Name	Function	Read/Write Control
27 hex (39 decimal)	R39	DAC_Control_Reg	RW

Default Contents = 000C hex, 12 decimal:

bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
x	x	x	x	x	x	x	x	x	x	x	0	1	1	0	0

Description:
Bit 4 = Load power-up DAC defaults.
Bit 3 = Reserved, set to 1.
Bit 2 = Invert standby pin, active low/active high.
Bit 1 = Disable on-chip ADC reference.
Bit 0 = Reload DAC values from digital block.

Limits:
Minimum = N/A
Maximum = N/A

2.6.4 Complete Register Descriptions (continued)

Register Address	Register Name	Function	Read/Write Control
28 hex (40 decimal)	R40	VCL	RW

Default Contents = 002D hex, 45 decimal:

bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
x	x	x	x	x	x	x	x	x	x	1	0	1	1	0	1

Description:
Internal voltage reference. (6 bits)

Limits:
Minimum = 32
Maximum = 63

Register Address	Register Name	Function	Read/Write Control
29 hex (41 decimal)	R41	IREF_VLN_ADCIN	RW

Default Contents = 0320 hex, 800 decimal:

bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
x	x	x	x	x	x	1	1	0	0	1	0	0	0	0	0

Description:
Internal current reference. (10 bits)

Limits:
Minimum = N/A
Maximum = N/A

2.6.4 Complete Register Descriptions (continued)

Register Address	Register Name	Function	Read/Write Control
2A hex (42 decimal)	R42	Reserved	R

Default Contents = 0000 hex, 0 decimal:

bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

Description:
Reserved.

Limits:
Minimum = N/A
Maximum = N/A

Register Address	Register Name	Function	Read/Write Control
2B hex (43 decimal)	R43	Green 1 Gain	RW

Default Contents = 0008 hex, 8 decimal:

bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
x	x	x	x	x	x	x	x	0	0	0	0	1	0	0	0

Description:
Gain for even rows, even colums (GREEN1 pixels for color sensor). Gain is 0-31.875, in steps of 0.125. Effect on image data output is delayed by one frame. (8 bits)

Limits:
Minimum = 1
Maximum = 255
Default = 8

2.6.4 Complete Register Descriptions (continued)

Register Address	Register Name	Function	Read/Write Control
2C hex (44 decimal)	R44	Blue Gain	RW

Default Contents = 0008 hex, 8 decimal:

bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
x	x	x	x	x	x	x	x	0	0	0	0	1	0	0	0

Description:
Gain for odd rows, even columns (BLUE pixels for color sensor). Gain is 0-31.875, in steps of 0.125. Effect on image data output is delayed by one frame. (8 bits)

Limits:
Minimum = 1
Maximum = 255
Default = 8

2.6.4 Complete Register Descriptions (continued)

Register Address	Register Name	Function	Read/Write Control
2D hex (45 decimal)	R45	Red Gain	RW

Default Contents = 0008 hex, 8 decimal:

bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
x	x	x	x	x	x	x	x	0	0	0	0	1	0	0	0

Description:
Gain for even rows, odd columns (RED pixels for color sensor). Gain is 0-31.875, in steps of 0.125. Effect on image data output is delayed by one frame. (8 bits)

Limits:
Minimum = 1
Maximum = 255
Default = 8

2.6.4 Complete Register Descriptions (continued)

Register Address	Register Name	Function	Read/Write Control
2E hex (46 decimal)	R46	Green 2 Gain	RW

Default Contents = 0008 hex, 8 decimal:

bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
x	x	x	x	x	x	x	x	0	0	0	0	1	0	0	0

Description:
Gain for odd rows, odd columns (GREEN2 pixels for color sensor). Gain is 0-31.875, in steps of 0.125. Effect on image data output is delayed by one frame. (8 bits)

Limits:
Minimum = 1
Maximum = 255
Default = 8

Register Address	Register Name	Function	Read/Write Control
2F hex (47 decimal)	R47	Dark Row Address	RW

Default Contents = 0004 hex, 4 decimal:

bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
x	x	x	x	x	x	x	0	0	0	0	0	0	1	0	0

Description:
Address of the dark reference row. (9 bits)

Limits:
Minimum = 0
Maximum = 303
Default = 4

2.6.4 Complete Register Descriptions (continued)

Register Address	Register Name	Function	Read/Write Control
30 hex (48 decimal)	R48	Dark Row Options	RW

Default Contents = 0004 hex, 4 decimal:

bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
x	x	x	x	x	x	x	x	x	x	x	x	x	1	0	0

Description:
Dark row processing options. Effect on image data output is delayed by one frame. (3 bits)
Bit 2 = 1 (Read-only bit)
Bit 1 = Enable dark row processing. Adds one row to window size. Dark row is the first row transferred in a frame. To maintain the frame rate, reduce R6 (Vertical Blank Count) by 1 row.
Bit 0 = 0 (Read-only bit)

Limits:
Minimum = N/A
Maximum = N/A

Register Address	Register Name	Function	Read/Write Control
31 hex (49 decimal)	R49	Reserved	R

Default Contents = 0000 hex, 0 decimal:

bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

Description:
Reserved.

Limits:
Minimum = N/A
Maximum = N/A

2.6.4 Complete Register Descriptions (continued)

Register Address	Register Name	Function	Read/Write Control
32 hex (50 decimal)	R50	Image Test Data	RW

Default Contents = 0000 hex, 0 decimal:

bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
x	x	x	x	x	x	x	x	0	0	0	0	0	0	0	0

Description:
Data multiplexed into ADC data output path. Enabled by Bit 6 of R7. (8 bits)

Limits:
Minimum = 0
Maximum = 255

2.6.4 Complete Register Descriptions (continued)

Register Address	Register Name	Function	Read/Write Control
33 hex (51 decimal)	R51	Maximum Gain	RW

Default Contents = 0080 hex, 128 decimal:

bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
x	x	x	x	x	x	x	x	1	0	0	0	0	0	0	0

Description:
Maximum Gain allowed for auto-exposure routine. Default is 128 = Gain of 16.0. (8 bits)

Limits:
Minimum = 1
Maximum = 255
Default = 128

2.6.4 Complete Register Descriptions (continued)

Register Address	Register Name	Function	Read/Write Control
34 hex (52 decimal)	R52	Minimum Gain	RW

Default Contents = 0008 hex, 8 decimal:

bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
x	x	x	x	x	x	x	x	0	0	0	0	1	0	0	0

Description:
Minimum Gain allowed for auto-exposure routine. Default is 8 = Gain of 1.0. (8 bits)

Limits:
Minimum = 1
Maximum = 255
Default = 8

Register Address	Register Name	Function	Read/Write Control
35 hex (53 decimal)	R53	Global Gain	R* W

Default Contents = 0008 hex, 8 decimal:

bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
x	x	x	x	x	x	x	x	0	0	0	0	1	0	0	0

Description:
Global Gain register. Writes to this register are copied into all four Gain registers (R43 through R46), if bit 10 of R32 is set to 1. Effect on image data output is delayed by one frame. (8 bits)

*Reads from this register return the value in R43.

Limits:
Minimum = 1
Maximum = 255
Default = 8

2.6.4 Complete Register Descriptions (continued)

Register Address	Register Name	Function	Read/Write Control
36 hex (54 decimal)	R54	Maximum Frame	RW

Default Contents = 0003 hex, 3 decimal:

bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
x	x	x	x	x	x	x	x	x	x	x	x	0	0	1	1

Description:
Maximum frame integration time (programmed into R8) allowed for auto-exposure routine. (4 bits)

Limits:
Minimum = 0
Maximum = 15
Default = 3

Register Address	Register Name	Function	Read/Write Control
37 hex (55 decimal)	R55	Minimum Frame	RW

Default Contents = 0000 hex, 0 decimal:

bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
x	x	x	x	x	x	x	x	x	x	x	x	0	0	0	0

Description:
Minimum frame integration time (programmed into R8) allowed for auto-exposure routine. (4 bits)

Limits:
Minimum = 0
Maximum = 15
Default = 0

2.6.4 Complete Register Descriptions (continued)

Register Address	Register Name	Function	Read/Write Control
38 hex (56 decimal)	R56	Reserved	R

Default Contents = 0000 hex, 0 decimal:

bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

Description:
Reserved.

Limits:
Minimum = N/A
Maximum = N/A

Register Address	Register Name	Function	Read/Write Control
39 hex (57 decimal)	R57	VOFFSET	RW

Default Contents = 0000 hex, 0 decimal:

bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
x	x	x	x	x	x	x	x	x	x	0	0	0	0	0	0

Description:
Controls voltage offset added to signal before Gain. (6 bits)

Limits:
Minimum = 0
Maximum = 63

2.6.4 Complete Register Descriptions (continued)

Register Address	Register Name	Function	Read/Write Control
3A hex (58 decimal)	R58	Snap-Shot Sequence Trigger	RW

Default Contents = 0000 hex, 0 decimal:

bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	0

Description:
Trigger for capturing a still image. When set, causes the sensor to restart the shutter, output a single frame (regardless of the state of chip enable), and then disable the chip enable bit (Bit 1 of R7). Do not use with dark row processing enabled. (1 bit)

Limits:
Minimum = N/A
Maximum = N/A

Register Address	Register Name	Function	Read/Write Control
3B hex (59 decimal)	R59	VREF_HI	RW

Default Contents = 000B hex, 11 decimal:

bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
x	x	x	x	x	x	x	x	x	x	x	0	1	0	1	1

Description:
Voltage that sets the high end of the ADC range. Effect on image data output is delayed by one frame. (5 bits)

Limits:
Minimum = 0
Maximum = 31
Default = 11

2.6.4 Complete Register Descriptions (continued)

Register Address	Register Name	Function	Read/Write Control
3C hex (60 decimal)	R60	VREF_LO	RW

Default Contents = 0001 hex, 1 decimal:

bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
x	x	x	x	x	x	x	x	x	x	x	0	0	0	0	1

Description:
Voltage that sets the low end of the ADC range. Effect on output is delayed by one frame. (5 bits)

Limits:
Minimum = 0
Maximum = 31
Default = 1

Register Address	Register Name	Function	Read/Write Control
3D hex (61 decimal)	R61	Reserved	R

Default Contents = 0000 hex, 0 decimal:

bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

Description:
Reserved.

Limits:
Minimum = N/A
Maximum = N/A

2.6.4 Complete Register Descriptions (continued)

Register Address	Register Name	Function	Read/Write Control
3E hex (62 decimal)	R62	Reserved	R

Default Contents = 0000 hex, 0 decimal:

bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

Description:
Reserved.

Limits:
Minimum = N/A
Maximum = N/A

Register Address	Register Name	Function	Read/Write Control
3F hex (63 decimal)	R63	Reserved	R

Default Contents = 0000 hex, 0 decimal:

bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

Description:
Reserved.

Limits:
Minimum = N/A
Maximum = N/A

2.6.4 Complete Register Descriptions (continued)

Register Address	Register Name	Function	Read/Write Control
40 hex (64 decimal)	R64	Red/Blue Gain	RW

Default Contents = 0808 hex, 2056 decimal:

bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0

Description:
Bits 15-8 = Red Gain. Bits 7-0 = Blue Gain. Effect on image data output is delayed by one frame.

Note:
R64 to R67, which are optimized for high-speed sequential programming through the I^2C bus, provide additional access to the registers required by an external auto-exposure routine.

Limits:
Minimum = 0
Maximum = 65,535

Register Address	Register Name	Function	Read/Write Control
41 hex (65 decimal)	R65	Green 2/Green 1 Gain	RW

Default Contents = 0808 hex, 2056 decimal:

bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0

Description:
Bits 15-8: Green 2 gain. Bits 7-0: Green 1 gain. Effect on image data output is delayed by one frame.

Note:
R64 to R67, which are optimized for high-speed sequential programming through the I^2C bus, provide additional access to the registers required by an external auto-exposure routine.

Limits:
Minimum = 0
Maximum = 65,535

2.6.4 Complete Register Descriptions (continued)

Register Address	Register Name	Function	Read/Write Control
42 hex (66 decimal)	R66	VREF_HI/LO	RW

Default Contents = 0161 hex, 353 decimal:

bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
x	x	x	x	x	x	0	1	0	1	1	0	0	0	0	1

Description:
Bits 9-5: VREF_HI. Bits 4-0: VREF_LO. Effect on image data output is delayed by one frame.

Note:
R64 to R67, which are optimized for high-speed sequential programming through the I^2C bus, provide additional access to the registers required by an external auto-exposure routine.

Limits:
Minimum = 0
Maximum = 1,023

Register Address	Register Name	Function	Read/Write Control
43 hex (67 decimal)	R67	Integration Time/ Row Unit Count	RW

Default Contents = 0050 hex, 80 decimal:

bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
x	x	0	0	0	0	0	0	0	1	0	1	0	0	0	0

Description:
Copy of R9. Effect on image data output is delayed by one frame.

Note:
R64 to R67, which are optimized for high-speed sequential programming through the I^2C bus, provide additional access to the registers required by an external auto-exposure routine.

Limits:
Minimum = 1
Maximum = 16,383
Default = 80

2.6.4 Complete Register Descriptions (continued)

Register Address	Register Name	Function	Read/Write Control
F0 hex (240 decimal)	R240	ADC Test	RW

Default Contents = 0000 hex, 0 decimal:

bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	0

Description:
Bit 0 = ADC test mode, if set.

Note:
R240 through R242 can be programmed through the Control Mode Register, R7. They are included here for test purposes.

Limits:
Minimum = N/A
Maximum = N/A

Register Address	Register Name	Function	Read/Write Control
F1 hex (241 decimal)	R241	Chip Enable	RW

Default Contents = 0001 hex, 1 decimal:

bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	1

Description:
Bit 0 = CE (Chip Enable) stops video output at end of current frame when set to 0.

Note:
R240 through R242 can be programmed through the Control Mode Register, R7. They are included here for test purposes.

Limits:
Minimum = N/A
Maximum = N/A

2.6.4 Complete Register Descriptions (continued)

Register Address	Register Name	Function	Read/Write Control
F2 hex (242 decimal)	R242	Reserved	R

Default Contents = 0000 hex, 0 decimal:

bit 15	bit 14	bit 13	bit 12	bit 11	bit 10	bit 9	bit 8	bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
x	x	x	x	x	x	x	x	x	x	0	0	0	0	0	0

Description:
Reserved.

Note:
R240 through R242 can be programmed through the Control Mode Register, R7. They are included here for test purposes.

Limits:
Minimum = N/A
Maximum = N/A

2.7 Auto-Exposure

The PB-0100 auto-exposure module controls the brightness of the captured image by automatically adjusting three parameters: integration time, ADC reference (VREF_HI), and gain. The algorithm sub-samples the image and counts the number of bright and dark pixels in the sub-sampled image. If the number of bright pixels exceeds a certain threshold, the algorithm darkens the image by reducing the integration time, increasing the ADC reference, or lowering the gain. Likewise, if the number of dark pixels exceeds a certain threshold, the algorithm brightens the image by increasing the integration time, decreasing the ADC reference, or raising the gain.

Auto-exposure is enabled by default on power-up. The settings for auto-exposure are controlled by Registers 14 through 28, 51, 52, 54, and 55.

Integration Time

The integration time determines how long a pixel is allowed to collect light before it is read out. The longer the pixel is allowed to collect light, the brighter the image will be. However, at some point the pixel will saturate (either due to collected photons or, with extremely long integration times, dark current) and will no longer respond to light. The pixel saturation region of operation should be avoided, as it produces "dirty" looking images (pixel level fixed pattern noise) in the white regions of the images, due to pixel level parameter variations. Using a gain of at least 2 ensures that the signal chain or ADC will saturate or go out of range before the pixel saturates. This produces a clean, uniform white level.

The PB-0100 counts the integration time in terms of the row time, which is the time required for the PB-0100 to read, gain, and convert one row of pixels (the default row time is 104 microseconds). If the number of rows of integration exceeds the number of rows in the image, then the frame rate will slow down as the imager pauses to allow for pixel integration. The other drawback of arbitrarily increasing the integration time is the increasing smear of movement in the scene.

By default, the auto-exposure routine will not increase the integration time beyond one frame where one frame is defined by Reg. 15 (Expose0). Setting Bit 5 of Reg. 14 will allow the auto-exposure to use multi-frame integration. The maximum and minimum number of frames of integration that the auto-exposure can use are set in Reg. 54 (Maximum Frame) and Reg. 55 (Minimum Frame). Note that if multi-frame integration is enabled, the output frame rate will vary depending on the lighting conditions.

By default, the auto-exposure routine can pick between only three discrete integration times, which are set in Reg. 15 (Expose0), Reg. 16 (Expose1), and Reg. 17 (Expose2). To avoid banding in the image from 60 Hz light flicker, these integration times are set to 1/30th, 1/60th, and 1/120th of a second, respectively. However, if Bit 6 of Reg. 14 is set, the auto-exposure routine will vary the integration time linearly between Reg. 17 (Expose2) and Reg. 15 (Expose0). This mode is intended for naturally lit scenes where 60 Hz light flicker is not a problem and intensity varies slowly.

Gain

The PB-0100 contains programmable gain amplifiers that apply gain to the analog pixel signal. The gain is individually controllable for each color in the Bayer pattern, which allows for white balance adjustments before analog to digital conversion. By default, the auto-exposure routine does not change the gain; gain adjustment is enabled by setting Bit 4 of Reg. 14.

The gain for each color is adjusted individually and in increments of 1/8th of the current value (rounded down to multiples of 0.125). For example, if the current gains in Red, Green1, Green2, and Blue are 10.5 (01010100), 8 (01000000), 8 (01000000), and 12 (01100000), and the scene is too dark, the new gains will be 11.75 (01011110), 9 (01001000), 9 (01001000), 13.5 (01101100). If the scene is too bright, the new gains will be 9.25 (01001010), 7 (00111000), 7 (00111000), and 10.5 (01010100).

Adjustments in this manner allow for the ratio between the color gains (the color balance) to be maintained across auto-exposure changes.

The maximum and minimum gains used by the auto-exposure are set in Reg. 51 (Maximum Gain) and Reg. 52 (Minimum Gain). The Green1 gain is checked against the maximum and minimum gains before adjustments are made. If the Green1 gain is less than or equal to the minimum, or greater than or equal to the maximum, no gain adjustments are made to any of the color gains.

2.7 Auto-Exposure (continued)

Gain (continued)
To avoid an underflow in Green1 gain, the smallest value that can be programmed into Reg. 52 (Minimum Gain) is 0.875 (00000111). To avoid an overflow in Green1 gain, the largest value that can be programmed into Reg. 51 (Maximum Gain) is 28.5 (11100100). Care should be used in programming the gain limits, since an overflow/underflow can occur in a color gain other than Green1 if that color starts at a gain value other than Green1. The Maximum and Minimum Gains may be adjusted to avoid this.

ADC Reference
The ADC reference VREF_HI (along with VREF_LO) sets the size of the least significant bit (LSB) in the analog to digital conversion process. A smaller VREF_HI produces a smaller LSB, which means a smaller analog signal level input is required to produce the same digital code out. Likewise, a larger VREF_HI produces a larger LSB, which means a larger analog signal level input is required to produce the same digital code out. Thus, the VREF_HI value can be used like a global gain adjustment.

The limits on the auto-exposure VREF_HI values are set in Reg. 12 (Low0_DAC), Reg. 13 (Low1_DAC), Reg. 14 (Low2_DAC), and Reg. 24 (High_DAC). The minimum value of VREF_HI is individually programmable according to the current integration time choice. Low0_DAC, Low1_DAC, and Low2_DAC correspond to Expose0, Expose1, and Expose2, respectively. The maximum value of VREF_HI is the same for all three integration time choices, and is set by High_DAC.

When the auto-exposure wants to brighten the image and has hit the lower limit on the VREF_HI value, as programmed in Low0_DAC, Low1_DAC, or Low2_DAC, it will transition to the next longer integration time (i.e., from Expose2 to Expose1, or from Expose1 to Expose0). Simultaneously, it will set the VREF_HI value to Trans1H (if going from Expose2 to Expose1) or Trans0H (if going from Expose1 to Expose0).

Similarly, when the auto-exposure wants to darken the image and has hit the upper limit on the VREF_HI value, as programmed in High_DAC, it will transition to the next shorter integration time (i.e. from Expose0 to Expose1, or from Expose1 to Expose2). Simultaneously, it will set the VREF_HI value to Trans1L (if going from Expose0 to Expose1) or Trans2L (if going from Expose1 to Expose2).

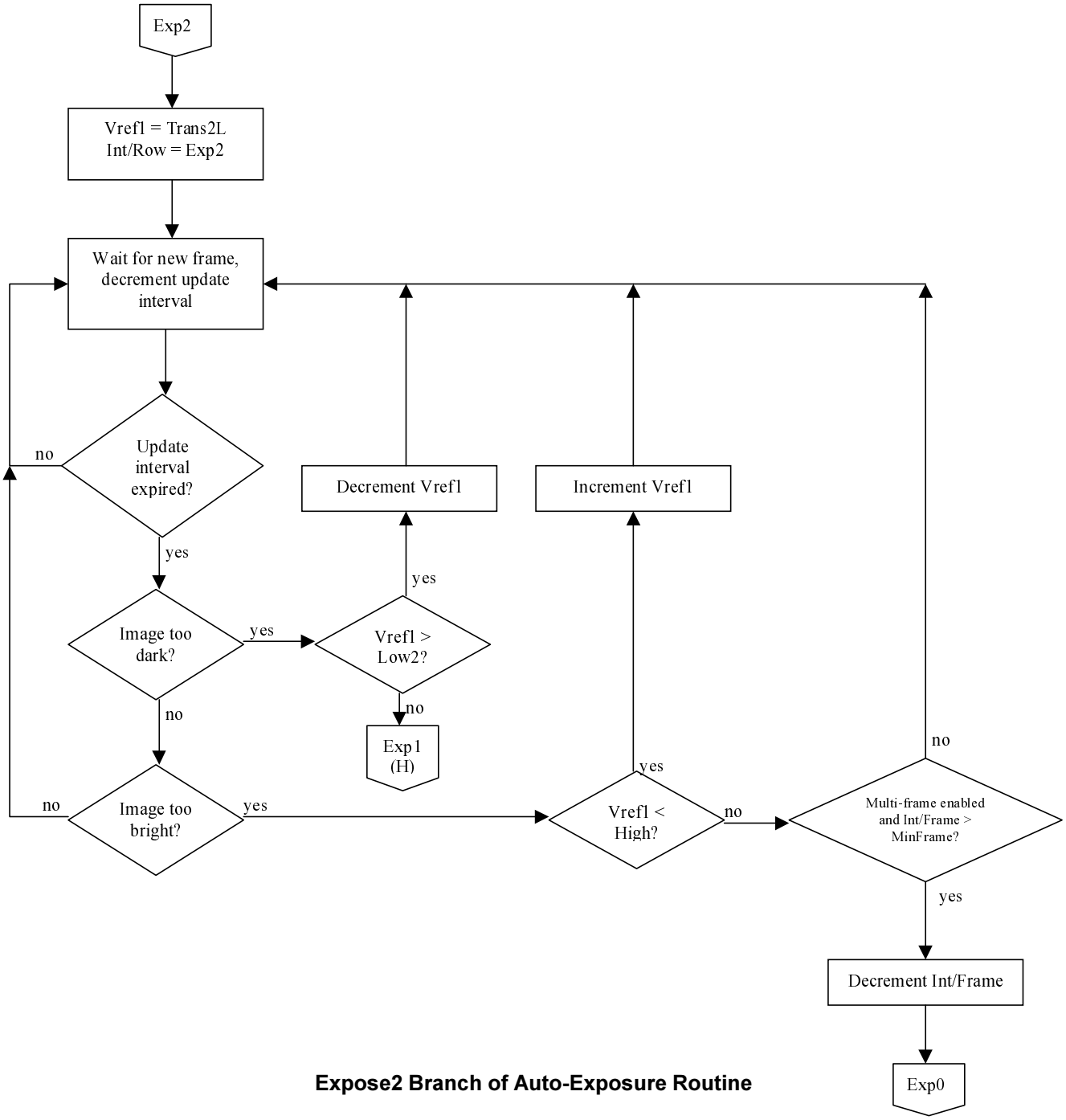
VREF_LO is not modified by the auto-exposure routine. It can be set through the I^2C port to adjust the black level of the image. If the image is washed out (black is gray), then VREF_LO should be increased. If dark area detail is being lost (gray is black), then VREF_LO should be decreased.

Sub-Sampling
The image is sub-sampled for auto-exposure pixel statistics. The sub-sampling is done on green pixels, for every eighth pixel on a row and for every eighth row, thereby sampling one pixel for every 64 in the image. Every sampled pixel is categorized as bright or dark, and the corresponding count is incremented.

Bright Pixel/Dark Pixel
A bright pixel is defined as having a value greater than or equal to 192. A dark pixel is defined as having a value less than or equal to 127.

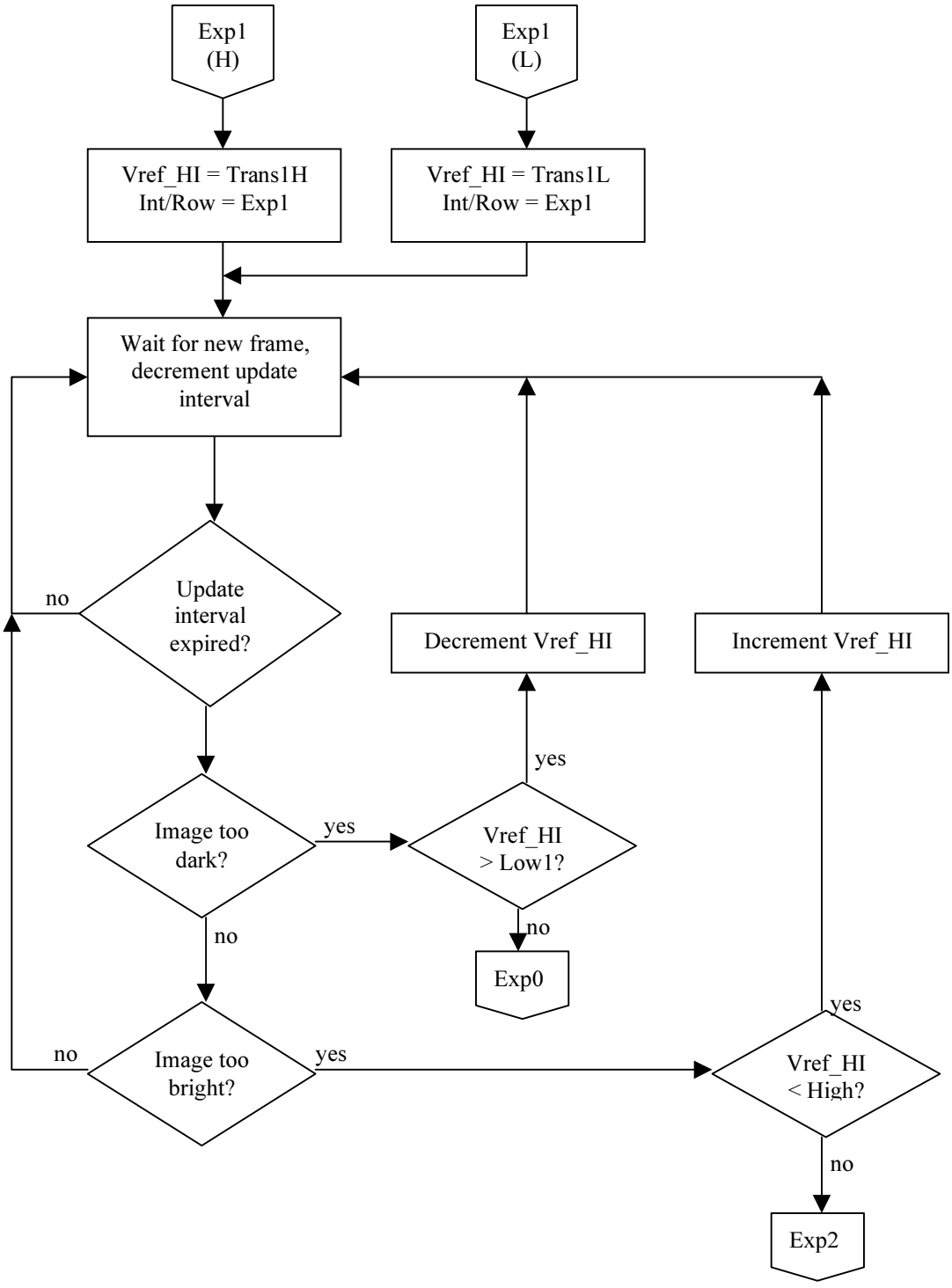
Update Interval
The auto-exposure can be programmed to wait a certain number of frames between evaluations of the image for exposure changes. This update interval is programmed in Reg. 23 and defaults to 8. When using linear integration mode, the update interval should be reduced to 1 to increase the speed of this mode.

Thresholds
The threshold registers, Reg. 21 (Threshold11) and Reg. 22 (Threshold0x), control how the auto-exposure decides if the image is too dark or too bright. When the number of dark pixels exceeds Threshold0x, the auto-exposure calculates that the image is too dark and attempts to brighten the image. When the number of bright pixels exceeds Threshold11, the auto-exposure calculates that the image is too bright and attempts to darken the image. Default values for the CIF-size window are Threshold0x = 1188 pixels (75% of the 1584 sub-sampled pixels) and Threshold11 = 476 (30% of the 1584 sub-sampled pixels). For different-size image windows, the thresholds must be adjusted appropriately. Note that to avoid oscillation, the sum of Threshold0x and Threshold11 should be slightly greater than the number of sub-sampled pixels.

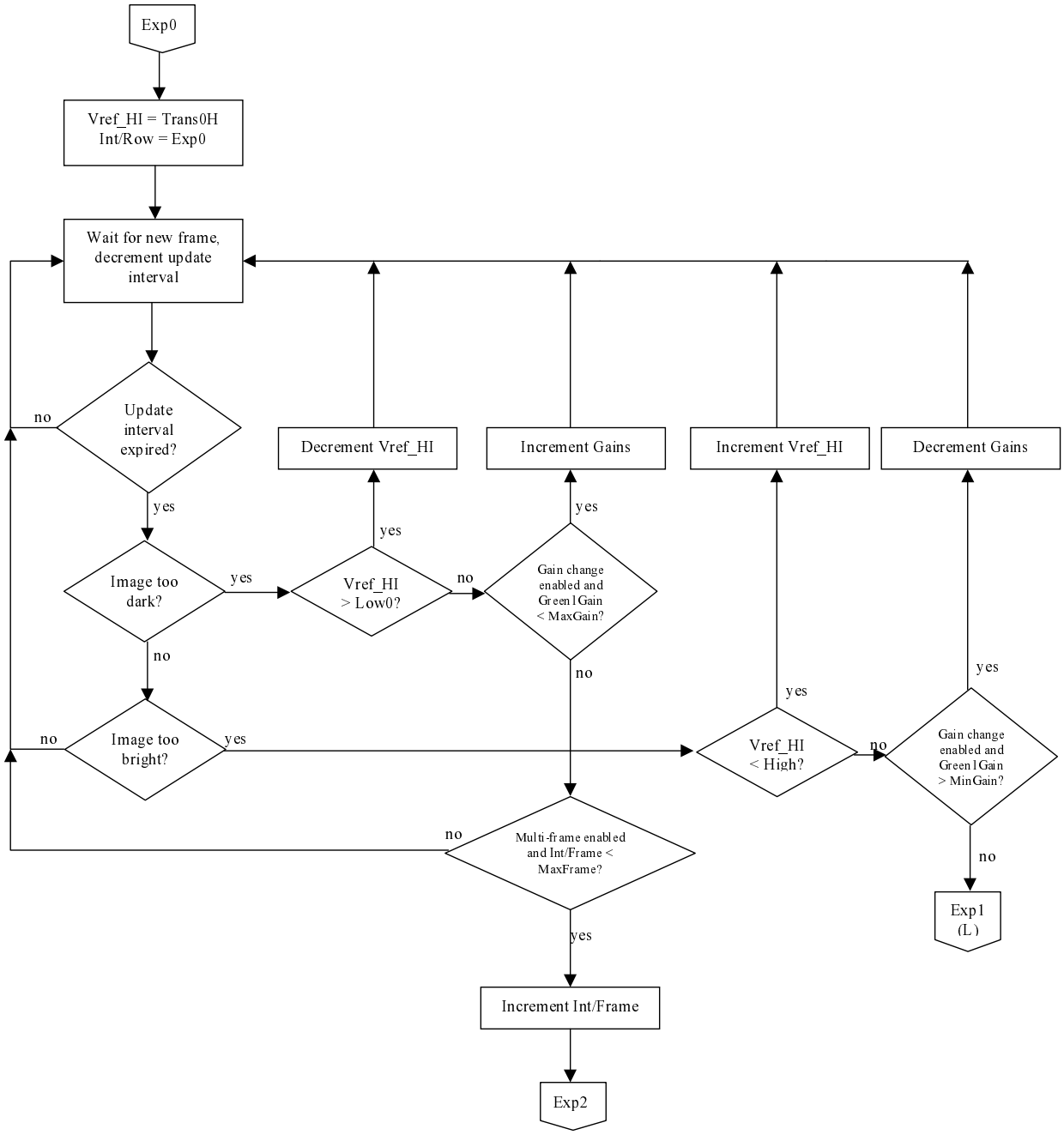


Expose2 Branch of Auto-Exposure Routine

2.7 Auto-Exposure (continued)

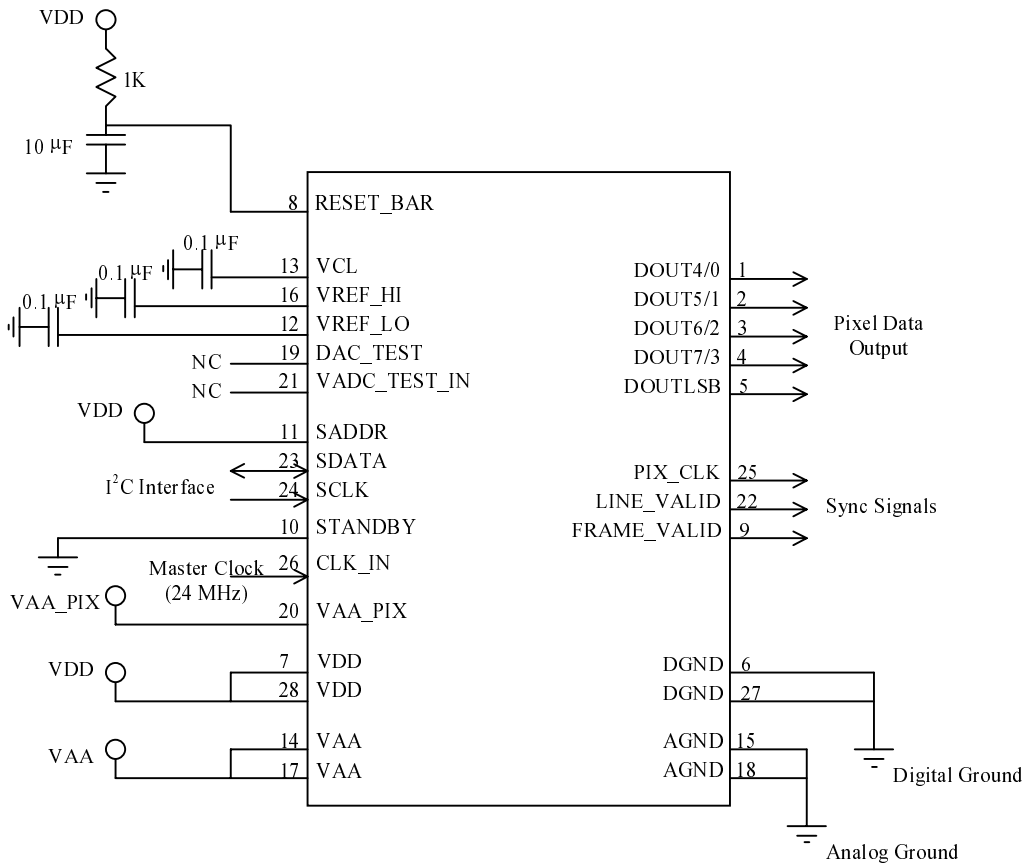


Expose1 Branch of Auto-Exposure Routine

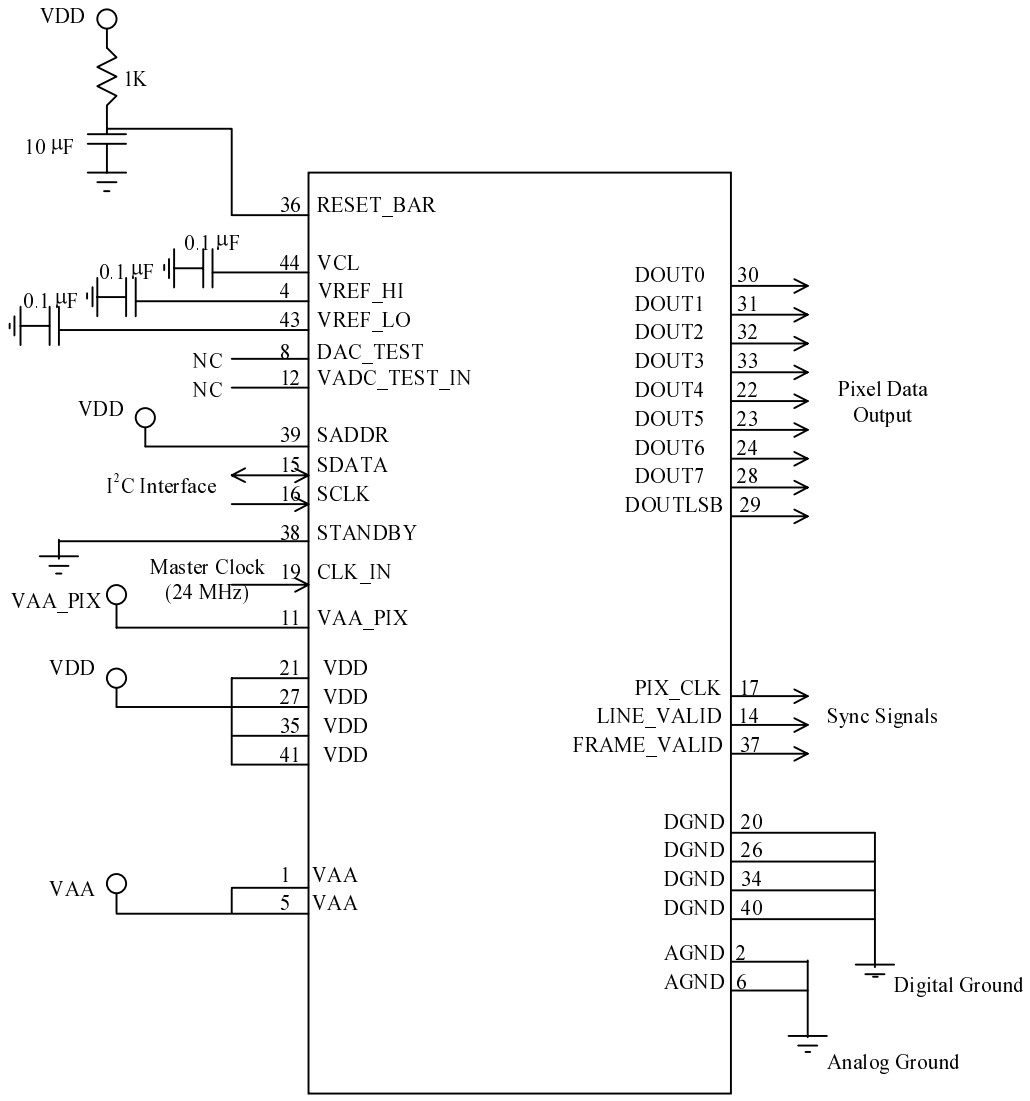


Expose0 Branch of Auto-Exposure Routine

2.8 Board Connections



28-Pin Sensor (PB-0100)



44-Pin Sensor (PB-0101)

2.9 Electrical Specification

Absolute Maximum Ratings[1]

Symbol	Parameter	Value	Unit
Vpwr	DC Supply Voltage	-0.5 to 5.5	V
Vin	DC Input Voltage	-0.5 to VDD + 0.5	V
Vout	DC Output Voltage	-0.5 to VDD + 0.5	V
I	DC Current Drain per Pin (Any I/O)	±50	mA
I	DC Current Drain, Vpwr and Vgnd	±100	mA

[1]Maximum Ratings are those values beyond which damage to the device may occur. Vpwr = VDD = VAA = VAA_PIX (VDD is supply to digital circuit, VAA to analog circuit, VAA_PIX to pixel array).Vgnd = DGND = AGND (DGND is the ground to the digital circuit, AGND to the analog circuit).

DC Electrical Characteristics (Vpwr = 3.3V +/- 0.3V; TA = 0°C to 70°C)

Symbol	Characteristic	Condition	Min.	Max.	Unit
VIH	Input High Voltage		2.0	Vpwr+0.3	V
VIL	Input Low Voltage		-0.3V	0.8	V
IIN	Input Leakage Current, No Pullup Resistor	Vin = Vpwr or Vgnd	-5	5	uA
VOH	Output High Voltage	Vpwr=Min, IOH=-100uA	Vpwr-0.2		V
VOL	Output Low Voltage	Vpwr=Min, IOL=100uA		0.2	V
IOZ	3-State Output Leakage Current	Sdata in high Z, Vout=Vpwr or Vgnd	-10	10	uA
Ipwr[1]	Maximum Quiescent Supply Current	Iout=0mA, Vin=Vpwr or Vgnd	0	50	mA

[1]Ipwr = I(VDD) + I(VAA) + I(VAA_PIX) (VDD is supply to digital circuit, VAA to analog circuit, VAA_PIX to pixel array)

Power Dissipation (TA = 25°C)

Symbol	Characteristic	Condition	Typical	Unit
Ppwdn	Powerdown Power	Vdd=3.3V, Vaa=0V, Vaa_pix=0V, clock stopped, standby enabled.	0.3	mW
Pstdby	Standby Power	Vdd=3.3V, Vaa=3.3V, Vaa_pix=3.3V, clock stopped, standby enabled.	20	mW
Pavg	Average Power	Vdd=3.3V, Vaa=3.3V, Vaa_pix=3.3V	100	mW

2.9 Electrical Specification (continued)

AC Electrical Characteristics (Vpwr = 3.3V +/- 0.3V; TA = 0°C to 70°C)

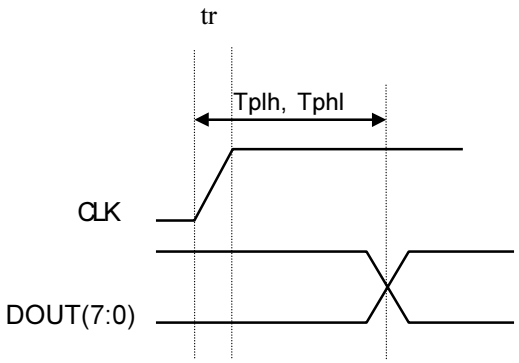
Symbol	Characteristic	Condition	Min.	Max.	Unit
Tplh	Data output propogation delay for low to high trans.			20ns	ns
Tphl	Data output propogation delay for high to low trans.			20ns	ns
Tsetup	Setup time for input to CLK	Vin = Vpwr or Vgnd	10		ns
Thold	Hold time for input to CLK	Vpwr=Min,VOH min	0		ns
Tr, Tf	Input rise and fall time		2		ns

Recommended Operating Conditions (to guarantee functionality)

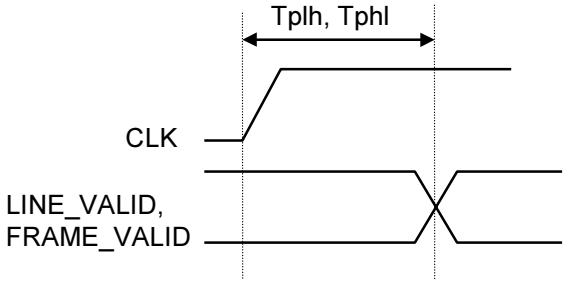
Symbol	Parameter	Min.	Max.	Unit
Vpower	DC Supply Voltage	3.0	3.6	V
TA	Commercial Operating Temperature	0	70	C
TJ	Junction Temperature	0	85	C

Special handling notes: This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than the maximum rated voltages.

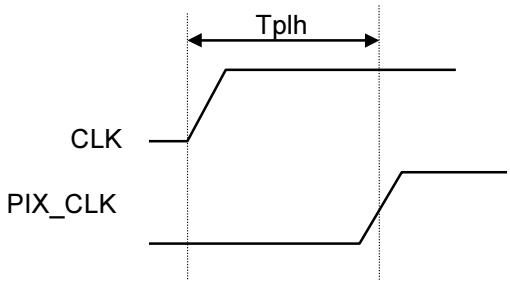
2.9 Electrical Specification (continued)

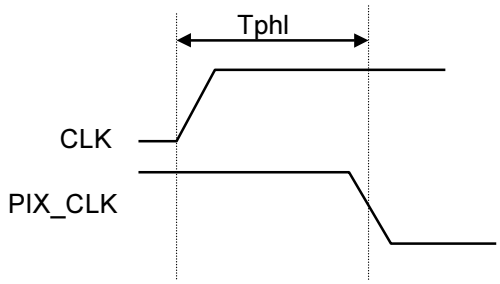


Clock to Data Propagation Delay



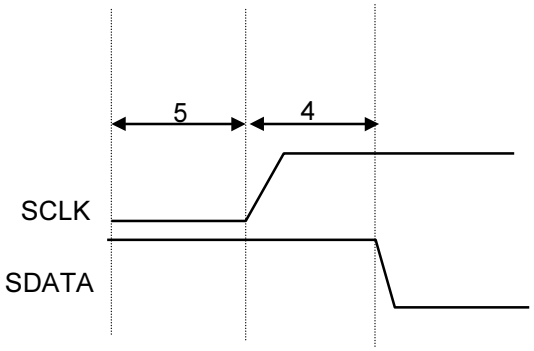
Clock to Line- or Frame-Valid Output Propagation Delay



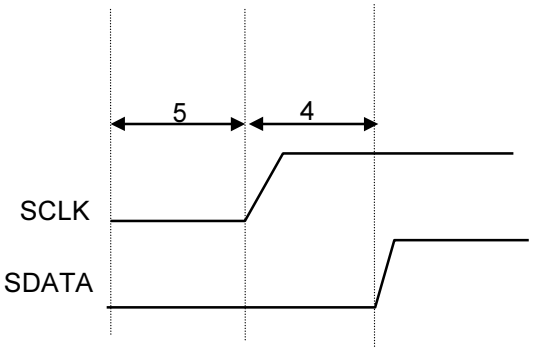


Clock to Pixel Clock Output Propagation Delay

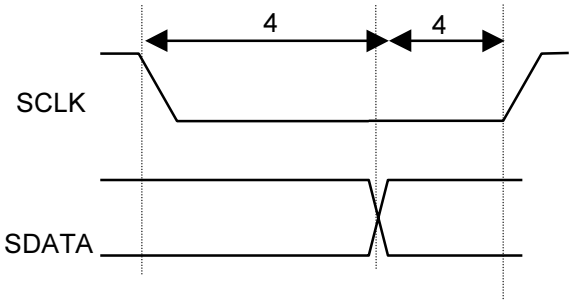
(Timing in units of master clock cycles)



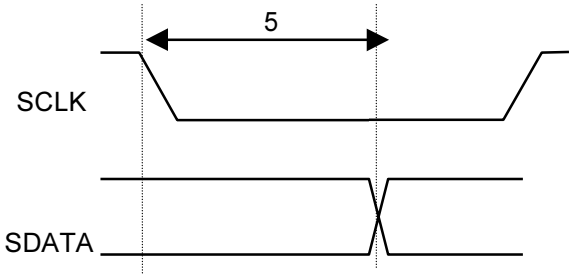
I²C Start Condition Timing



I²C Stop Condition Timing



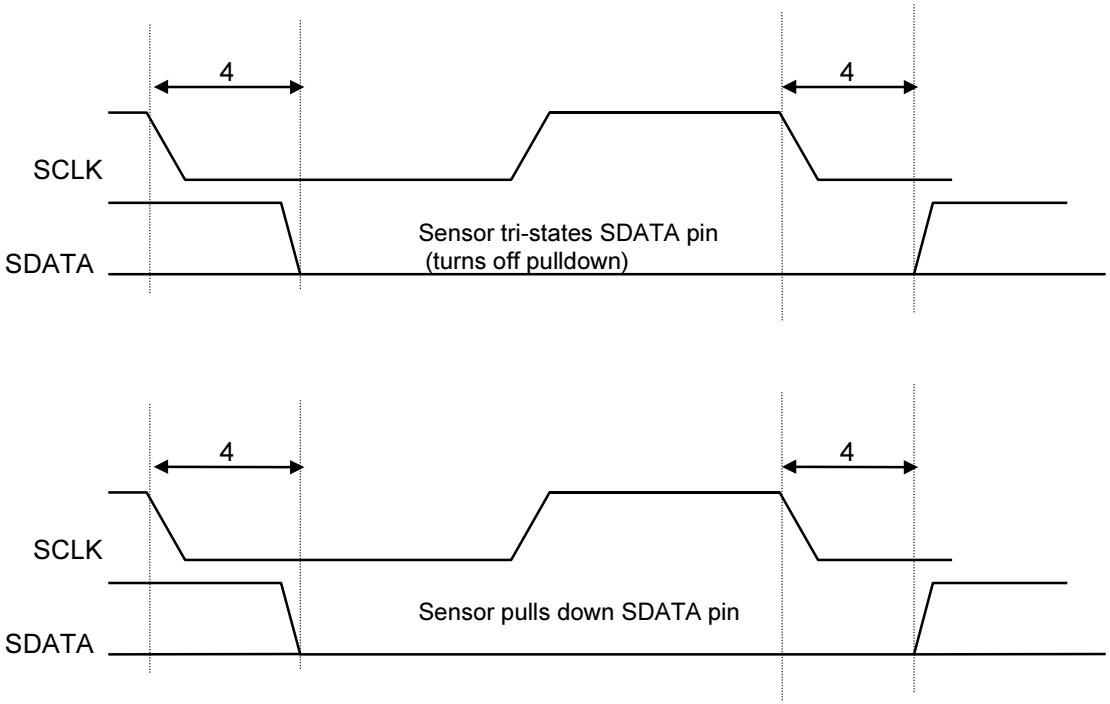
I²C Data Timing for Write
SDATA is driven by off-chip transmitter.



I²C Data Timing for Reads
SDATA is pulled low by sensor or allowed to pull high by pull-up resistor off-chip.

2.9 Electrical Specification (continued)

(Timing in units of master clock cycles)



Acknowledge Signal timing After an 8-Bit Read From the Sensor (top) and After an 8-Bit Write To the Sensor (bottom)

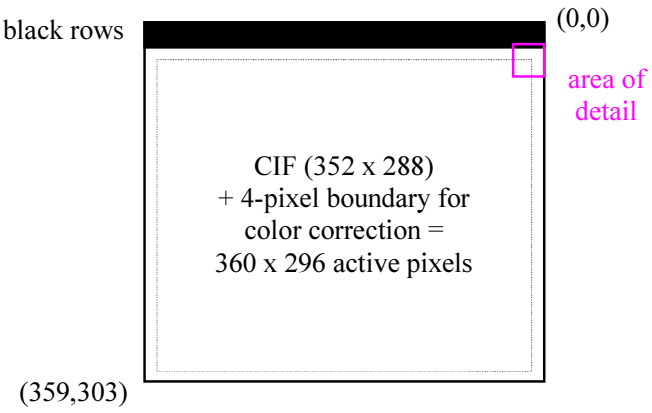
After a read, the master receiver must pull down SDATA to acknowledge receipt of data bits. Master generates no acknowledge, leaving SDATA to float high, when read sequence is complete. On the following cycle a start or stop bit may be used.

3.0 Optical

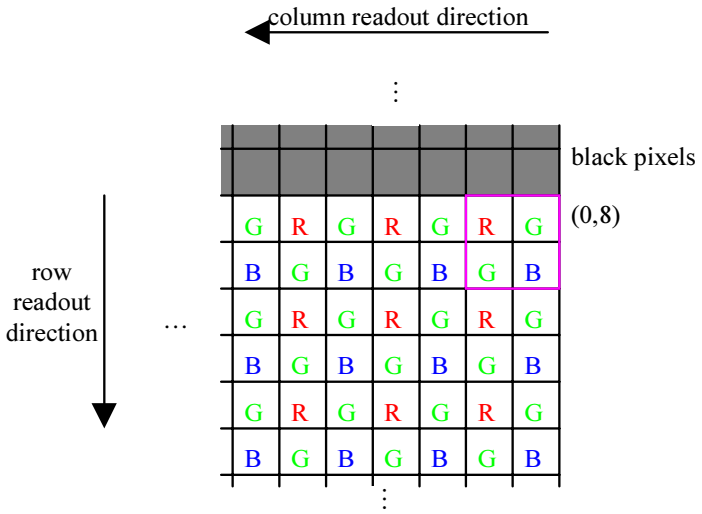
Format: 1/5-inch
Sensor area: 2.84 mm x 2.34 mm
Pixel pitch: 7.9 microns

Typical f-numbers = f/1.8–f/2.8
Typical focal lengths = 3 mm–6 mm
Typically 1–5 elements

Field of view (horizontal) = 50–25 degrees, respectively



Pixel Array Layout



Bayer Pattern (Pixel Color Pattern Detail)

Pixel read out proceeds from right to left, and from top row to bottom row. Image can be mirrored (read out from left to right) by setting bit 14 of register 32, which will change the color pixel order. (Does not apply to monochrome sensors.)

3.1 Optical Specification

Image Sensor Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Unit
Digital Responsivity	(Gain 8, "Illuminant A" Infrared cut-off filter $\lambda_{0.5}$=[400÷710]nm)				
	Red		2000		bits/μJ/cm^2
	Green		950		bits/μJ/cm^2
	Blue		430		bits/μJ/cm^2
SIG_NU	Responsivity non-uniformity			3	%
Nsat	Pixel saturation level	67,000			electrons
Vdrk	Output referred dark signal			35	mV/sec
NE	Input referred noise			40	electrons
Dyn_I	Internal dynamic range	64			dB
DRK_NU	Dark signal non-uniformity			50	%
Kdrk	Dark current temperature coefficient			100	%/8C

Pixel Array Parameters

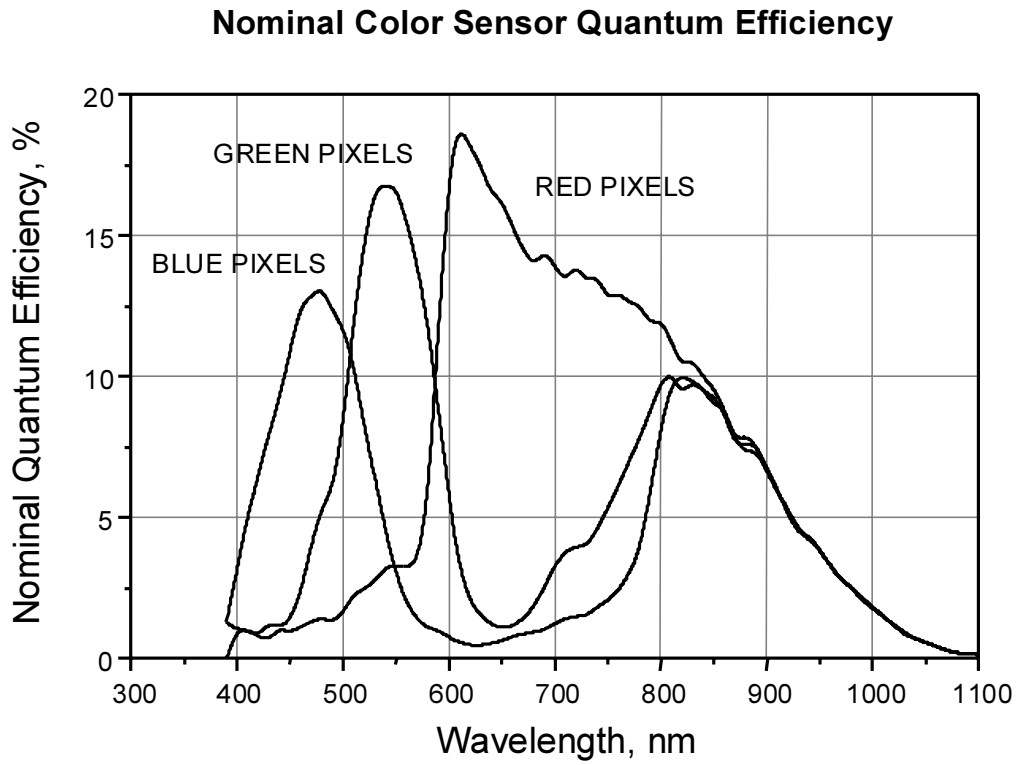
Symbol	Parameter	Min.	Typ.	Max.	Unit
Resolution	Number of pixels in optical array		360 x 296		pixels
Pixel size	X-Y dimensions		7.9 x 7.9		um
Pixel pitch	Center to center pixel spacing			7.9	um
Pixel fill factor	Drawn active to total pixel area		24		%

Color Filter Characteristics[1]

Symbol	Parameter	Min.	Typ.	Max.	Unit
QEr	Red Peak Quantum Efficiency		19		%
QEg	Green Peak Quantum Efficiency		17		%
QEb	Blue Peak Quantum Efficiency		13		%
CC_NU	Chip Color filter response non-uniformity			5	%
WC_NU	Wafer Color filter response non-uniformity			15	%

[1]Color mosaic pattern defined as follows:
even row, even column address: Green
even row, odd column address: Red
odd row, even column address: Blue
odd row, odd column address: Green

3.2 Quantum Efficiency

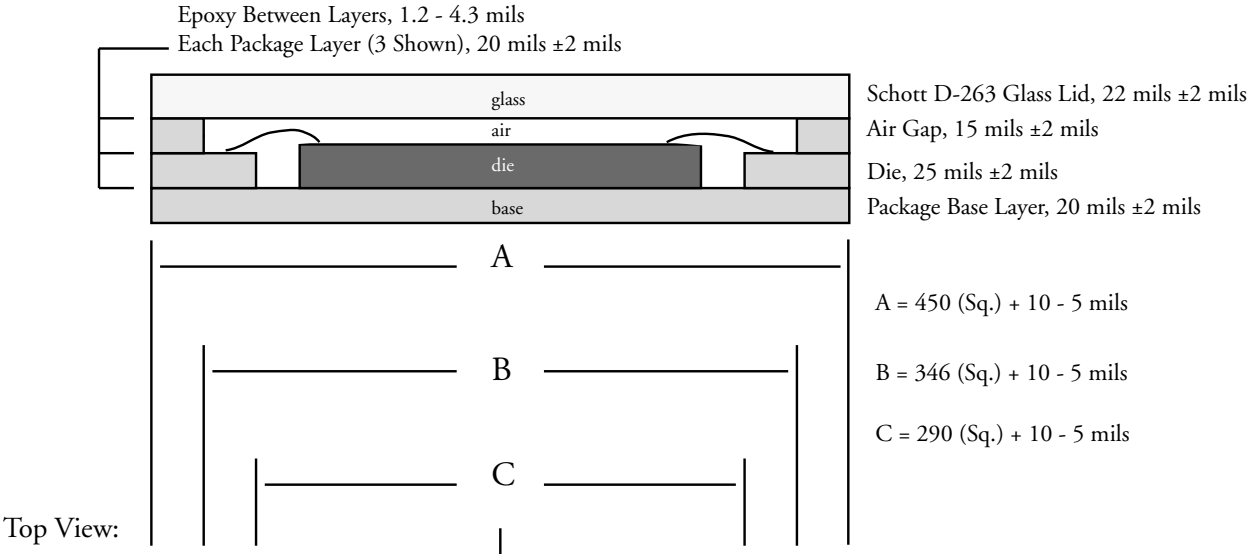


Wave	RED	GREEN	BLUE	Wave	RED	GREEN	BLUE	Wave	RED	GREEN	BLUE
390	1.3	0.0	1.3	630	17.5	1.6	0.5	870	7.7	7.6	7.8
400	1.0	1.0	3.1	640	16.5	1.2	0.6	880	7.9	7.6	7.3
410	1.0	1.0	5.1	650	16.3	1.1	0.6	890	7.6	7.6	7.4
420	0.8	0.8	6.5	660	15.3	1.2	0.8	900	6.8	6.6	6.7
430	0.6	1.3	8.0	670	14.5	1.4	0.9	910	6.1	6.0	5.9
440	1.1	1.1	9.2	680	13.9	1.8	0.9	920	5.2	5.2	5.3
450	0.9	1.4	10.9	690	14.5	2.5	1.0	930	4.5	4.5	4.6
460	1.1	2.3	12.5	700	13.9	3.3	1.3	940	4.4	4.3	4.2
470	1.3	4.0	12.9	710	13.4	3.8	1.4	950	3.9	3.9	3.9
480	1.5	5.4	13.2	720	14.0	4.0	1.5	960	3.3	3.3	3.3
490	1.3	5.9	12.3	730	13.3	4.0	1.5	970	2.9	2.9	2.8
500	1.6	8.3	11.7	740	13.6	4.6	1.8	980	2.5	2.5	2.5
510	2.3	12.0	10.5	750	12.7	5.3	2.1	990	2.1	2.1	2.1
520	2.5	14.8	8.2	760	13.0	6.1	2.4	1000	1.8	1.9	1.8
530	2.8	16.7	6.4	770	12.6	7.0	3.0	1010	1.5	1.5	1.5
540	3.2	16.8	4.6	780	12.6	7.8	3.8	1020	1.2	1.2	1.2
550	3.3	16.7	3.0	790	11.9	8.7	5.8	1030	0.9	0.9	0.9
560	3.2	15.5	1.9	800	12.0	9.8	8.2	1040	0.7	0.7	0.7
570	3.4	14.0	1.4	810	11.3	10.1	9.7	1050	0.6	0.6	0.6
580	5.4	11.9	1.1	820	10.3	9.4	10.0	1060	0.5	0.5	0.5
590	11.5	9.0	1.0	830	10.6	9.9	9.9	1070	0.3	0.3	0.3
600	17.3	5.7	0.7	840	10.0	9.5	9.6	1080	0.2	0.2	0.2
610	19.0	3.3	0.6	850	9.6	9.3	9.0	1090	0.2	0.2	0.2
620	18.1	2.0	0.5	860	8.8	8.8	8.9	1100	0.1	0.1	0.1

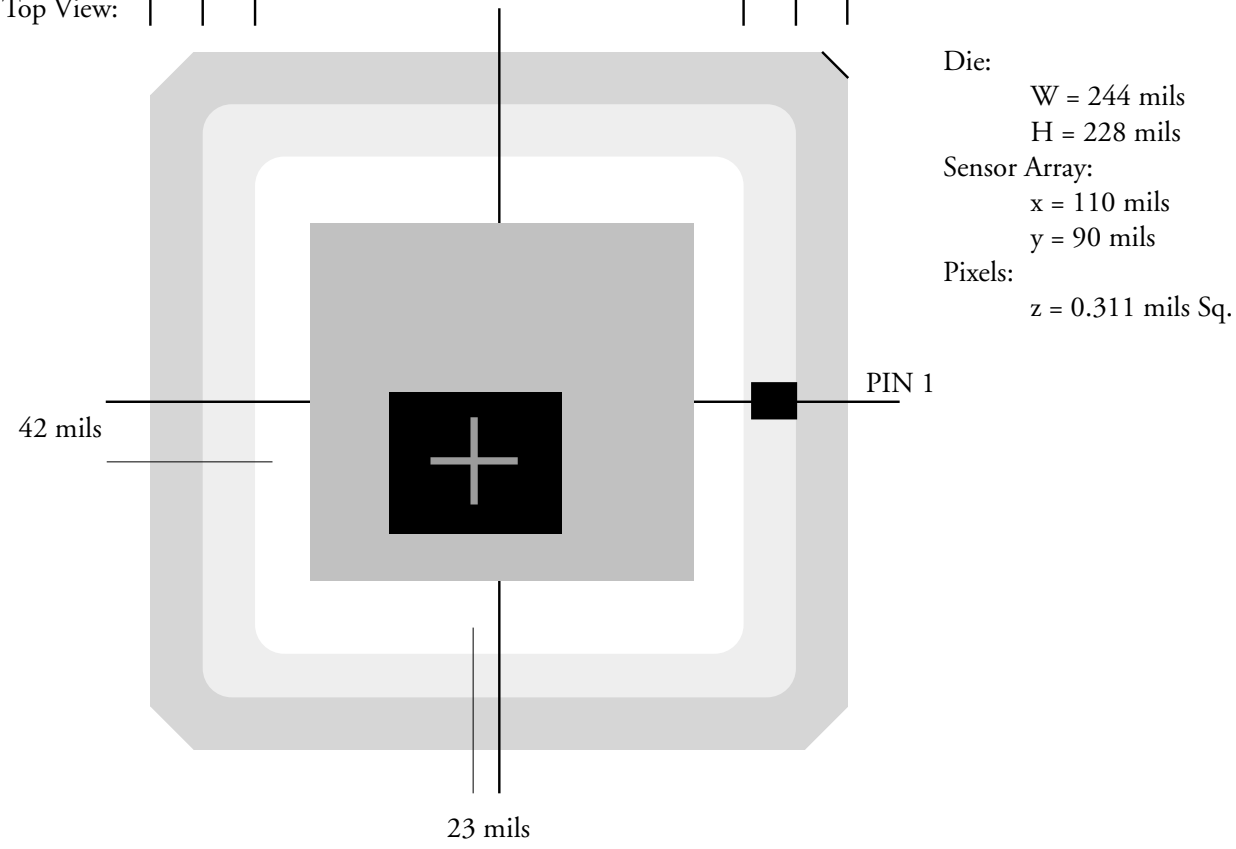
3.3 Pixel Array Offset Drawings

28-Pin CLCC (Ceramic Leadless Chip Carrier) — PB-0100
Chip Centered on Package Center, Pixel Array Off-Center

Cut-Away Side View:

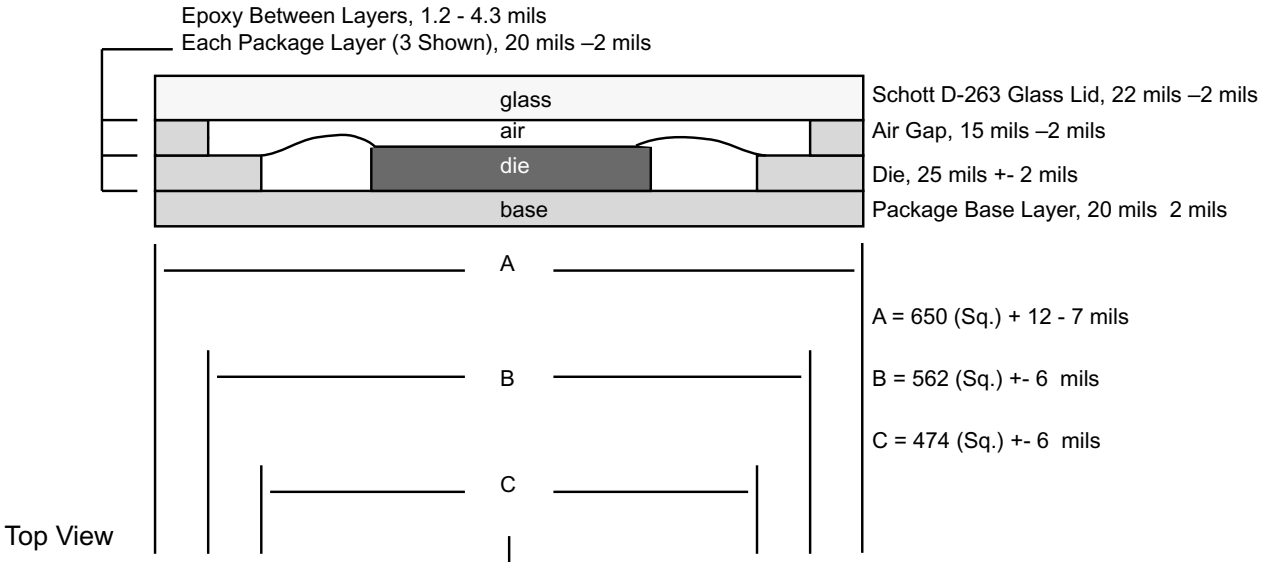


Top View:



44-Pin CLCC (Ceramic Leadless Chip Carrier) — PB-0101
Chip Centered on Package Center, Pixel Array Off-Center

Cut-Away Side View



3.4 Lens Selection

Much of the specific information in this section is explained in detail in the Technology section on the Photobit website. The following information applies specifically to the Photobit PB-0100 CIF image sensor.

Format

The PB-0100 CIF image sensor is fabricated within the parameters of a 1/5-inch optical format. The diagonal of the image sensor array, 3.51 mm, fits most closely within the optical format corresponding to the 1/5-inch specification. Therefore, any imaging lens chosen should also satisfy this optical format criterion. For example, a lens with a 1/5-inch format will form an image that covers comfortably, but not excessively, an image sensor with a 1/5-inch format. Alternatively, a lens with less than a 1/5-inch format will form an image too small to adequately cover an image sensor with a 1/5-inch format, leaving the edges of the captured image cut off and under-utilizing the performance of the image sensor. Furthermore, a lens with greater than a 1/5-inch format will form an image that exceeds the area of an image sensor with a 1/5-inch format, thereby under-utilizing the performance of the lens.

Mounting

Several lens mounting standards exist that specify the threading of the lens' barrel as well as the distance the back flange of the lens should be from the image sensor for the lens to properly form an image. Typical lens mounting standards for the PB-0100 are:

Mount Name	Mounting Threads	Back-Flange-to-Image-Sensor
C	1 - 32	17.526 mm
CS	1 - 32	12.5 mm
S	M12x0.5	Unspecified
X	M10x0.5	Unspecified

Field of View and Focal Length

The field of view of an imaging system will depend on both the focal length of the imaging lens and the width of the image sensor. As most of the image information humans pay attention to generally falls within a 45-degree horizontal field of view, many camera systems attempt to imitate this field of view. However, in some cases a telephoto system (with a narrow field of view, say less than 20 degrees), or a wide angle system (with a wide field of view, say more than 60 degrees) may be desired. The approximate field of view that an imaging system can achieve is shown in the following equation:

$$\theta \approx 2\tan^{-1}\left(\frac{w}{2f}\right)$$

where q is the field of view, tan-1 is the trigonometric function arc-tangent, w is the width of the image sensor, and f is the focal length of the imaging lens. For example, the imaging system's diagonal field of view can be determined by using the diagonal of the image sensor (3.51 mm) for w and a particular lens' focal length for f. Alternatively, the imaging system's horizontal field of view can be determined by using the horizontal of the image sensor (2.81 mm) for w and a particular lens' focal length for f. A lens with an approximately 3.4 mm focal length will provide a 45-degree horizontal field of view with a PB-0100 (keep in mind that the above equation is a simplified approximation).

F-Number

The f-number, or f/#, of an imaging lens is the ratio of the lens' focal length to its open aperture diameter. Every doubling in f-number reduces the light to the sensor by a factor of four. For example, a lens set at f/1.4 lets in four times more light than that same lens when it is set at f/2.8. Low f-number lenses capture a lot of light for delivery to the image sensor, but also require careful focus. Higher f-number lenses capture less light for delivery to the image sensor, and do not require as much effort to bring the imaging system to focus. Low f-number lenses generally cost more than high f-number lenses of similar overall performance. Typical f-numbers for various imaging systems are:

F-#	Imaging application
1.4	Low-light level imaging, manual focus systems
2.0	Typical for PC and other small form cameras
2.8	Common in digital still cameras
4.0+	Often used in machine vision applications

Typical f-numbers will range from 1.8 to 2.8. For example, most S-mount lenses come with a fixed f-number of f/2.0.

MTF

Modulation Transfer Function (MTF) is a technical term that quantifies how well a particular system propagates information. For cameras, the "system" is the lens and the sensor, and the "information" is the picture they are capturing. MTF ranges from zero (no information gets through) to 100 (all information gets through), and is always specified in terms of information density. In most imaging systems, the MTF is limited by the performance of the imaging lens. A lens must be able to transfer enough information to the image sensor to be able to resolve details in the image that are as small as the pixels in the image sensor. The pixels are set on a 7.9-micron pitch (the center of one pixel is 7.9 microns from the center of its neighboring pixel). Thus, a lens used should be able to resolve image features as small as 7.9 microns. Typically, a lens' MTF is plotted as a function of the number of line pairs per millimeter the lens is attempting to resolve (more line pairs per millimeter mean higher information densities). For an electronic imaging system, one line pair will correspond to two image sensor pixels (each pixel can resolve one line). This is equated as:

$$LP/mm = \frac{1}{2z}$$

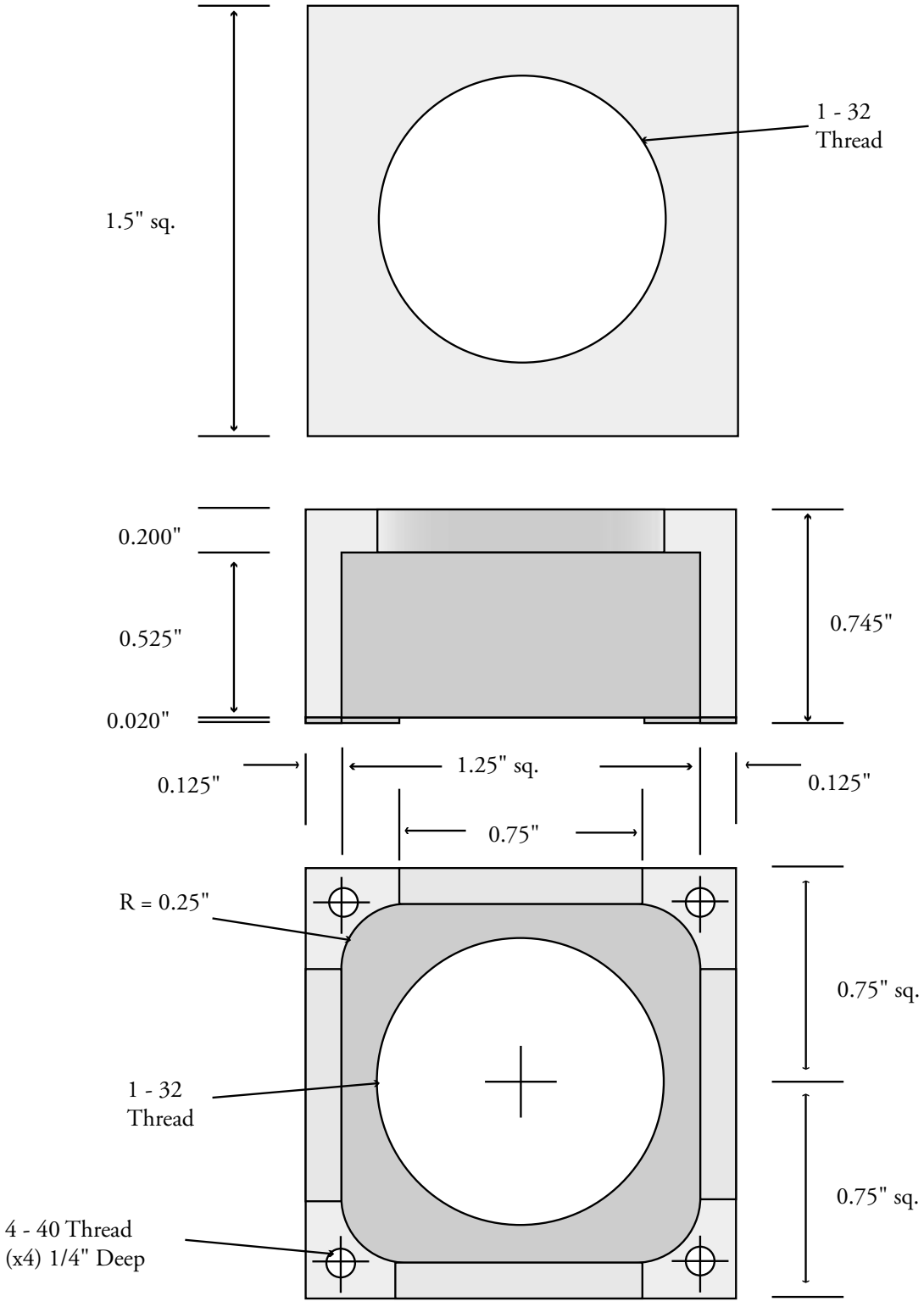
where LP/mm means line pairs per millimeter and z is the image sensor's pixel pitch, in millimeters. For the PB-0100, z = 0.0079 mm, such that the PB-0100 has 63 LP/mm. Thus, a lens should provide an acceptable level of MTF all the way out to 63 LP/mm. For most lenses, the MTF will be highest in the center of the images they form, and gradually drop off toward the edges of the images they form. As well, MTFs at low values of LP/mm will generally be larger than MTFs at high values of LP/mm. One of the many trade-offs that must be decided by the end user is how high the MTF needs to be for a particular imaging situation. Generally, near an image sensor's LP/mm good MTFs are higher than 40, moderate MTFs are from 20 to 40, and poor MTFs are less than 20.

Infrared Cut-Off Filters

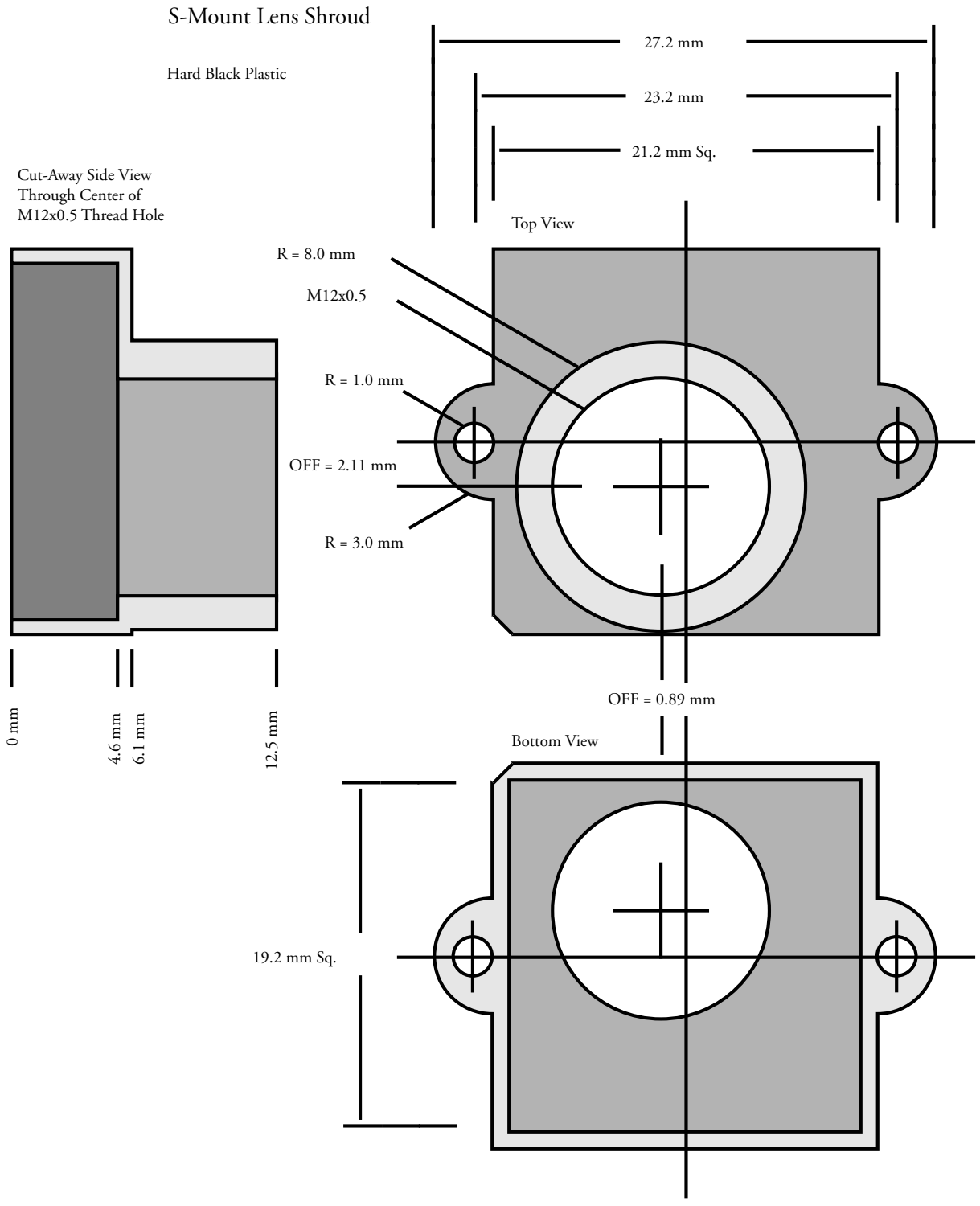
In most visible imaging situations it is necessary to include a filter in the imaging path that blocks infrared (IR) light from reaching the image sensor. This filter is called an IR cut-off filter. Various forms of IR cut-off filters are available, some absorptive (like Hoya's CM500 or Schott's BG18) and some reflective (i.e., dielectric stacks). Infrared light poses a problem to visible imaging because its presence blurs and decreases the MTF in the images formed by a lens. Since human vision only extends across a narrow range of the electromagnetic spectrum, camera systems hoping to capture images that look like the images our eyes capture must not capture light outside of our vision range. Silicon-based light detectors (like the ones in the PB-0100's pixels) detect light from the very deep blue to the near infrared. Thus, a filter must exist in the light's path that keeps the infrared from reaching the image sensor's pixels. In most cases, it is important that such a filter begin blocking light around 650 nm (in the deep red) and continue blocking it until at least 1100 nm (in the near IR). In most camera systems, the IR cut-off filter is included in the imaging lens. However, this point must be verified by a lens vendor when a particular lens is chosen for use with an image sensor.

3.4 Lens Selection (continued)

C-Mount Lens Shroud



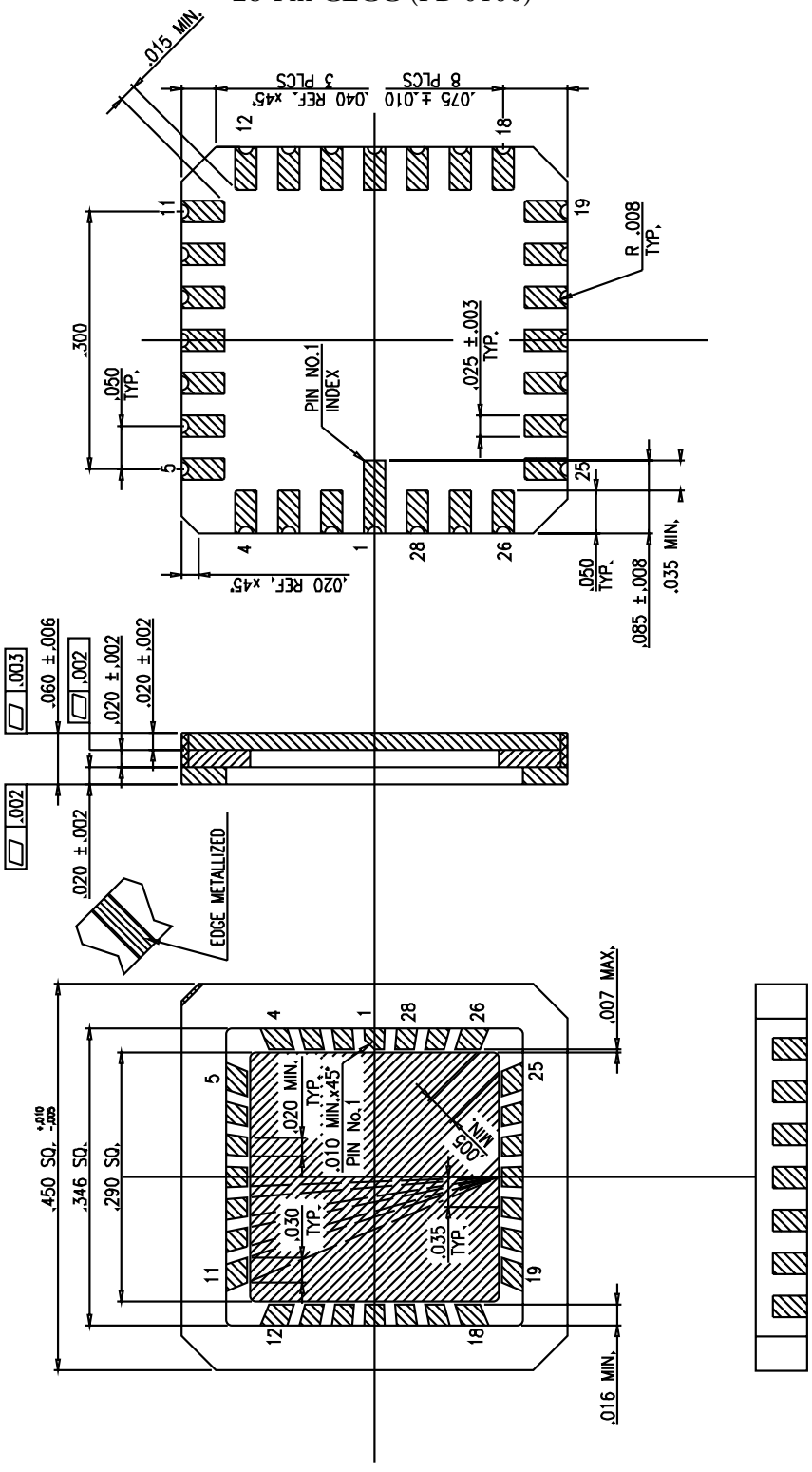
3.4 Lens Selection (continued)



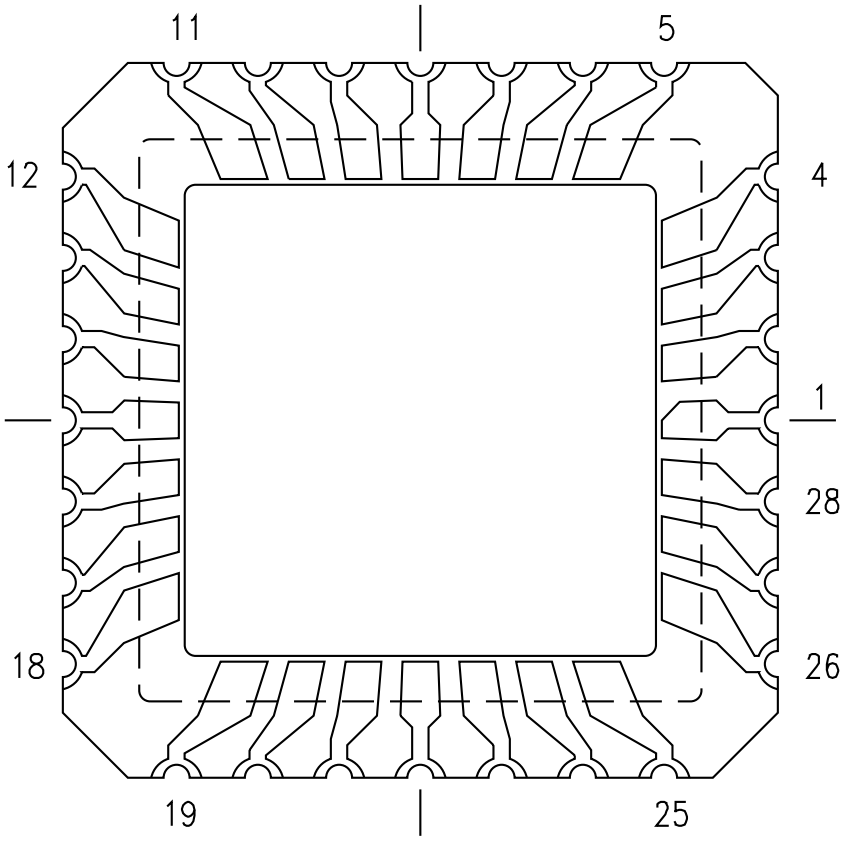
4.0 Mechanical

4.1 Package Views

28-Pin CLCC (PB-0100)

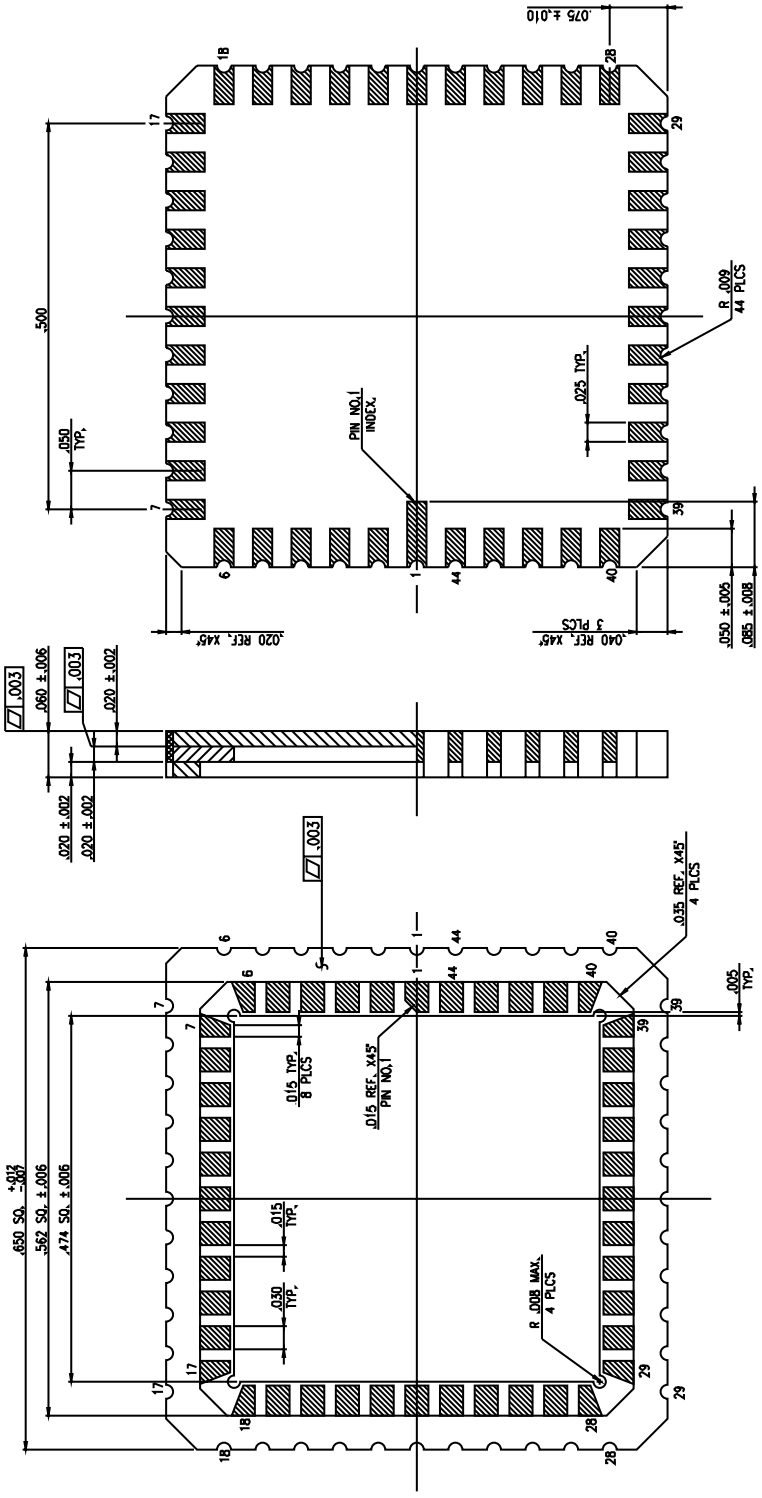


28-Pin CLCC (PB-0100)
Internal Package Routing



4.1 Package Views (continued)

44-Pin CLCC (PB-0101)



5.0 Environmental

Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
Tstorage	Storage Temperature Range	-40 to +125	C
TLead	Lead Temperature (10 second soldering)	300	C
RthetaJA	Package to junction thermal resistance	100	C/W
Humidity	Maximum humidity exposure@ 85C and 100 hours	85	%
Shock	Maximum acceleration	500	g
Vibration	Peak acceleration for frequency range from 20 Hz to 20KHz and 48 minutes	2	g