

How to implement a digital oscilloscope in Structured ASIC fabric

By Mircea Moldovan, Dan Nicula, and Traian Tulbure, eASIC Corporation

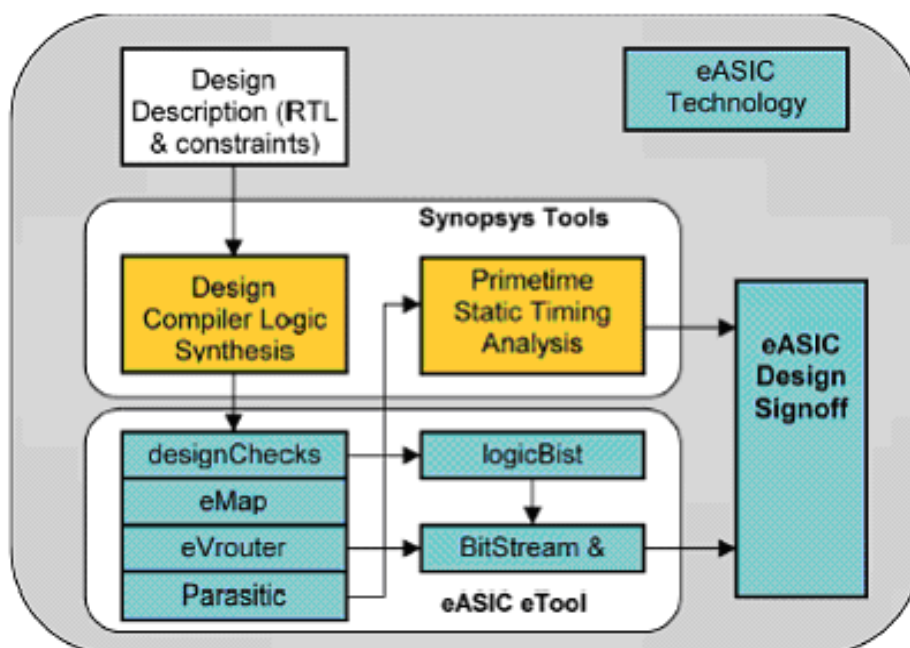
Page 3 of 3

[Programmable Logic DesignLine](#)

(07/12/2006 7:07 PM EDT)

Implementing the eScope on eASIC's Programmable ASIC fabric

The eTool design flow used for this implementation is illustrated in Fig 9 and is based on ASIC design tools for a standard cell design. This tool flow leverages existing ASIC design methodology and infrastructure as much as possible.



9. The eTool design flow.

Logic synthesis was performed with the Synopsys Design Compiler synthesis tool using eASIC's Liberty-format synthesis library containing all of the two, three, four, and five input functions that can be implemented with combinations of LUT configurations in the eCell, as well as the inverting buffer models and a number of DesignWare components that have been optimally implemented in the eCell logic.

The netlist produced by Design Compiler is passed through the eASIC-developed "technology mapping and packing" tool (called eMap) that replaces the slower LUT-based functions with faster nand and mux functions where possible, and then packs multiple functions into a single eCell where possible. The netlist created by eMap was characterized with standard wire-load models before place and route for use with the Synopsys Primetime static timing analysis.

The results from the implementation of eScope on eASIC's Structured ASIC fabric using the Synopsys tools as described above are reflected in Fig 10.

| Clocks | Synthesis (ns) | Mapping (ns) | Place & Route (ns) |
|----------------|----------------|--------------|--------------------|
| system | 3.95 | 4.72 | 7.53 |
| wave generator | 3.00 | 4.43 | 5.42 |
| host interface | 26.37 | 28.97 | 35.62 |

| Synthesis (eCells) | Mapping (eCells) | Place & Route (eCells) |
|--------------------|------------------|------------------------|
| 5945 | 3923 | 3923 |

10. eScope implementation timing and area results.

The back-end design flow uses eASIC's eMap and eVrouter tools to implement the final place and route. Parasitic extraction was performed to annotate the final netlist for back-end (signoff) static timing analysis using Primetime. In parallel, logicBIST (embedded BIST) test parameters are created and embedded into the final bitstream and Via Mask database. The bitstream assembly and the configuration via mask generation steps are performed using the eDK tools.

The graphical user interface (GUI)

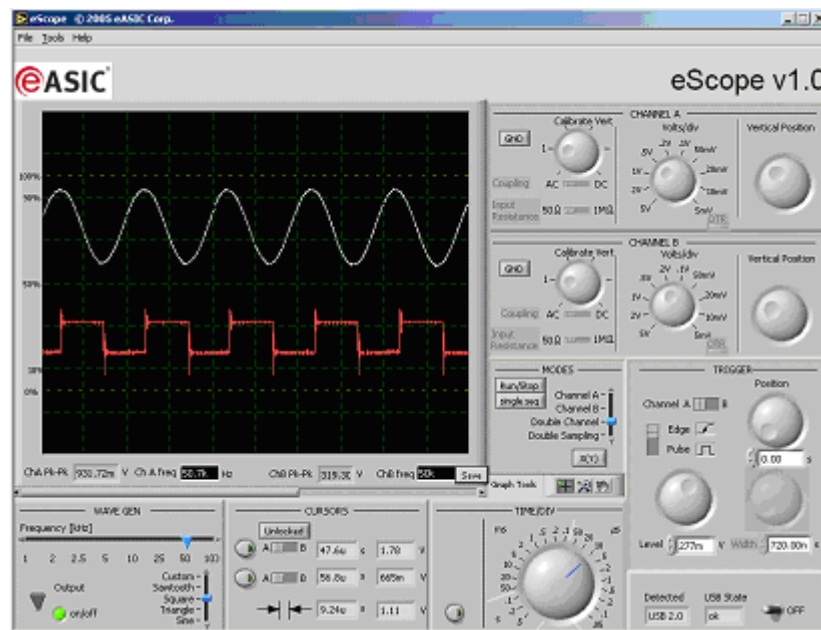
eScopeSW is a GUI application that controls the eScope hardware. It was developed as a LabVIEW "VI" using the LABVIEW development environment and C libraries. The USB interface is the physical medium used for data transfer between the eScope hardware and the PC running the eScope software. The communication between GUI and eScope device uses a 2-layer structure as follows:

- EZ-USB driver (written only for the Win32 platform).
- C high-level access functions that access the low-level driver's functions.
- The EZ-USB driver is responsible for data transfer between the software and the hardware modules. It provides low level functions that are used in the C libraries.

There are two kinds of C function:

- Low level functions (read/write samples/register values, connection status) that use the features implemented in the EZ-USB driver.
- High level functions that the driver. These functions are called by the LabVIEW application when an operation accessing the hardware module is done.

A screen shot of the eScope GUI application is shown in Fig 11.



11. The eScope GUI application.

Graphical objects include controls and indicators. The controls are divided into Boolean controls (push-buttons), toggle buttons, horizontal switches and numerical controls: horizontal and vertical sliders with multiple values. The indicators are divided into numerical, text indicators, leds, and graphical waveform indicators. The controls and the indicators from the front panel are grouped by function as might be found on a traditional desktop oscilloscope.

Summary

eScope was developed as a reference design to be used in a tutorial for the eASIC design tool flow and to demonstrated the technology advantages of eASIC's innovative Programmable ASIC fabric for high-speed logic design. In addition, eScope demonstrates that high-speed, low-cost products can be created using programmable-ASIC technology from [eASIC Corp.](http://www.easic.com)

References

1. eScope design specification, eASIC Corp.
2. "OCP-based memory access arbitration for a digital sampling oscilloscope", by Traian Tulbure and Dan Nicula, 2005, [Programmable Logic DesignLine](#).
3. The www.ocpip.org website.
4. The PC Oscilloscope section on the www.oscilloscopeguide.com website.
5. "Oscilloscopes," Fifth Edition by Ian Hickman – Reed Educational and Professional Publishing Ltd 2001. ISBN 0 7506 47574
6. Tektronix TDS5000B Series Digital Phosphor Oscilloscopes Quick Start Manual 071-1355-02 by [Tektronix Inc.](#)

Dr. D. NICULA is a professor at Transilvania University in Brasov, Romania, Department of Electronics and Computers. He graduated the Polytechnic Institute of Bucharest, Romania, in 1990 with a MSc degree in Electronics. In 1997 he was awarded the PhD in Computer Sciences by Transilvania University. His research interests are mainly in the area of VLSI design and HDL RTL level modelling. Teaching duties include HDLs, microprocessors and digital electronics. He is author of Romanian books regarding VHDL and Verilog. He is leading the R&D team of Romanian eASIC Corporation subsidiary.



Traian Tulbure is a lecturer and Ph.D. candidate at Transilvania University of Brasov. He graduated from Transilvania University in Brasov, Romania, Department of Electronics and Computers, in 2000 with MSc degree in Electronics and Computers. His graduation thesis was entitled: "EDA tools for eASIC technology." His research interests are in the area of VLSI design, HDL modelling, C/C++ programming, and synthesis. Traian can be reached at traian@easic.ro.



Mircea Moldovan is a system engineer at eASIC Corporation. He is also a student at Transilvania University in Brasov, Romania, Department of Electronics and Computers, for obtaining a MSc degree in digital communication networks. He graduated from Transilvania University in Brasov, Romania, Department of Electronics and Computers, in 2005 with BSc degree in Electronics and Computers. His graduation thesis was entitled: "eScope - Digital Sampling Oscilloscope on a Chip." His research interests are VLSI design, HDL modelling, C/C++ programming and synthesis. Mircea can be reached at mircea@easic.ro.

