SOI DRAM Process Integration and Data Retention Schemes

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Abstract: *The paper focuses on the design of SOI DRAM by different processing technology and corresponding process sequence has been explored. Later since data refresh and retention is the key to DRAM's functioning therefore along with the problems related to refresh and retention being discussed, different schemes used to improve the retention characteristics are also being presented both at the process and device level. The corresponding change in the DRAM operation is also looked around.*

Introduction

SOI has received wide attention for the future high density DRAM as a substitution of bulk-Si due to the feasibility of simple cell capacitor cell fabrication, reduced parasitic junction capacitance, easy shallow junction formation, good soft error-rate immunity, suppression of short channel effect and body effect, latch up free and improvement of data retention time. Whereas some of the problems which needs to be solved carefully while designing DRAM's with SOI are Floating Body Effects (FBE) which causes degradation of S/D breakdown voltage (BVDS). I_d-V_d including Kink. Increase of S/D parasitic resistance is another such problem.

For future ULSI DRAM's several new circuit techniques and memory cell structures are proposed for high performance both as core and embedded applications. Regarding the memory cell structure, only how to enlarge the memory cell capacitance in smaller area is an issue, so as to realize higher soft error immunity, long data retention characteristics and high read out signal amplitude.

I -Device fabrication

A) Scalable SOI DRAM with SOC[1]:

Fig.1 shows layout of SOI DRAM cells with SOCs (Silicon on Capacitor) PBSOI (Pattern Based SOI) process. LOCOS is used as the stopper for the silicon CMP for SOI layer thickness to be small. Isolation is formed by both stopper and 0.2 μm STI processes. Process sequence is shown in Fig.2. Because capacitors are under active layer in the SOC structure, it is not possible for the buried contacts to overlap gate and bit line. It makes the overall accuracy window wide and good shrinkability. Fully planarized interconnection process is realized with bit line damascene process.

As tungsten is used for the bit line material, very low bit line resistance (~1.5ohm/sq.) can be acquired. For interconnection the double metal process including the reliable aluminum (Al.) reflow technique is used. For FBE local implantation post field oxidation (LIF) process is introduced after STI formation (B, 2e13/cm^2, 60 KeV) and boron is implanted after spacer as halo (B, 2e13/cm^2, 40 KeV, 7 KeV, 7 degree) for improving the FBE of peripheral transistors (Fig.3). Fig.4 shows the V_t distribution of both transistors. Uniform V_{th} indicates that the SOI layer thickness is uniform.

B) RSTC using Bonding Process[2].

Reverse Stacked Capacitor Cells (RSTC) for DRAMs where a storage capacitor and MOSFET are reversed are made using CMP and bonded SOI technology. Fig.5 shows the structure of RSTC DRAM's. Bit-line and metal surface on the metal wiring on a flat surface is realized by reversing both the MOSFETs and storage capacitor with bonded SOI technology. Bit-line and metal wiring are easily made on the flat surfaces with low aspect ratio for both memory cell-array and peripheral-circuit regions. Key process steps are as shown in the Fig. 6. Firstly the surface is polished after both the MOSFET and the storage capacitor are fabricated. The supporting surface is bonded to the surface. Then virtual flat surface at the bottom of the MOSFET is brought in a real surface by reversing the polishing process. LOCOS SiO_2 is utilized as a stopper for polishing. Original bulk MOS are turned to bonded SOI MOS thermally oxidized and CVD oxide is then deposited on it. Contact holes are opened and TiN/Ti bit lines are formed. CVD oxide is deposited again and Al. metalization is carried out.

C) SOI DRAM using Smart Cut technology[3].

Smart cut technology is based on ion implantation and wafer bonding technologies. Here after the storage capacitors and the MOS devices are built, a hydrogen implant is initiated followed by the wafer bonding and splitting (Fig. 7). Using the smart cut SOI technology can substantially reduce Grinding and CMP times and the split wafer can be reused.

D) Fabrication Using SIMOX wafers[4].

SOI DRAM using SIMOX wafer are made have Si film and buried oxide thickness of 100-160nm and 400nm respectively. The silicon films are thinned down by thermal oxidation and wet etching before capacitor cells are fabricated using LOCOS isolation. To adjust V_t p^+ poly and n^+ poly silicon gates are used for n type and P type memory cells, respectively. An ONO film (t_{eff} = 12nm) was adapted as the gate insulator for both cell transistors. An LDD structure with the sidewall spacer of 200nm is used for the NMOS cell transistors while a conventional drain structure was used for the PMOS one. After depositing CVD-oxide film on these cell transistors, the storage node contact nodes are opened. A 1st poly-silicon film is deposited as the storage electrode. After forming an ONO dielectric film (t_{eff}=5nm) on the 1st poly a 2nd poly film is deposited and patterned by RIE to define the top cell plate. After depositing a CVD-oxide film on these capacitors, the bit-line contacts and the bit lines are fabricated. The measured cell capacitance is ~25fF/cell. With improvements in technology the capacitance can be further brought down.

II-Data refresh and retention Scheme

Required minimum data retention times becomes longer and longer with the rapid progress of the DRAM generation increasing the data retention time is a major factor in realizing the higher density DRAM's. Since the retention time strongly depends on the leakage transistor of the leakage current of the cell transistor, the off-state leakage current may be greatly reduced for higher density DRAMs. Data retention time increases remarkably by using the thin SOI substrates because of the reduction in the area of p-n junctions of the cell transistor.

Data stored on a memory cell slowly degrades due to various leakages. Since DRAM can only retain stored information periodically reading and re-writing the data (refresh) before the data is corrupted. The cell refresh time requirements has increased from 2ms for 64k DRAM to 128ms for 64MB DRAM. The SOI body is tied down in circuits like the sense amplifier to avoid variability in the body voltage and contribute more leakage, and to ensure accurate sensing. There are two types of data retention techniques.

1. Static Data retention

Common leakage mechanisms that affect charge storage in static data retention schemes are Junction Leakage; Pass transistor sub-threshold leakage; leakage through capacitor dielectric and other parasitic leakage paths. Fig.10 shows the retention time of NMOS/SIMOX[5] as a function of the source voltage of the cell transistor for different memory cells. In static operation condition, the source voltage (V_{IL}) is equal to bit-line voltage of 1.5V. Thus this figure clearly shows that retention time of SIMOX wafers are much longer then that of the bulk ones. It decreases suddenly at V_{IL}=0 which corresponds to dynamic operation conditions, resulting in a much shorter retention time then that of the bulk one. The result can be attributed to a slight increase in the sub-threshold current at V_{gs}=0V. Single latch phenomenon is not responsible for this result.

2. Dynamic Data Retention

Here the bit line capacitance of a selected cell swing from high to low (V_{dd} to GND), increasing V_{gs} of the cell transistor, thus causing sub-threshold leakage. Body potential rises as a result of hole injection/redistribution (fig. 9) and capacitive coupling reducing V_t and degrading sub-threshold leakage. A particularly severe case is when dynamic data retention occurs after long static data retention. The leakage current charges over a period of time, and enables dynamic data retention. Body contact (like in Logic) is not an option due to tighter cell density. Following are some of the schemes to improve the dynamic data retention characteristics.

A) Process modifications LDD[6]

Lightly doped S/D region, which is composed of n^- & n+ regions, gives rise to effectively increased BVDs because of the low current gain of parasitic current gain of parasitic BJT and the less impact ionization rate near the drain, although the drive current and contact resistance are degraded. Use of pMOS cell transistor is also an option at process level.

B) Boosted Sense Ground (BSG)[7]

Here a low bit line level is raised above the unselected wordline level to suppress subthreshold leakage thus improving dynamic retention time. Fig.11 shows the BSG circuit. V_{ref} is set to 0.5V. As the current mirror amplifier is made inactive in the standby state, standby current doesn't increase and the BSG level (VBSG) level is clamped by the n-channel transistor(Q3). To suppress unnecessary rise of VBSG from the sensing current of the bitline, a large n-channel transistor (Q2) is turned on at the beginning of sensing. As the ground line for the supply charge to the BSG line is fully separated from ground lines, current flow through Q2 doesn't affect other circuits.

C) Body Refresh Mechanism[8]

It gives stable body potential, long dynamic data retention time and low power consumption. Body refresh function is to remove the accumulated holes from the body region by utilizing the forward bias of P-N junction. After "H" data (2.5 V) is stored in the cell, the gate voltage is pulled down to 0v (for~20ns), and the bit line maintains the half V_{cc} level (1.5V) in the static retention period. BSG of 0.5V is assumed to be present for the "L" level of the bit line. The body potential increases due to the junction leakage as shown in fig.12 (a). Thus the bit line goes to 0V, the accumulated holes are removed out of the body region to the bit line and the body potential decreases and becomes stable as shown in Fig.12 (b). At the start time of body refresh, although an e-current density of about 140 A/cm^2 flows from the memory as the sub-threshold leakage current, a decrease in high stored high data is only 0.04V. Thus there is no danger destroying the stored data with the body refresh function. The simulated potential and e-current density plots are shown in fig.13.

Discussion and Conclusion

Although many of the processing sequences for SOI DRAM devices have been studied looking towards today's increasing demand of high density, low power and high data retention scheme needs to be chosen for future ULSI applications. Bonding as well as other technologies such as SIMOX and Smart Cut are the possible ones for SOI DRAM fabrication at large volumes depending upon the requirements (like Embedded DRAM's) one needs to choose correct process sequence. Other issues relating to data retention needs to solved by one or more methods of increasing the data retention times. Even the allowed soft error immunity and Sense amplifier operation also needs to be correctly taken care of.

References

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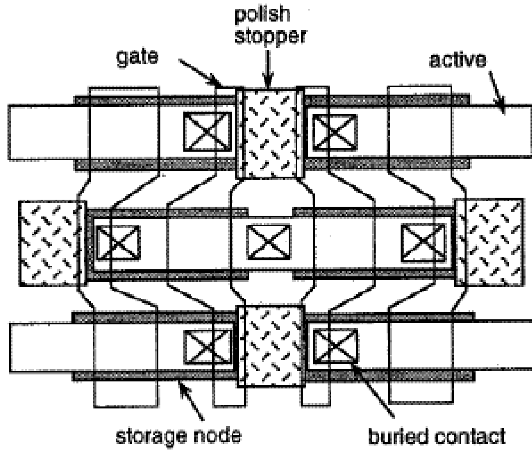


Fig. 1 Layout of SOI DRAM with SOC using PDSOI[1]

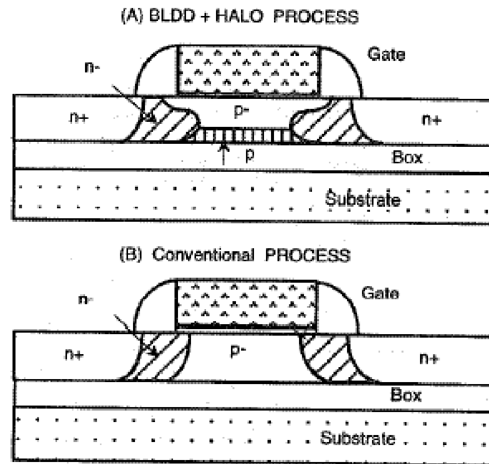


Fig.3 Schematic diagram of NMOS peripheral transistors[1].

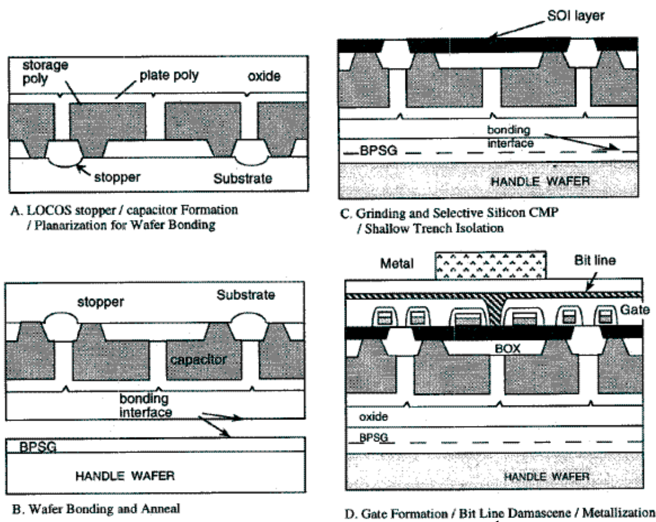


Fig.2(a). Process sequence of SOI DRAM cell[1].

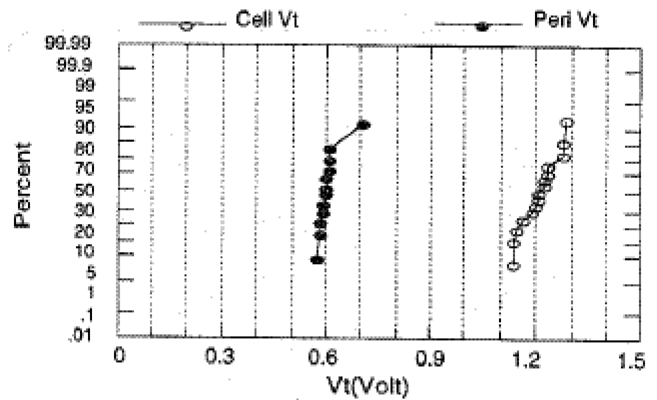


Fig.4 V_t distributions of cell and peripheral transistors[1].

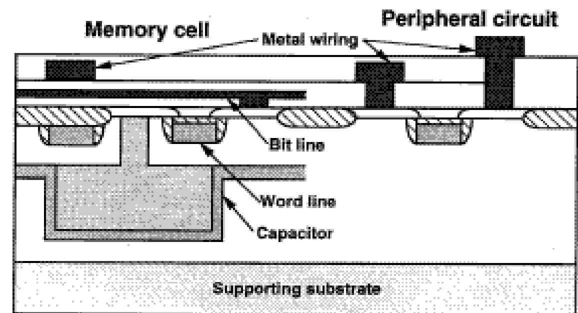


Fig.5 Bit Line and Metal wiring formation scheme[2]

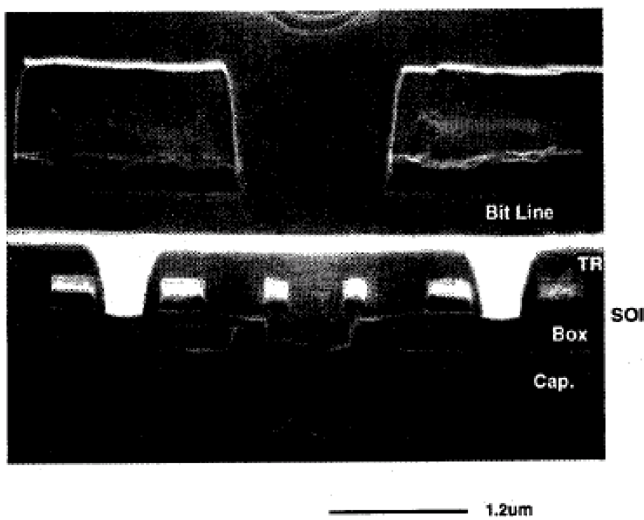


Fig.2(b) SEM picture of the vertical structure of SOI DRAM cell

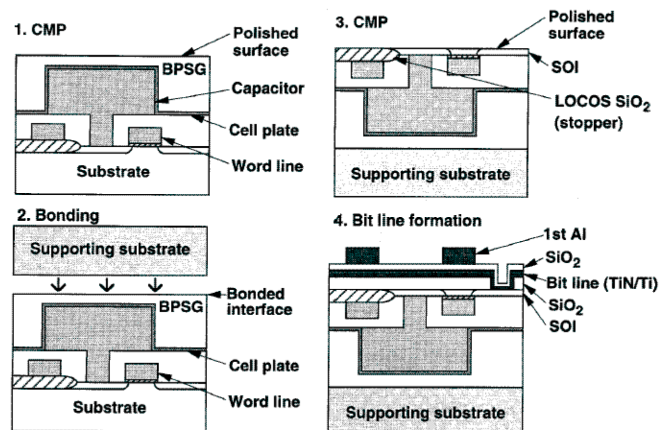


Fig.6 Process sequence for alternative method[2].

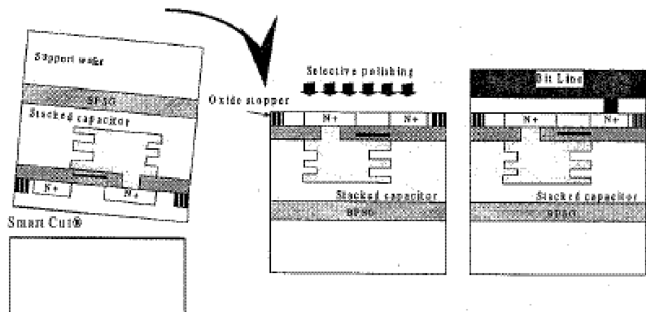


Fig. 12 *Application of Smart Cut to DRAM buried capacitor structure.*

Fig. 7 Smart Cut DRAM buried capacitor structure[3].

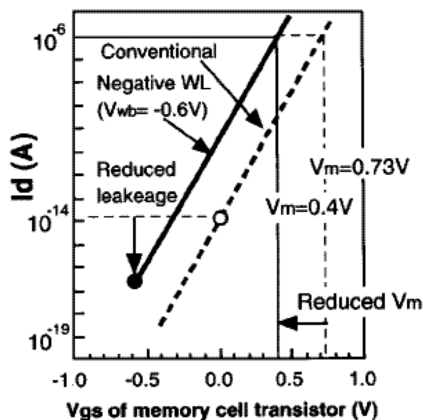


Fig.8 Subthreshold characteristic of memory-cell transistor[9].

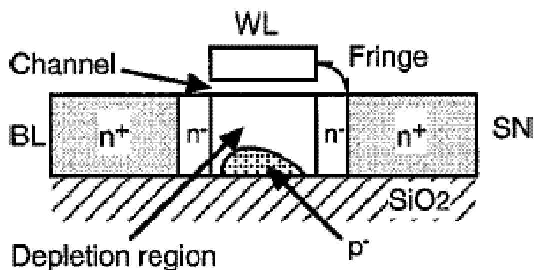


Fig. 9. Cross-sectional view of the memory-cell transistor[9].

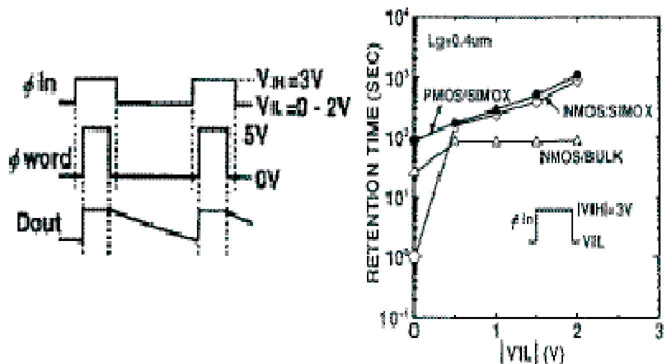


Fig.10 Retention time as function of source volt[5].

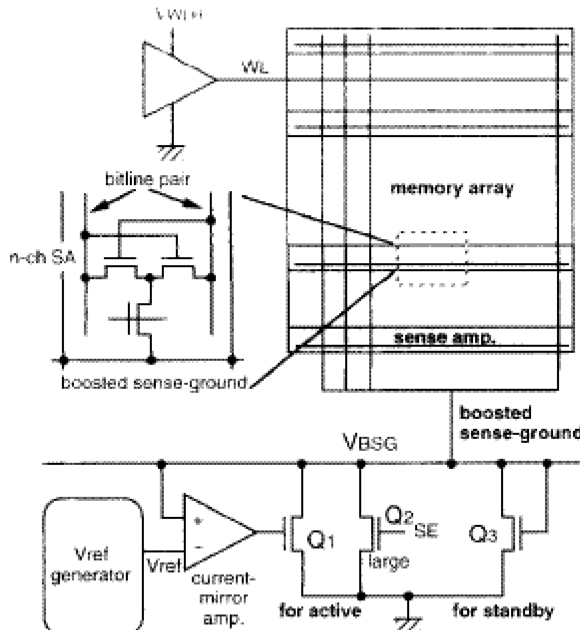


Fig.11 Circuit of boosted sense-ground[7].
SE is enabled at the beginning of sensing

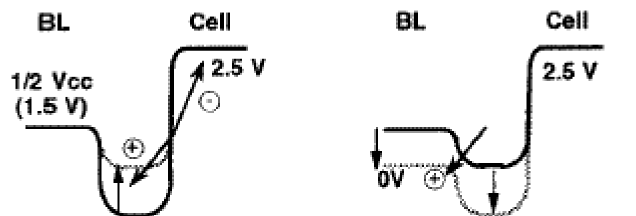
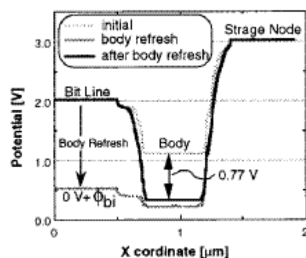


Fig.11 Model potential of SOI DRAM cell[8].



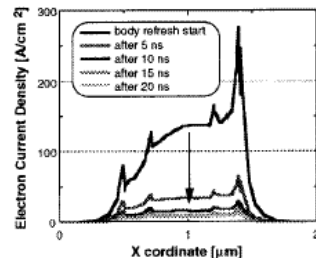


Fig. 12(a) Simulated potential (b) Simulated e-current density[8]

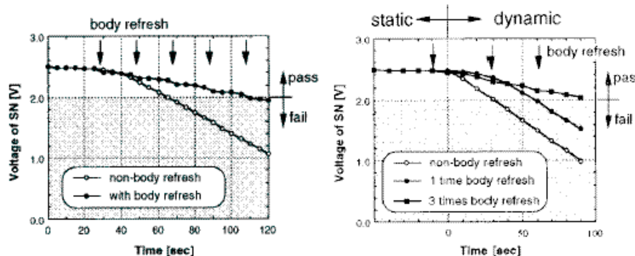


Fig.13 (a) Estimated Dyn. Data Retention (b) Estimated data retention at worst case[8]