A Design Report in
MR-201 Thin Films and Devices: Science and Engineering
On

High-k Dielectric for Gate insulators in IC's

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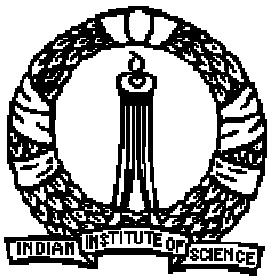

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Contents

1. Abstract

Dielectric materials used for Gate oxide and intermetallic insulation in modern VLSI process has been discussed along with their properties and manufacturing techniques in the process flow. The techniques are basically divided into two classes, firstly thermal oxidation technique (higher temperatures) for small and accurate thickness and high purity of layers. This technique has two variations wet (fast) and dry (slow) oxidation methods. Secondly the deposition technique for comparatively large thickness (comparatively lower temperatures) these includes Physical and Chemical (atmospheric, low pressure and PlasmaEnhaced) means of vapor deposition. New variant in deposition technique called Ozone CVD is also discussed in detail as a case study. Some design and process compatibility related issues are discussed. Finally Current challenges in dielectrics with scaling of transistor, the materials and processes to be used for the modern High-κ dielectrics for Gate insulator and Low-κ dielectrics for metal interconnects are also discussed.

2. Introduction

The first Integrated circuit (IC) was made by Jack Kilby in 1958. It consisted of one transistor, three resistors, and one capacitor, all made of germanium and connected by wire bonding. Today several million transistors are incorporated on one IC and the transistor size is less than 1 μm. This explosive development has, up to now, followed the law formulated by Moore, which states that a doubling of the number of components on an IC takes place every second year. As the number of components on the IC has increased, the size has decreased correspondingly, and transistors with a size down to 0.1 μm can be manufactured today. The insulating Dielectric layer used in the transistor has decreased from 100 nm in the early 1970s to only a few nanometers today.

Dielectric Layers is one of the major crucial constituents in today's VLSI technology. The materials used for the Dielectrics are highly selective and the manufacturing techniques used for making these thin films are also very sophisticated today.

Most critical application of Dielectric layers as insulators in CMOS VLSI technology are as Gate insulator. These layers are typically 2.25-5 nm thick in current state-of the-art-technology and are projected to be <1nm in another decade. These small dimension layers are invariably formed by thermal (wet or dry) oxidation. Thicker Dielectric Layers can also be deposited using APCVD or LPCVD techniques.

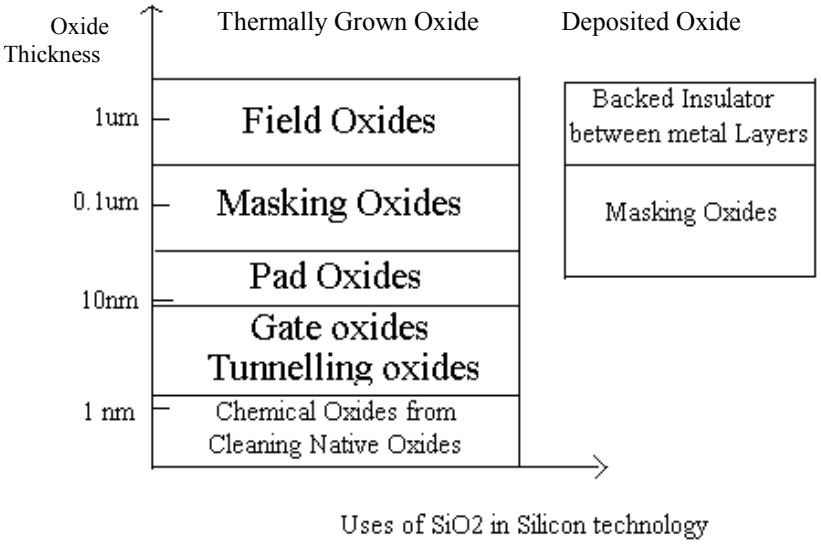
3. Materials used for Dielectric Layers and their properties

Many of materials are being searched and investigated for being used as Dielectric materials but for any material to be suitable as Dielectric layers, they must satisfy some critical properties such as high Dielectric strength and Dielectric constant, thermally and mechanically stable, low interface state, high purity, process fabrication and compatible etc. So the dielectric material needs to be chosen with great care. Earlier mainly SiO_2 was mainly used but with shrinking device sizes other dielectric materials are also under used today.

<u>Dielectric Applications in CMOS</u>

1. Gate oxide formation	→grown oxidation
2. Isolation (a. LOCOS b. Shallow Trench)	→Grown/Deposited
3.Intermetal Dielectric (for interconnects)	→Deposition
4. Implant Mask	→Grown/Deposited

Typical thickness of Dielectric Layers: The figure depicts thickness of various layers used in VLSI circuits.



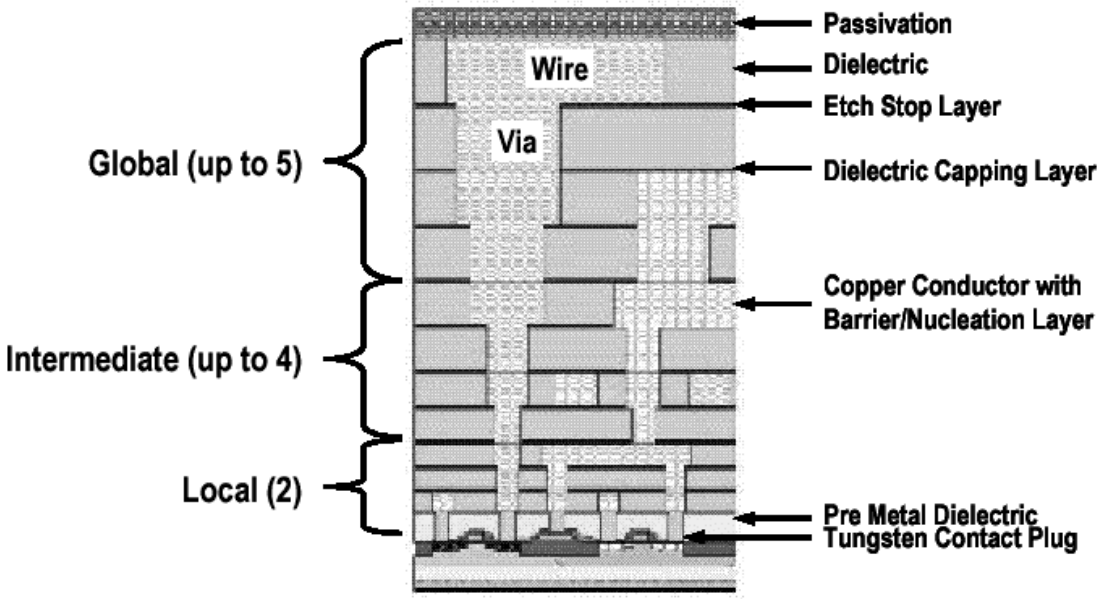


Fig. Showing use of Dielectrics in CMOS Transistor

a) Silicon Dioxide (SiO_2):

This is the most natural choice for using as a dielectric material since it has the properties that it is very good insulator against electric field, has very high dielectric strength. Its electrical and mechanical as well as those of layer itself are almost ideal. SiO_2 layers are easily grown thermally on silicon or deposited on other materials. They adhere well, block the diffusion of impurities, they are resistant to most of the chemicals used in the silicon processing and yet can be easily patterned and etched, they are excellent insulators, and they have stable and reproducible bulk properties. The interface that forms between Si and SiO_2 has very few electrical and mechanical defects and is stable over time. SiO_2 deposited is amorphous is nature

but has a short range order thus its Band gap is defined to be~9.01eV. Since it is most widely used material all of its characteristics are well defined and its limitations especially when the device sizes in IC are shrinking are also known.

b) Silicon Nitride (Si_3N_4):

This is used in at places where oxidation is not to be done. It acts as an mask during oxidation. Most common use of Si_3N_4 is in spacer formation in NMOS and PMOS transistor in CMOS technology in sub-micron devices to define shallow extension for gate lengths less than 0.5μm where short channel effect becomes very critical. To suppress this short channel effects shallow extension Implants are done.

c) Silicon OxyNitride (SiO_xN_y):

It is composed primarily of of SiO_2, with small % of nitrogen (<10%) of nitrogen at the silicon/dielectric interface. Boron diffusion through gate dielectric has recently been identified as a potential problem in dual doped poly-silicon-gate CMOS. Silicon OxyNitride are effective at preventing the diffusion of Boron from p-type polysilicon in the channel region. The blocking action results from the nitrogen rich layer at the interface. A disadvantage of using this is that the initial electrical char. Is inferior to that of pure SiO_2. Even its pure has higher densities of interface state (D_{it}) and positive charge (Q_F) than SiO_2. The fixed charges are introduced during the nitradation process, and can be minimised by subsequent annealing either during reoxidation or later in the process.

d) Zirconium Oxide ($Zi0_2$):

ZrO_2 is likely to replace SiO_2 as the gate dielectric material in metal-oxide-semiconductor devices for its high dielectric constant, good thermal stability on silicon, and large band gap. One atomic layer of ZrO_2 can be deposited after each alternating exposure to the precursor and oxygen, ideal for achieving conformal coverage of ZrO_2 over high aspect ratio features. Stoichiometric, uniform, and amorphous ZrO_2 can be obtained, and highly conformal step coverage of the deposited ZrO_2 can be observed.

The dielectric constant of ZrO_2 is high and ranges from 15 to 22 and is predicted to be thermodynamically stable, and large band gap (5–7 eV). Moreover, zirconium dioxide is the only thermodynamically stable (on silicon high breakdown field (~15–20 MV/cm)) solid form of zirconium with a simple fluorite structure. It may exist in either monoclinic (<1170 °C), tetragonal (1170–2370 °C), or cubic (2370–2680 °C) crystalline structures.

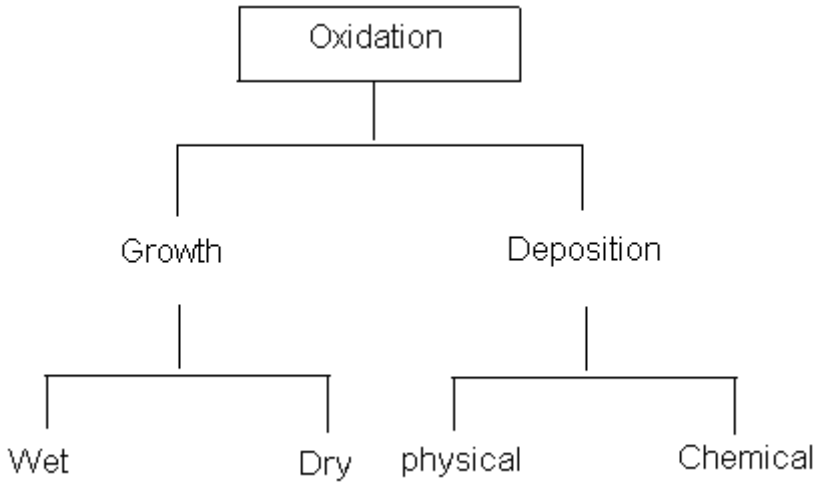
For metal-oxide-semiconductor field effect transistor (MOSFET) application, an amorphous ZrO_2 film is preferred to prevent the leakage current through the crystallite grain boundaries. As to its electrical property, zirconium oxide is oxygen deficient when nonstoichiometric, therefore the predominant defects have been proposed to be oxygen ion vacancies.

e) Other Alternatives

Potential high-*k* dielectric materials with a dielectric constant ranging from 10 to 100 include transition metal oxides (Ta_2O_5,TiO_2), Al_2O_3, ZrO_2, HfO_2, ferroelectric materials (e.g., $Pb(Zr,Ti)O_3$, $(Ba,Sr)TiO_3$), and silicates ($ZrSi_xO_y$, $HfSi_xO_y$). These materials also have applications in RF circuits and/or in dynamic random access memory (DRAM) devices.

4. Oxidation- Methods of formation of Dielectric layers in VLSI technology

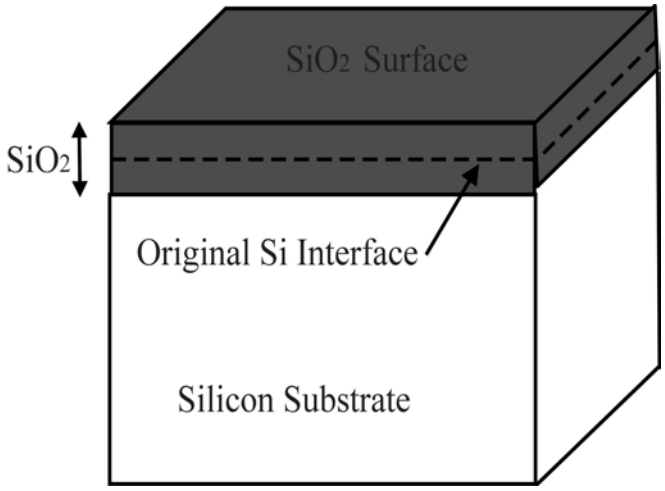
Since SiO_2 is mainly used as dielectric material for layer formation the process of Dielectric



layer is called more commonly as oxidation Fig. shows the most commonly used methods of Dielectric layers formation techniques This are mainly divided into two classes as thermal growth and Deposition.

5. Thermal Growth Techniques

It is Central to the production of bipolar and CMOS devices. A great advantage of Si over Ge and GaAs is that it can be oxidised to form a stable and passivating dielectric film. A silicon surface has a high affinity for oxygen.(An unterminated Si surface has unsaturated dangling bonds that are acceptor like in their effect at or near the surface, which can affect devices. The density of surface states can be reduced four or five orders of magnitude by oxidising the Si – electronic surface ***passivation***.)



Rapid thermal processing has been widely used in semiconductor manufacturing for thermal oxidation/nitridation, deposition, annealing, ultrashallow junction formation, silicide formation, and borophosphosilicate glass reflow.

An oxide can also be used as a ***mask*** to implantation and diffusion. An oxide can be used to electrically ***isolate*** different devices on the same chip Oxides ***doped*** with phosphorous, arsenic or boron can be used as diffusion sources. Two methods used most frequently

- Dry oxidation
- Wet oxidation

Wet oxidation occurs very fast and is used for thick oxide formation e.g. insulation whereas dry oxidation occurs comparatively slower and is used for thinner layers formation e.g. Gate formation.

Wet oxidation is limited by diffusion ofO_2 in SiO_2 whereas dry oxidation is limited by surface kinetics. Both these factors are enhanced at higher temperatures so oxidation rate is also high

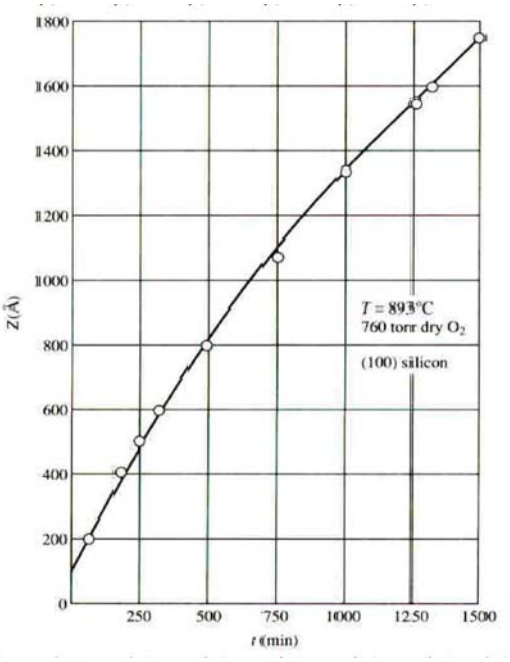
The Si wafer is heated in an oxidising environment. Only ultra-pure and *filtered* gases are used. The *rate* at which the wafers are heated and cooled is of considerable importance in reducing thermal stresses that can mechanically damage the wafer and devices on it. During oxidation the Si-SiO_2 interface moves into the Si. The resulting external surface expands resulting in the external surface not being coplanar with the original Si surface.

Oxidation proceeds as the oxidising species diffuses from the surface to the Si/SiO_2 interface and reacts with the underlying Si. Based on densities and molecular weights we can calculate that for an oxide thickness *d*, a layer of Si 0.44***d*** is "consumed". Due to this there is a compressive stress due to Volume mismatch since the fresh SiO_2 layer grows at Si-SiO_2 interface at and not at the top of SiO_2.

Furnace Processing for thermal oxidation

The traditional equipment for performing thermal oxidation is the horizontal furnace. The tube furnace consists of a long ceramic tube with resistive heaters separated into zones. Inside the furnace tube is a quartz reaction tube, which acts as the reaction chamber.

The reaction chamber provides a controlled ambient of reactive gases and seals out possible contaminants from the ambient. The quartz chamber wall also acts as a heatsink that distributes the heat more evenly. The quartz reaction tubes have a gas inlet end and a wafer load end. The load end has a precision ground fitting that caps the furnace.



High purity quartz is used due to its stability at high temperatures and its compatibility with contamination control. An alternative material to quartz is silicon carbide. Silicon carbide is structurally stronger than quartz and is more stable over temperature cycles. During thermal oxidation processes, silicon carbide tube develops a thin layer of silicon dioxide. When the oxide is removed in HF, the etch process is self limiting, stopping at the silicon carbide. This allows for an extended lifetime of silicon carbide tubes over repeated HF cleans. The primary disadvantage of SiC, however, is its cost.

One of the primary difficulties with furnace processing is maintaining temperature uniformity over large diameter wafers. When there are significant temperature gradients over the wafer, the wafers can warp. The problem of wafer warping increases with higher temperatures. One method of minimizing warping is by using a procedure called ramping. The furnace is maintained at a temperature several hundred degrees below the process temperature. The wafers are slowly inserted into the furnace at this lower temperature and after a short stabilization period, the temperature is ramped up to the setpoint. After the thermal treatment, the temperature is ramped down before the wafers are removed.

<u>Masking Properties of SiO_2:</u>

A silicon oxide can provide a selective mask against the diffusion of a dopant, even at higher temperatures. This is not just because the oxide can be made very thick, most commonly used n-type dopants P, Sb, and As, as well as p-type dopants B have very small diffusion coefficients in the oxide.

Oxide Charges: The Si/SiO_2 interface contains a region of transition between crystalline Si and amorphous silica. Various charges and traps are found in this region and are linked directly to the oxide. These can be due to:

- Structural imperfections (defects)
- Metallic impurities
- Mobile ionic charge from alkali ions eg sodium, lithium(Q_m)
- Oxide trapped charge (Q_{ot})
- Fixed oxide charge (Q_f)
- Interface trapped charges (Q_{it})

Any charges at this interface can induce an equal and opposite charge in the underlying Si. This is particularly a problem with MOS devices, which can suffer yield and reliability problems. A low temperature anneal (450°C) in hydrogen can effectively eliminate oxide interface charge. "Careful" processing can only reduce the other contributions.

A) Dry oxidation of Si

Most common method is to heat the Si wafer in an oxygen atmosphere at a temperature between 800 to 1200°C. The reaction can be represented by:

$$Si + O_2 \xrightarrow{heat} SiO_2$$

This reaction involves two steps:

- Diffusion through the surface layer to the interface
- Reaction at the interface

However, the diffusion time is typically four orders of magnitude less than the reaction time, so the process can be modelled as using simple kinetics. Special dedicated high purity quartz furnace furnaces are used, with heaters under computer control. These run continuously under an inert gas (such as N_2) to keep them clean. Manufacturers will often run many furnaces at different temperatures, and for different parts of the device process. This avoids the possibility of cross contamination.

Typical reaction times are given as

B) Wet Oxidation

This reaction proceeds according to

$$Si + 2H_2O \xrightarrow{heat} SiO_2 + 2H_2$$

"Wet" oxidation is carried out using water vapour (steam) as the reactive gas.

In fact water is vary rarely used as an oxidising agent because it is very hard to store pure water. Usually ultra-pure gases of O_2 and H_2 are added into the furnace, where they combine to form very pure steam. Wet oxidation proceeds much more rapidly than dry oxidation, but the electrical and structural properties are different.

Wet oxides tend to be porous and therefore have higher leakage currents than dry oxides. This is particularly important for gate oxides, such as in MOS devices. Sometimes we want thin oxides e.g. a gate oxide can be as thin as 0.5 nm. This would be very difficult to achieve using

a wet oxide. However, if we just need a thick “field” oxide for implant or diffusion masking then the wet oxide is well suited.

6. Deposition Techniques

The problem with wet and dry oxidation methods is that the temperature (800°C and above) is too high for some applications. In the tunnelling diode, for example, boron doped layers of less than 1 nm thick is crucial to the performance of the diode. As we shall see later, the thermal budget required to oxidise the sample would destroy the device by solid-state diffusion.

SiO_2 can be sputtered called physical deposition even at room temperature. However the Quality of SiO_2 and the interface is not good for both Physical and chemical Vapor Deposition. Here Si from the substrate is not consumed by any of these methods.

A) Physical Vapor Deposition (PVD)

Physical Vapor Deposition (also called sputtering) is a process technology in which molecules of conducting material (aluminum, titanium nitride, etc.) are "sputtered" from a target of pure material, then deposited on the wafer to create the conducting circuitry within the chip. It is possible to deposit oxides of titanium, zirconium, and aluminum by PVD, but not easy. The problem is that the one tends to oxidize the deposition system as well. If sputtering, the rate of deposition is dramatically lower if the target gets oxidized. So this technique is not commonly used in CMOS VLSI technology for dielectric layer formation. It finds application in processes such as Poly-Silicon Thin Film Transistor Technology where the substrate is itself poly-crystalline Si.

B) Chemical Vapor Deposition

The use of chemical vapor deposition for various insulator films is paramount in the fabrication of semiconductor devices. The initial use of such films for passivation led to the development of low temperature techniques for film deposition. With the availability of silane, the pyrlosis of silane in the presence of oxygen at atmospheric pressure provided the deposition mechanism.

Further enhancements in the film characteristics through the use of phosphorous as a dopant within the film allowed the film to provide gattering of impurities during wafer fabrication. This lead to the need of smoothing the films, now known as reflow to minimize the sharp corners that the metal lines had to cover. Reflow is further enhanced by the addition of Boron as a dopant. The technology continues to be used for better implantations of reflow processes.

For more than a single metal layer, dielectric films are required for electrical isolation. These dielectrics are deposited at temp. below 400 ^{o}C to prevent affecting the underlying metal layer. Initially, using silane at atoms. Press., suitable films could be formed. With the advent of plasma enhanced film deposition enabled or improved dense film deposition. Low freq. Power during deposition improved both the film deposition process and film properties.

Now other reactants in the form of liquid precursors have been developed to provide better step coverage. At high temperatures (>650 C) TEOS (tetrathylorthosilicate) is used as a precursors in plasma Enhanced Deposition and for atmospheric pressure deposition with ozone. At technologies with 0.1 μm linewidths and gaps, better gap filling capabilites are needed and, as much as possible, dielectric films need an in-situ flow characteristics.

(I) APCVD:- Atmospheric Pressure CVD refers to systems whose deposition environments operate at or near atmospheric pressure. Typically, wafers are placed horizontally on belt-driven flat susceptors, which move through the deposition zone. Belt speed and gas flow determine the film thickness. Temperature range is 400 C and grew films in the 200-300 nm. The resulting films have suitable electrical dielectrical characteristics but due to gas phase reactions the step coverage is poor which causes "Bird Loafing" as the film becomes thicker.

The reaction takes place in a "mass transport limited" regime, careful design of the reactant supply system is required to prevent from taking place within the gas dispersion plumbing. Deposition uniformity is sensitive to the uniform availability of reactants and exhaust of resulting by-products.

(II) Low Pressure CVD

The LPCVD system has four tubes for the deposition of various thin films, including silicon nitride, polycrystalline silicon, and low temperature oxide (LTO). Si_3N_4 is deposited at ~800C and low pressure (~250 mtorr) using dichlorosilane ($SiCl_2H_2$) and ammonia (NH_3). The deposition rate is 30 – 60 Å/min for 4 inch wafers. A bare Si wafer is included in a batch to measure the deposited Si_3N_4 film thickness and film stress. Polycrystalline silicon (or poly-Si) is deposited at a low pressure (~200 mtorr) using silane (SiH_4).

The tube has a sloping temperature profile. Deposition temperature is ~620 ^{0}C for polysilicon and ~560C for amorphous silicon. The deposition rate for poly silicon is 40 – 160 Å/min for 4 inch wafers. Silicon dioxide (SiO_2) is deposited at between 300C and 400C, at low pressure (150 - 350 mtorr), from silane and oxygen with or without phosphine doping. Doped LTO is also called PSG, or phosphosilicate glass. The oxide deposition rate is mostly dependent on the temperature and is ~175Å/min at 400C for 4 inch wafers.

(III) Thermal CVD of Silicon Nitride

Thermal silicon nitride is generally produced using a tube reactor operating at low pressures. Dichlorosilane $SiCl_2H_2$ is a common precursor, with silane also being used. The oxidant is ammonia. Typical conditions are between 700 and 800 C, at around 1 Torr; deposition rates are in the 10 nm/minute range, but many applications employ very thin films, so throughput is reasonable in batch processing.

The resulting films are dense and hard, and also highly stressed: 10^{10} dynes/cm^2 is typical. The films are excellent barriers to just about everything, including hydrogen, although 4-8 atomic % H is generally incorporated. By varying the gas mixture, silicon-rich films can be produced. Conformality of the deposition is significantly better than e.g. silane oxides.

Hydrogen-free silicon nitride is nearly impervious to wet hydrofluoric acid (HF); thermal CVD films etch very slowly. Nitride films etch readily in fluorine-containing plasmas, and can be selectively etched with respect to silicon using hot (>150 C) phosphoric acid.
The deposition process tends to produce copious amounts of powder in the exhaust system, in part due to the formation of NH_4Cl (essentially an adduct of hydrochloric acid HCl and ammonia NH_3).

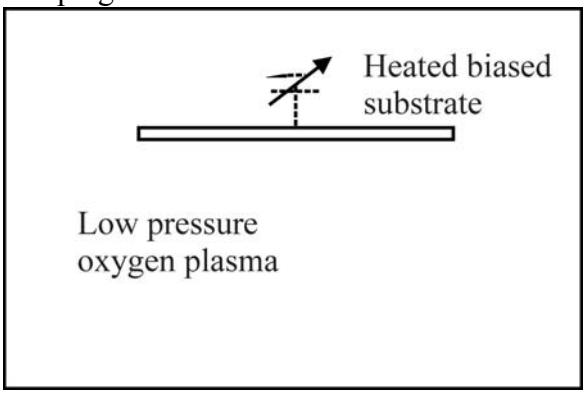
Thermal CVD films have various applications in semiconductor fabrication: combined with various thin oxide and polysilicon layers, they are used to mask regions for selective oxidation during LOCOS isolation. Nitride layers can be used as an etch stop for self-aligned contact

holes, to allow lithographic misalignment to expose the polysilicon gate stack without excessive erosion during contact etch. Nitride layers can be used as a CMP (chemical mechanical polishing) stop layer for oxide polishing, and as a barrier to sodium diffusion to protect gate oxides. Deposited nitrides are frequently part of the dielectric stack for capacitors in DRAM (dynamic random access memory) fabrication processes, and sometimes used in gate dielectric stacks.

(IV) Other Oxidation Methods

Plasma Oxidation

This is a low temperature vacuum process, which can grow reasonably thick oxides (~ 1μm) at low temperatures (600°C) using oxygen plasma. The plasma is generated using a high-frequency discharge. The growth rate increases with increasing oxygen pressure, substrate temperature, and substrate doping.



The mechanism is not well understood, but the oxide probably grows by inward migration of oxygen atoms. This is also called Plasma Enhanced CVD.

7. Case Study: TEOS/Ozone Thermal CVD

New precursors are developed to deposit intermetal(IMD) and interlevel dielectric (ILD). As the technology is driving towards 0.10 μm line widths and gaps, better gap filling capabilities are needed and, as much as possible, dielectric films need an in-situ flow characteristics.

TEOS(tetra-ethyl-ortho-silicate) is a relatively inexpensive, safe source for silicon dioxide. However, deposition using oxygen or inert ambients requires temperature in excess of 600 C. To achive lower temperature deposition, it is necessary to add a more aggressive oxidant. The use of ozone as this oxidant has been widely explored and found commercial applications.

Ozone is triatomic oxygen, O_3. The molecule is metastable at room temperature, slowly degrading into molecular oxygen over a few days. The decomposition reaction, which generates monatomic oxygen intermediates, is strongly activated and takes place in milliseconds at temperatures > 200 C.

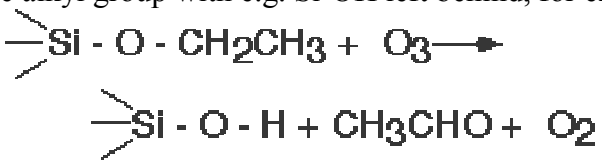
Ozone is normally generated from oxygen at the point of use, since it cannot be readily stored for long periods. Ozone in concentrations of greater than about 12-15 mole% is explosive even at room temperature, limiting most applications to maximum concentrations of less than 10 mole %. Generators use "silent discharge" (RF capacitive discharges at atmospheric pressure through a dielectric wall) cells; efficient generation requires generous cooling provisions to keep the cell temperature low, and avoid decomposition of the ozone as it is produced. Traces of nitrogen are sometimes added to help catalyze the formation of ozone and stabilize the

generator output, but may generate nitric oxides and help corrode metal plumbing and contaminate wafers in process.

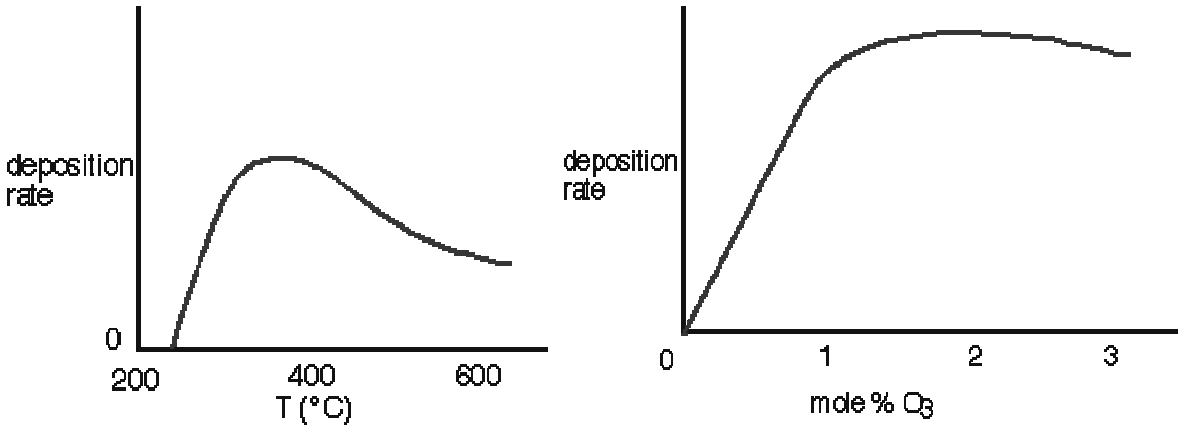
Ozone is highly toxic, but also has excellent warning properties -- you can smell it easily around copying machines in concentrations well below toxic levels. Toxic monitoring and handling in organic-free plumbing are essential: ozone will attack most sealing materials (o-rings) during long-term exposure. Ozone dissolves in water but does not decompose immediately, so simple water scrubbing of exhaust is not adequate for treatment; burning or catalysis is helpful.

Deposition: With the addition of a few mole% of ozone to oxygen, silicon dioxide deposition can be obtained at much lower temperatures than with oxygen alone. The deposition rate is generally observed to saturate as the concentration of ozone is increased, although film quality (discussed below) is often improved by using ozone conc.'s well in excess of the "knee":

The mechanism certainly involves attack of monatomic oxygen produced in the heated gas on TEOS both at the surface and in the gas phase. Gas phase reactions have been shown to represent a significant influence on deposition in SACVD (**s**ub-**a**tmospheric) and APCVD processes; they are probably less important at low pressures (< 10 Torr). Typical reactions involve the attack of the alkyl group with e.g. Si-OH left behind, for example:



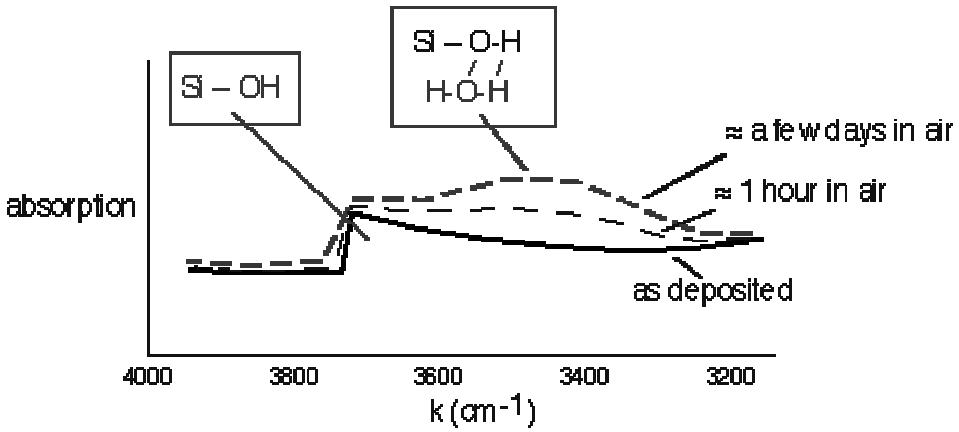
Film Quality: Moisture, Stress, Cracking TEOS/ozone films, like TEOS/O3 films, have excellent conformality in some cases they even seem to display a "flow-like" or more-than-conformal behavior, filling re-entrant features that could not be filled by merely uniform deposition over the existing topography. However, this excellent behavior comes at a price.
Some of the earliest work on TEOS/ozone reactions was performed at pressures of 1-10 Torr,



but it was found that film quality is much improved by deposition at higher pressures. Most commercial implementations of this process employ pressures of 200-760 Torr. Even at higher pressures, TEOS/ozone films are subject to several problems which are rarely observed in thermal deposition from silane, or from TEOS and oxygen at high temperature. In this section we discuss the nature of some of the problems.

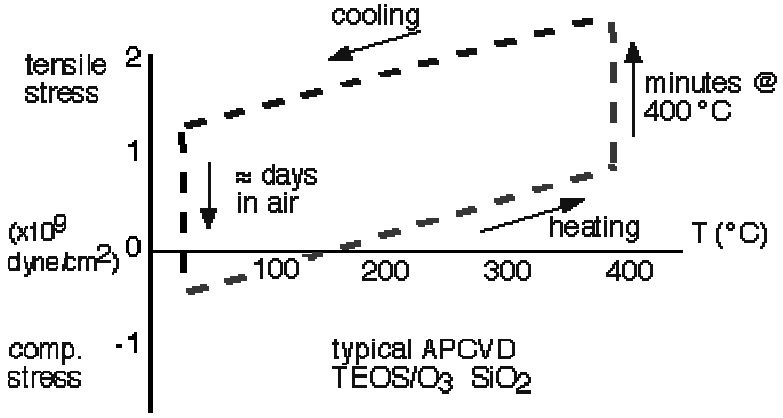
As we noted previously, CVD silicon dioxide is amorphous and cannot be characterized by classic crystallographic (x-ray diffraction) techniques. However, infrared spectroscopy is extremely useful: the nature and quantity of bonds in the material can be detected quickly and

non-destructively. A slice of a typical IR spectrum of silicon dioxide from TEOS and ozone is shown below:



The infrared spectrum in this region is mostly sensitive to vibrations of hydrogen atoms, which due to their low mass have high characteristic frequencies. In the band shown, as-deposited films show a characteristic sawtooth absorption which is assigned to silanol (Si-OH) groups which are hydrogen-bonded to various extents to nearby silanols; the left edge of the sawtooth is near the frequency of the O-H vibration of a truly isolated silanol group, around 3750/cm. Upon exposure to air and remeasurement, we observe the growth of a more symmetrical broad absorption centered around 3300/cm. This absorption is assigned to water molecules hydrogen-bonded to the silanol groups. The extent of this symmetric absorption is essentially an indicator of the amount of water absorbed into the film from the air.

The absorption of water found in the IR spectrum is also indicated in the film stress, typically measured by the change in the curvature of the wafer without and without the film. A typical result for stress during a thermal cycle is shown schematically below:



The films are under modest tensile stress as deposited, but if the measurement of stress is not performed quickly, apparent compressive stress will be measured as water is absorbed into the film over the course of a few hours. Upon heating, water is driven off, with a consequent increase in tensile stress superimposed upon the tensile stress resulting from differential thermal expansion of the silicon wafer and silicon dioxide film. If the wafer is heated at maximum temperatures up to about 400 C, the stress upon cooling will be more tensile than it was initially, and will slowly relax back to comp. stress over several days: this is the phenomenon of stress hysteresis.

Stress hysteresis and IR absorption both signal the presence of water molecules in the films. The water can diffuse into underlying gate oxides and degrade hot-electron reliability of transistors. The stress variations can also impact the reliability of aluminum metallization.
It seems likely (at least to me) that the underlying cause of the increased susceptibility of TEOS/ozone films to silanol incorporation is the large size of the TEOS molecule.

Films deposited from TEOS must undergo significant restructuring to form dense silicon dioxide, as the "holes" left behind by the elimination of ethane or ethoxy groups are filled in. This restructuring becomes difficult if the adsorbed molecule is "under" the surface, covered by subsequent deposition. Thus, higher deposition rates (necessary to reduce cost) give poorer films. Either no bridge bonds are made, giving porous films, or the bonds are strained, and thus susceptible to later hydrolysis.

Silane chemistry only requires elimination of small H_2 molecules (or perhaps water molecules), and doesn't lead to as much porosity; Si-H bonds incorporated into the film may also act as an "internal getter" for any residual moisture. High-temperature TEOS deposition allows bonds to stretch and readjust during deposition, and again produces a denser and purer film.

Thus in order to take advantage of TEOS/O_3 step coverage without impacting transistor reliability, the TEOS/O_3 film is usually encapsulated within layers of plasma-deposited oxide. Achieving uniform growth in these conditions is dependent on avoidance of another problem unique to TEOS/ozone: surface sensitivity. The deposition rate of TEOS/ozone films is strongly influenced by the nature of the substrate.

Film growth is rapid and facile on bare silicon, but thermal oxide substrates produce slow-growing, porous films when deposition is performed by SACVD or APCVD at high ozone concentrations. Traces of fluorine at surfaces also have a strong deleterious effect on deposition rate; F has been intentionally introduced to improve planarization by suppressing growth over metal lines. Introduction of nitrogen on the surface by nitrogen or ammonia plasma treatments enhances growth. Growth on silicon nitride is modestly suppressed. Thus the nature of the underlayer and possible trace contamination at the surface must be considered for successful TEOS/O_3 integration.

Consequences of Chemistry

Conformality and gap fill	Conformality is excellent under most conditions, and sometimes spectacular. However, the need to sandwich the TEOS/O3 film between two PECVD films can degrade the overall ability of the IMD to fill gaps. Doped films (BPSG) have poorer conformality than undoped films.
Smooth film	Very smooth surfaces are normally produced.
Silanol and stress	Films contain silanol as deposited and show stress hysteresis and moisture absorption. Higher ozone concentrations, lower deposition rates, and higher deposition temperature help.
SA/APCVD preferred	High pressures are required for usable films, presumably to increase the absolute concentration of ozone. APCVD is commonly employed; alternatively, pressures between 200 and 700 Torr in a sealed chamber may be used.

8. Processing issues in Dielectric Layer formation

There are many underlying process issues which needs to be addressed well before choosing any Dielectric material and its formation technique in VLSI technology since these issues are directly or indirectly related to actual devices such as transistor, resistors and capacitors etc. and thus have implications on to the actual performance of circuit as a whole. Some of the critical issues are mentioned with their implication on the device behavior

Bird's beak encroachment: -The region at the edges, which spans the transition from the thick field oxide to the thinner pad oxide. This is shown in the fig. when field oxide is formed some of oxygen molecules move into the pad oxide and due to compressive stress the Si_3N_4 layer rises up and the overlap increases.

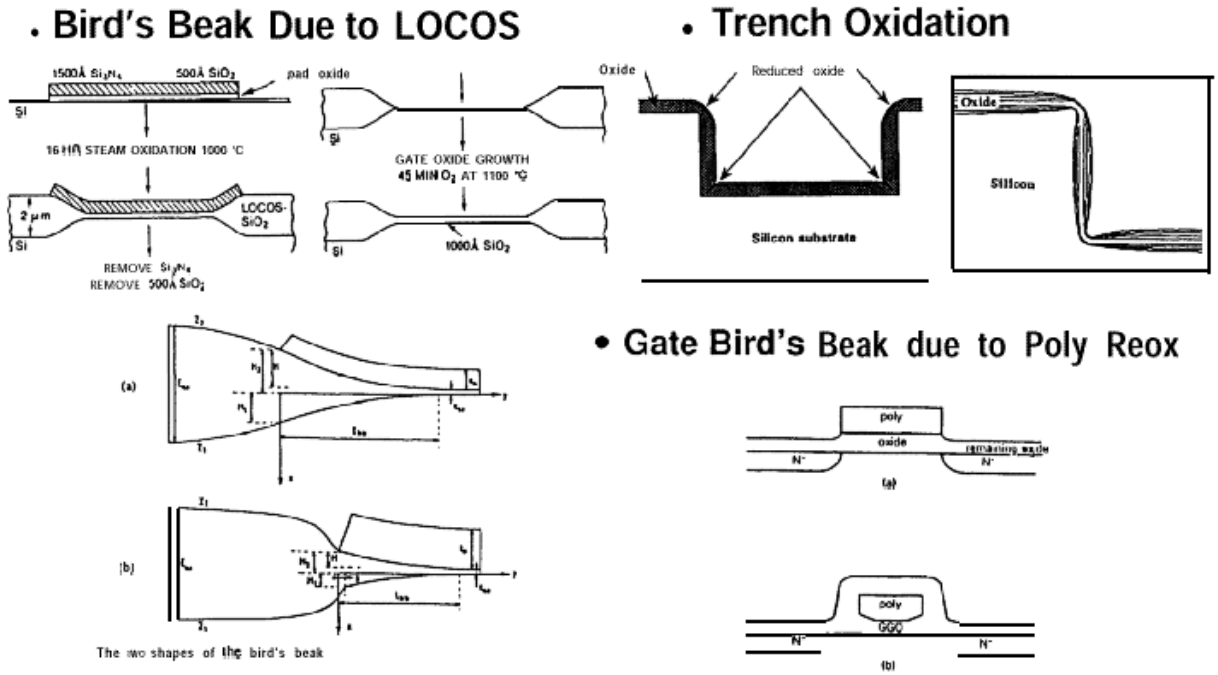


Fig. Illustrating Bird's Beak in thermal oxidation

Effects of Chlorine in the Oxidizing Ambient
Increase oxidation rate
. Cl accumulates within - 30 A of the Si/SiQ interface
Improves oxide properties
- reduced mobile charge
-increased minority lifetime in silicon
- reduced number of oxide defects (higher E_{BD})
- reduced Q_f and Q_{it}
HCI, Cl_2, TCE,TCA

Effect of Crystal Orientation on SiO_2 Growth
The number of Si bonds available at the Si surface depends on crystal orientation impacts reaction rate (the more bonds available per unit area, the greater will be the Si + 02 → SiO2 reaction rate). (111) surface has more bonds than (100) surface.

Effect of doping conc. in the Si on Oxidation rates:-
In general, high doping concentrations in the Si will increase the oxide growth rates. Boron segregates into the oxide during oxide growth and remains in the SiO_2 film. This weakens the

SiO_2 structure, and allows the oxidizing species to diffuse more rapidly through the oxide film and thus oxide growth rates increase. Phosphorus remains in the Si, but the high phosphorus concentration shifts the Fermi level, which increases the vacancy conc. at the Si surface additional sites for the oxidation reaction. Hence oxide growth rates are again increased.

Effect of pressure on Oxidation rates:-
By increasing the pressure we Can grow oxide of same thickness in the same time.For each increase in pressure of 1 Atm, oxide growth temperature can be reduced by 300 C.

9. Challenges in Today's Technology:

With shrinking device geometries to incorporate more number of transistors on a single chip in both CMOS VLSI (to increase the no. of available function) as well as S/DRAM (here the concern is to increase the memory sizes) technologies, current Dielectrics are not just sufficient for future technologies since the requirements of materials for these technologies is also stringent. Therefore a lot of work is going on to find the substitutes of current dielectric materials being used in both gate Dielectric as well as Intermetal dielectrics.

A) High-k Dielectrics for Gate-Insulator

Many materials systems are currently under considerations as potential replacements for SiO_2 as the Gate dielectric material for 0.1μm CMOS technology. The rapid shrinking of transistor feature sizes has forced the Gate Dielectric and channel length to also decrease rapidly. Many materials have been investigated but only few of them adhere to following specification required for selecting an alternative Gate Dielectric:-

(a) Permittivity, band gap, and band alignment of silicon
(b) Thermodynamic stability
(c) Film morphology
(d) Interface quality
(e) Compatibility with current or expected materials to be used in processing for CMOS devices
(f) Process compatibility and
(g) Reliability

The pseudobinary materials systems offer large flexibility and show most promising towards successful integration into the expected processing conditions for future CMOS technologies. Basically to increase the Drive current for shrinking transistor at lower supply voltages the threshold voltage of transistor needs to be decreased. Since ($C_{ox}=\varepsilon_{ox}A/t$) this is possible by increasing the capacitance of the insulator dielectric between gate and the channel, which can be done either by reducing the thickness, or by increasing the dielectric constant (κ) of the material. Former option has many implications on processing so the latter option is investigated in great detail called high-κ metal oxides as a means to provide a substantially thicker (physical thickness) dielectric for reduced leakage and improved gate capacitance.

Most commonly studied high-κ gate dielectric candidates have been materials systems such as TA_2O_5, using epitaxial $SrTiO_3$ and Al_2O_3,which have κ ranging from 10 & 80, and have been employed mainly due to their maturity in memory applications. However, these materials are not thermodynamically stable in direct contact with Si. high-κ dielectric, such as $SrTiO_3$, requires submonolayer control of the channel interface for dielectric deposition. As with the use of all perovskites for dynamically random access memory (DRAM) applications (e.g. $Ba_xSr_{1-x}TiO_3$, $Pb_xZr_{1-x}TiO_3$ etc.) ,the dielectric must be crystalline(using poly crystalline line)to

obtain the enormous permittivities typically observed(κ>300). The work done so far on gate dielectrics therefore has required Molecular Beam Epitaxy (MBE), to obtain interface control and layer-by-layer deposition. Since it is difficult to attain a crystalline oxide on Si, interface engineering has been employed to provide submonolayer deposition of several initial "template" Sr-Si-O layers.

Comparison of relevant properties for high-κ candidates

Material	κ	Band gap E_G(eV)	ΔE_c(eV)	Crystal Structure
SiO_2	3.9	8.9	3.2	Amorphous
Si_3N_4	7	5.1	2	Amorphous
Ai_2O_3	9	8.7	2.8	Amorphous
Y_2O_3	15	5.6	2.3	Cubic
La_2O_3	30	4.3	2.3	Hexagonal,Cubic
Ta_2O_5	26	4.5	1-1.5	Orthogonal, Cubic
TiO_2	80	3.5	1.2	Tetrag
ZrO_2	25	7.8	1.4	Mono,Trag,Cubic

B) **Low-k Dielectrics for Interconnects**

Increasing clock speeds and reduced sizes require new dielectrics with k values of less than 3.Since the capacitance is proportional to k, a reduction in k leads to lower capacitance and RC delay. Also Silicon oxide generally reacts badly with copper at operating temperatures.

The reduced capacitance of these materials permits shrinkage of spacing between metal lines and the ability to decrease the number of levels of metal in a device. Interfacial adhesion properties are similar for both porous and non-porous films, and are not significantly impacted by increasing a material's porosity.

The dielectric constant of a material decreases as its porosity increases. Elasticity decreases with increasing porosity. Hardness decreases with increasing porosity. The decrease in elasticity and hardness severely degrade the mechanical strength of the dielectric material, increasing the risk of thermo-mechanical failures within dielectric/interconnect structures.

Low-k materials can be deposited either by spin-on or CVD (chemical vapor deposition) methods. Porous materials are typically spun on. Controlled evaporation of solvent provides the desired pore structure. Baking of the material is normally done in a batch furnace. Bake temperature is typically between 350°C - 400°C.

Although copper-containing chips were introduced with silicon dioxide insulators, the lowering of insulator dielectric constant is predicted by the ITRS (International Technology roadmap for Semiconductors). Fluorine doped silicon dioxide (κ = 3.7) was introduced at the 0.18μm technology node and there will undoubtedly be insulating materials with κ = 2.6–3.0 introduced at the 0.13μm node. Since the development and integration of these new low κ materials is rather time invariant, κ values will translate to lower technology nodes with the roadmap acceleration.

The introduction of these new low dielectric constant materials, along with the reduced thickness and higher conformality requirements for barriers and nucleation layers, is a difficult integration challenge.

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