A Design Report in
MR-201 Thin Films and Devices: Science and Engineering
On

Hafnium Dioxide (HfO_2) High-k Dielectric thin film formation for Gate Insulators in IC's

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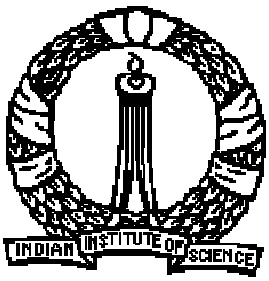

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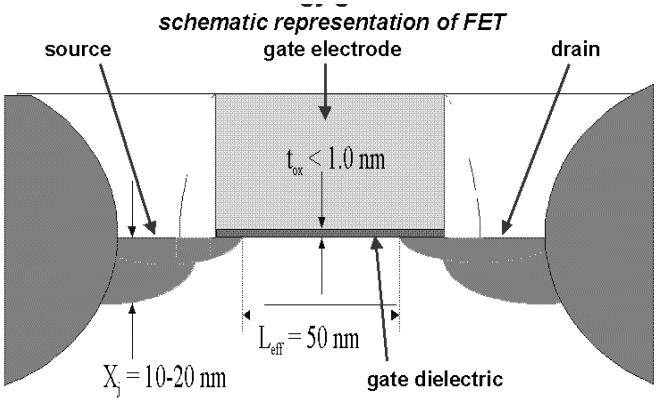
1. Abstract

The Design project focuses on designing high-k Gate Dielectric considering today's increasing demands towards them for many obvious reasons discussed. HfO_2 is found to be the most favorable candidate to replace the conventional SiO_2 Gate Dielectric. Its properties along with the Atomic Layer Deposition methods for HfO_2 thin film formation are presented. Some of the limitations and the methods to overcome their limitation, Hf-Al-O thin film a variation in HfO_2 using Plasma-Laser Deposition is also discussed along with the TEM and X-Ray images. The electrical properties and the C-V characteristics of the film deposited by both the techniques is also shown. The modeling aspects for CAD simulation of these high-k dielectrics are discussed. Finally the issues in High-k Dielectrics from the materials properties and processing related issues are also discussed.

2. Introduction

The industry's demand for greater integrated circuit functionality and performance at lower cost requires an increased circuit density, which has translated into a higher density of transistors on a wafer. This *rapid shrinking* of the transistor feature size has forced the channel length and gate dielectric thickness to also decrease rapidly. The current CMOS gate dielectric SiO_2 thickness can scale to at least 13 Å, but there are several critical device parameters that must be balanced during this process.



direct tunneling across gate dielectric presents serious limitation for continued use of thermally-grown SiO_2

Fig. 1 showing the typical dimensions of MOS Transistor

As scaling is done on the MOS transistors the Supply voltages are also scaled accordingly (to enable constant field scaling) the gate needs to have better control on the channel beneath the Gate insulator. For which we need to increase the gate capacitance (which also increases the drive current)

3. Need for High–k Dielectrics

Consider a parallel plate capacitor C=κεA/t where κ is the dielectric constant *A* is the area of the capacitor, and *t* is the thickness of the dielectric.

Now C can be increased by either decreasing thickness t or by increasing the κ value. Using former option of lower thickness can cause several effects such as Quantam mechanical effects, SIBL (Stress Induced Barrier lowering), DBIE (Dielectric Barrier Induced Epitaxy), GIDL (Gate Induced Drain leakage) etc. So the later option called of using materials of higher permittivity is tried and so called *High-κ Dielectrics*.

This expression for *C* can be rewritten in terms of t_{eq} (i.e., equivalent oxide thickness) and k_{ox}

$$\frac{t_{eq}}{\kappa_{ox}} = \frac{t_{high-\kappa}}{\kappa_{high-\kappa}} \qquad \text{or simply,} \quad t_{high-\kappa} = \frac{\kappa_{high-\kappa}}{\kappa_{ox}} t_{eq} = \frac{\kappa_{high-\kappa}}{3.9} t_{eq}.$$

(=3.9, dielectric constant of SiO_2) of the capacitor. The term t_{eq} represents the theoretical thickness of SiO_2 that would be required to achieve the same capacitance density as the dielectric (ignoring issues such as leakage current and reliability) The physical thickness of an alternative dielectric employed to achieve the equivalent capacitance density of t_{eq}=10 Å can be obtained from the expression A dielectric with a relative permittivity of 16 therefore affords a physical thickness of ~40 Å to obtain t_{eq}=10 Å (As noted above, actual performance of a CMOS gate stack does not scale directly with the dielectric due to possible quantum mechanical and depletion effects).

4. Metal–Insulator–Semiconductor (MIS) gate stack structures

Fig. 2 provides a schematic overview of the various regions associated with the gate stack of a CMOS FET (regions are separated simply to clarify the following discussion). The gate dielectric insulates the gate electrode (gate) from the Si substrate. Gate electrodes in modern CMOS technology are composed of polycrystalline Si (poly- Si) which can be highly doped

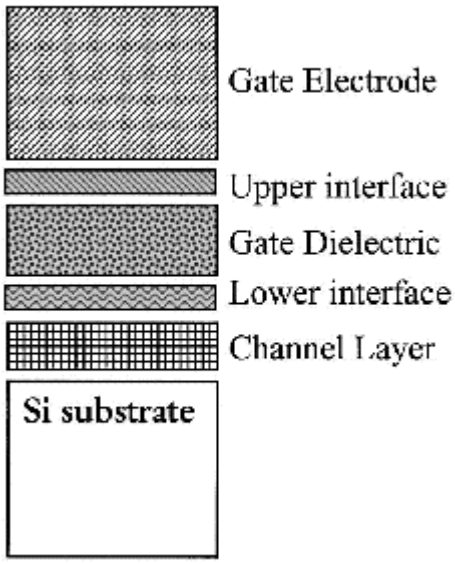


Fig.2. Schematic of important regions of a field effect transistor gate stack.

(e.g. by ion implantation) and subsequently annealed in order to substantially increase conductivity. The selection of the dopant species and concentration permits the adjustment of the poly-Si Fermi level for either nMOS or pMOS FETs.
The interfaces with either the gate or the Si channel region are particularly important in regard to device performance. These regions, ~5 Å thick, serve as a *transition* between the atoms associated with the materials in the gate electrode, gate dielectric and Si channel. These interface regions can alter the overall capacitance of the gate stack, particularly if they have a thickness which is substantial relative to the gate dielectric. Additionally, these interfacial regions can be exploited to obtain desirable properties. The upper interface, for example, can be engineered in order to block boron outdiffusion from the *p*+ poly-Si gate. The lower interface, which is in direct contact with the CMOS channel region, must be engineered to permit low interface trap densities (e.g. dangling bonds) and minimize carrier scattering (maximize mobility) in order to obtain reliable, high performance.

5. Scaling Limits for Current Gate Dielectrics (SiO_2)

A. SiO_2 inherent limitations

With decreasing thickness of SiO_2 studies have been done(on 7-15 Å SiO_2 on Si) and observed that full band gap is obtained only after two monolayers of SiO_2. But the leakage current is

extremely high at this thickness, which are not suitable for current Low power and memory applications.

B. Reliability

An equally important issue regarding ultrathin SiO_2 gate oxides has been understanding and predicting oxide reliability. Oxides down to 14 Å at 1.4 V operating voltage will meet ten year reliability requirements. Recently reached similarly encouraging reliability projections for such thin SiO_2 gate oxides. Other extrinsic reliability factors, however, such as particles or contaminants, could still yield ultimately poorer oxide reliability. A "percolation model" proposed by DeGraeve has described breakdown of oxide as a built up of many "defects" within the SiO_2 layer, where after a certain amount of stress a complete path of defects form across the oxide thickness.

C. Boron Penetration and surface penetration

In addition to leakage current increasing with scaled oxide thickness, the issue of boron penetration through the oxide is a significant concern. The large boron concentration gradient between the heavily doped poly-Si gate electrode, the undoped oxide and lightly doped Si channel causes boron to diffuse rapidly through a sub-20 Å oxide upon thermal annealing,

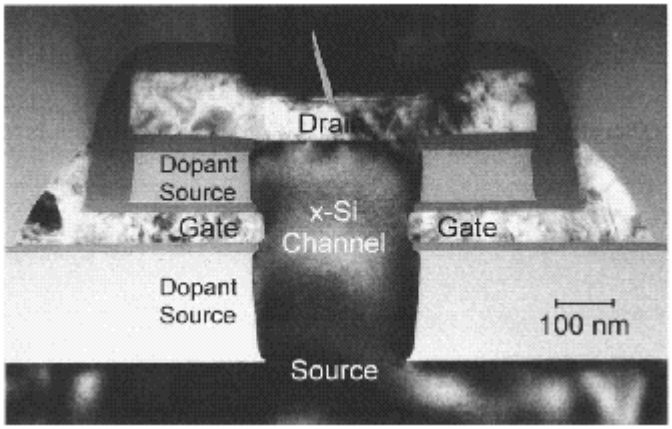


Fig.3 Cross-sectional TEM image of a vertical replacement gate transistor, with a 50 nm gate length and 25 Å SiO_2 gate oxide.

which results in a higher concentration of boron in the channel region. A change in channel doping then causes a shift in threshold voltage, which clearly alters the intended device properties in an unacceptable way.

D. Fundamental Limitations

Despite the current efforts with SiO_2, oxynitrides and even high- k gate dielectrics (HfO_2 to be discussed), several potential fundamental limitations could seriously threaten the continued scaling of all gate dielectrics, regardless of the material. First, the electrical thickness of any dielectric is given by the distance between the centroids of charge in the gate and the substrate. This thickness, typically denoted by t_{eq}, therefore includes the effective thickness of the charge sheet in the gate and the inversion layer in the substrate (channel). These effects can add significantly to the expected t_{eq} derived from the physical thickness of the dielectric alone.

Depletion in the poly-Si gate electrode arises from the depletion of mobile charge carriers in the poly-Si near the gate dielectric interface, particularly in the gate bias polarity required to invert the channel. The result is often that ~3–4 Å in the poly-Si electrode nearest to the gate dielectric interface essentially behaves like intrinsic Si, which adds ~3–4 Å to the effective dielectric thickness (rather than acting as a metal with a Fermi sea of electrons right up to the dielectric interface). In the best case, the electrode depletion region can be reduced to ~1–2 Å for degenerately doped poly-Si electrode right up to the interface, but this is difficult to obtain.

6. Alternative High-κ Gate Dielectric-HfO_2 (Hafnia)

To circumvent the above limitations of SiO_2 other materials are proposed to replace it. Much research work is undergoing in the field of High-k Gate Dielectrics and many materials are investigated for potential replacement. These materials include Si_3N_4, ZrO_2, HfO_2, Al_2O_3, Ta_2O_5 and pseudobinary compounds such as $SrTiO_3$, Hf-Al-O. In the *Literature report* the possible Dielectrics have been discussed. Here the discussion is limited to HfO_2 (Hafnia) and its variant Hf-Al-O. HfO_2 has recently emerged as strong candidate for replacing SiO_2 because of its various favorable properties and ease in thin film formation techniques and process compatibility with the existing and future materials and processes to be used in CMOS VLSI integrated Circuit fabrication.

HfO_2 Growth and properties

As metal–oxide–silicon transistor lateral dimensions decrease and higher switching speeds are required, the SiO_2 gate dielectric thickness must be decreased to<1.5 nm for a 0.1 mm channel length device. However, as the thickness of the SiO_2 decreases, the leakage current across the gate dielectric increases enormously through direct tunneling. In order to reduce the leakage current, high dielectric constant material HfO_2 is being widely investigated because it provide a much lower effective electrical thickness (or, alternatively, greater capacitance density), while retaining sufficient physical thickness of the dielectric to avoid direct carrier tunneling between the gate metal and the Si channel.

Crystal Structure of Hafnium Dioxide

HfO_2 (hafnia) is well established to exhibit three crystalline phases at ambient pressure, i.e., monoclinic, tetragonal and cubic, as temperature is increased. With increasing pressure, phase transitions involving two orthorhombic phases occurs.

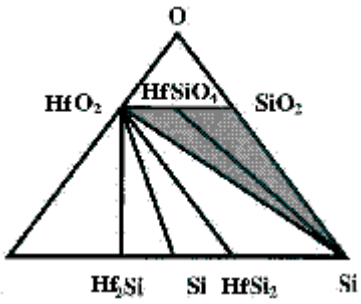


Fig.4 Ternary phase diagrams for Hf–Si–O.
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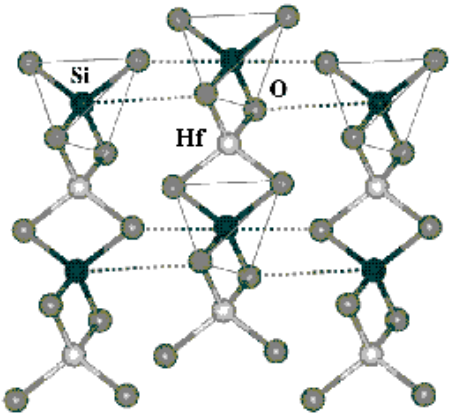

Fig.5 Struct. of crystalline $HfSiO_4$ showing the Hf bonding to Si-SiO_2 units. Hf–O bonding also exists in and out of plane of page.

7. Atomic Layer Deposition (ALD) of HfO_2 thin Film

Among many possible deposition techniques for preparing ultrathin metal oxide films, atomic layer deposition (ALD) is very promising because it can produce high quality films with precise thickness control and near-perfect conformality owing to its adsorption-controlled deposition mechanism. At present, HfO_2 is drawing significant attention for high permittivity gate dielectric applications because it has been reported that HfO_2 gate dielectric is compatible with conventional poly-Si without needing a barrier layer. However, unlike ALD-grown ZrO_2 films, which are typically observed to be polycrystalline, there is a phase change during

annealing of as-deposited HfO_2 in which an amorphous phase transforms to a polycrystalline film in the monoclinic phase.

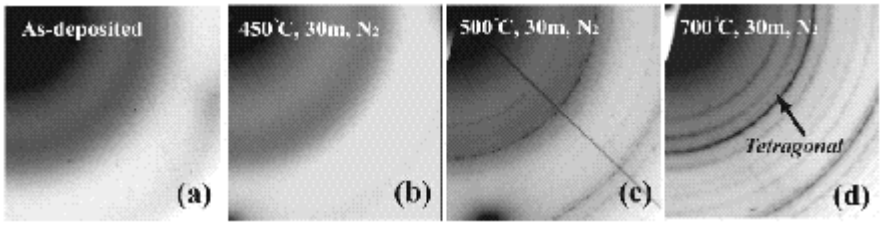

Fig.6 Selected area electron diffraction patterns of 30 Å HfO_2 film after N_2 annealing at various temperatures for 30 min: (a) as-deposited, (b) 450, (c) 500, and (d) 700 °C.

The effects of crystallization on the electrical characteristics of the HfO_2 film have not yet been reported in detail. However the microstructural evolution and interfacial oxidation of ALD-grown HfO_2 as a function of N_2 annealing temperature without a capping layer are reported. Effects of microstructural changes on the electrical characteristics of the resulting gate stacks, as probed by capacitance–voltage(C–V) and current–voltage (I–V) measurements, are also discussed.

As an interfacial layer, ~25 or ~15 Å SiO_2 is thermally grown on 4 in. diameter p-type (100) Si wafers having 1–10 (V cm) resistivity. The deposition of 28–30 Å HfO_2 is performed at 300 °C using alternating surface-saturating reactions of $HfCl_4$ and H_2O in a cold wall-type, high vacuum ALD system. Various process results such as linear growth rate, independence of growth rate on precursor and purging duration time, and near-perfect step coverage on high aspect-ratio structure confirms the ALD regime for the HfO_2 process used.

Annealing Conditions

In order to investigate the HfO_2 phase transformation, samples are annealed from 450 to 900 °C in N_2 ambient for 30 min without any capping layer. Various sizes of Pt electrodes for electrical measurement are deposited by the shadow mask technique using an electron-beam evaporation system and, subsequently, Al is deposited on the backside to reduce the contact and series resistance of the samples. C– V measurements are performed before and after forming gas anneal (4% H_2 /N_2 , 400 °C, 30 min) using a LCR meter. I–V measurements are performed using a voltage source and electrometer.

Thickness and microstructures of various samples are analyzed by both cross-sectional and plan-view *transmission electron microscopy (TEM)* operating at 200 kV. In order to identify the crystallization temperature and the crystalline phases present in the ALD-grown HfO_2 dielectric layers, selected-area electron diffraction (SAED) patterns are collected during TEM analysis after N_2 annealing at various temperatures, as shown in Fig.6 All of the samples are annealed without a capping layer on the HfO_2 films. The as-deposited state exhibits a typical amorphous diffraction pattern and few widely separated nanometer-sized crystallite ''seeds'' are detected after extensive TEM plan-view studies. Significant crystallization of the 30-Å-thick ALD-grown HfO_2 films is detected after annealing for 30 min at ~500 °C. The majority of the crystalline phase formed is found to be monoclinic, as reported previously by others. After 30 min N_2 anneals at 600–700 °C, the HfO_2 film appeared to be fully crystallized based on plan-view images. An additional, second-phase diffraction ring is detected during SAED studies of samples annealed at temperatures in this range. Other researchers have reported formation of residual cubic, orthorhombic, or tetragonal phases during crystallization of amorphous HfO_2. Careful measurement of interplanar spacings detected from SAED patterns suggests that only crystalline second phase observed in our experiments is tetragonal HfO_2. Plan-view bright-field and dark-field imaging indicates that the crystallized microstructure is composed of clusters of very small grains separated by either low angle grain boundaries or

twin boundaries. These clusters of nanometer-scale grains with small mutual misorientation are a few hundred angstrom scale and are separated by surrounding high angle grain boundaries.

8. Electrical Properties of thin film formed by ALD

High frequency C– *V* measurement is performed before and after the forming gas annealing using 18,500 μm^2 circular capacitor patterns. Capacitance is measured at 100 kHz as a function

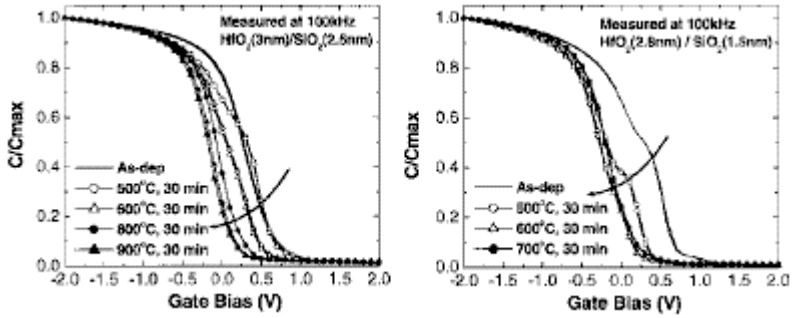

FIG. 7 Normalized C– *V* characteristics as a function of N_2 annealing temperature measured at 100 kHz before forming gas anneal: (a) 30 Å HfO_2 /25 Å SiO_2 and (b) 28 Å HfO_2 /15 Å SiO_2 .

of gate voltage and the capacitor is swept from inversion to accumulation and back to check the amount of hysteresis. In general, the metal–oxide–semiconductor field effect transistor devices are annealed in forming gas to passivate interface states with hydrogen in the final

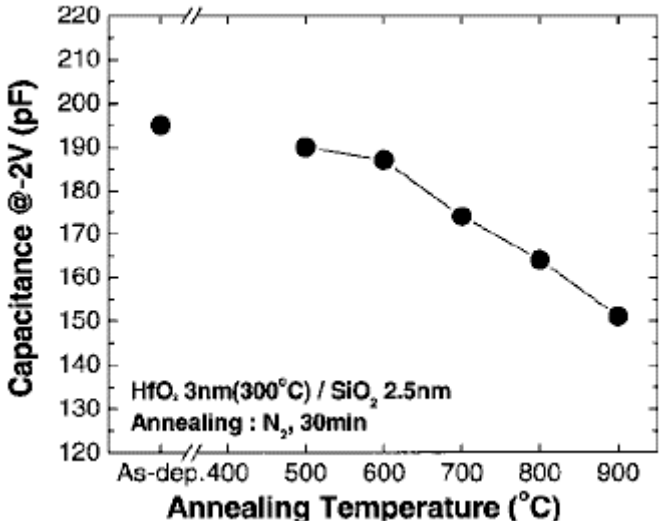

Fig.8 Change of maximum capacitance at -2 V with N_2 annealing temperature after forming gas anneal.

fabrication stage, and this annealing step can screen out changes of intrinsic interface and bulk properties that would otherwise be detected in C–V measurements. Therefore, the generic characteristics of HfO_2 films having various microstructural evolution stages are also analyzed by C–V measurement prior to forming gas annealing. As is evident from Fig.7, there is no significant change in the C–V hysteresis as crystallization of the initially amorphous HfO_2 films takes place.

This suggests that introduction of grain boundaries or crystal/amorphous boundaries does not significantly increase the density of carrier trapping defect sites that contribute to C–V hysteresis at these frequencies. The initial C– V curve from the as-deposited sample is slightly stretched compared to one measured after forming gas anneal, indicating a high density of

interface states prior to hydrogen exposure, which is significantly reduced by forming gas anneal. A noticeable shoulder on the C–V curve is observed at a gate bias of ~0.25 V in the case of HfO_2 /25 Å SiO_2 structure annealed at 500 °C before forming gas anneal Fig.7(a). When a very thin (~15 Å) interfacial SiO_2 layer is used Fig.7(b), this shoulder is detected in C–V measurements of the as-deposited sample, and became more distinct after 500 °C annealing.

It is believed that this feature, which can be attributed to a very large density of interface states, may originate from Hf diffusion and subsequent interfacial layer mixing with SiO_2 layer during deposition and subsequent annealing depending on the interfacial oxide thickness. If the interfacial oxide is moderately thick such as 25 Å SiO_2 case, interfacial mixing would occur through thermal annealing at least 500 °C. On the contrary, if it is thin enough like 15 Å SiO_2 case, during the deposition interfacial layer is already mixed and caused the significant generation of interface states. After the forming gas annealing, all the interface states disappeared as expected by hydrogen passivation effects. At higher annealing temperatures, interfacial oxidation or phase separation of interfacial layer results in the decrease of the C–V feature, indicating a decrease of interface state density. Above 700 °C, the flatband voltages are shifted lower and deviated further from ideal value (~0.95 V). This is believed to be mainly caused by the decrease of total maximum capacitance maintaining the similar fixed oxide charge density.

Fig.8 shows the change of maximum capacitance measured in the accumulation region (-2 V) after forming gas anneal as a function of N_2 annealing temperatures. The maximum capacitance decreased as the annealing temperature is increased and the decrease is particularly dramatic for 30 min anneals at temperatures of 700 °C and above.

This significant change at higher temperatures is caused by growth of the amorphous interfacial oxide layer, as is confirmed by cross-sectional TEM studies. Interestingly, in plan-view TEM images of samples annealed at 700 °C and above, distinct white boundaries are observed as shown in the inset of Fig.9 This boundary contrast may result from thermal grooving, which would reduce the surface energy along grain boundaries separating the nanometer-scale HfO_2 grains. Cross-sectional TEM pictures show significant interfacial oxide growth (25% increase after 900 °C annealing) during N_2 annealing. Although high purity N_2 is used , the interface oxide growth may result from the presence of 1–10 ppm of oxygen as an impurity in the nitrogen gas. The shorter diffusion length along the thermally grooved high angle boundaries enhances the diffusion of oxygen through thin HfO2 film.

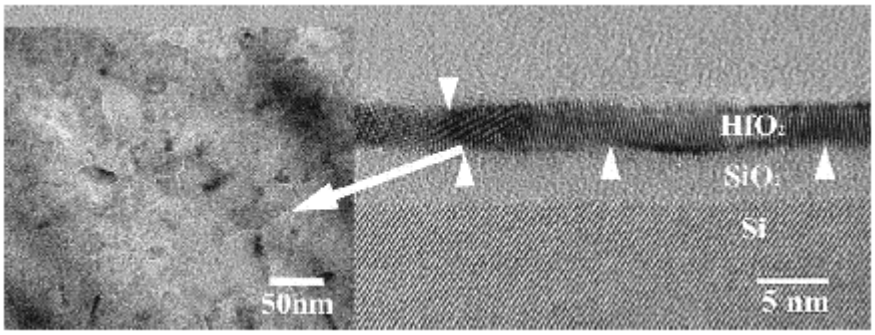

Fig.9 Cross-sectional high-resolution TEM micrograph of HfO_2 /SiO_2 after 900 °C N_2 annealing for 30 min. (Inset of the figure shows the bright-field TEM image of plan view sample)

Room temperature leakage current behavior is measured at various stages of microstructural evolution after annealing. Representative results are as shown in Fig.10 for HfO_2 films of 30 Å thickness deposited onto Si (100) Substrates passivated by 25 Å of thermal oxide. In the case of as-deposited samples, a distinct leakage current mechanism change is observed at ~3.2 V. At higher electric fields, the Fowler–Nordheim tunneling mechanism matches well with measured results and an interface potential barrier of ~2.34 eV is obtained by assuming the

effective electron mass in HfO_2 is 0.1m. This barrier height value is very similar to the recently published experimental value measured at low temperatures, 2.48 eV. At low electric fields, a trap-assisted tunneling conduction mechanism is consistent with the data observed from these films in variable-temperature I–V measurements, and with other published experimental results.

Detailed TEM and electron diffraction results 10 indicate that significant crystallization is observed after 30 min anneal at 500°C, and HfO_2 crystallization is essentially complete in 30 Å films after a 600°C anneal of the same duration. However, as is evident from Fig. 5, the leakage current in the trap assisted tunneling regime did not change significantly as a result of these crystallization anneals. A monotonic decrease in leakage current density with increasing

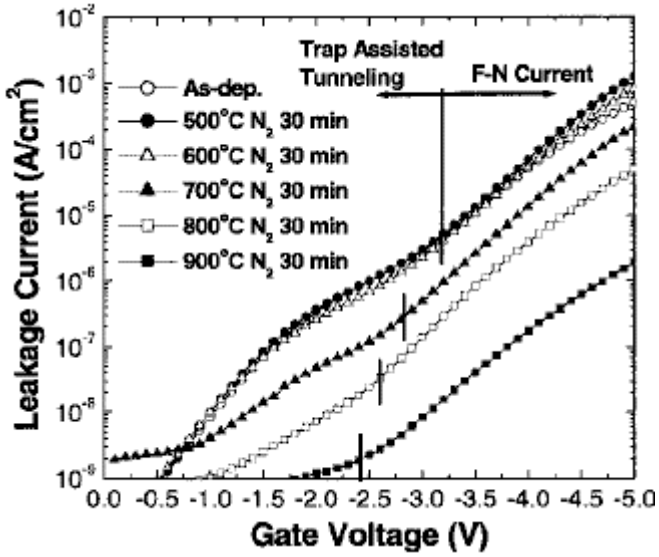

Fig.10 Leakage current characteristics of 30 Å HfO_2 /25 Å SiO_2 structure after forming gas anneal as a function of N_2 annealing temperature.

annealing temperature is observed after 30 min anneals at temperatures of 700 °C and higher (Fig. 10). This trend, and the change in the transition voltage from trap-assisted tunneling to Fowler–Nordheim tunneling conduction, are consistent with a decreasing electric field across the gate stack with increasing anneal thermal budget. Trends in the I–V data are consistent with the observed increase in interfacial oxide thickness after annealing the ALD–HfO_2 dielectric layer at these annealing temperatures. In the case of HfO_2 samples annealed at various temperatures on thin SiO_2 (15Å) (data not shown), interfacial oxide growth and simultaneous decrease in the leakage current is detected at much lower annealing temp. (~500 °C).

There are concerns that leakage current densities may be higher across polycrystalline dielectrics than in amorphous films of the same composition because defective grain boundary regions may enhance electronic conduction. For this and other reasons, a number of methods are now being studied to suppress the crystallization of high-k gate dielectric materials. On the contrary, although as-deposited ALD–ZrO_2 gate dielectrics are polycrystalline, measured leakage current densities across ALD–ZrO_2 gate stacks are comparable to or even lower than those reported for amorphous high-k dielectric candidates with comparable EOTs. The present experimental results, in which crystallization of HfO_2 films is shown to have almost no effect on the gate leakage current, even in the trap assisted tunneling conduction regime, suggests that the additional trap states introduced by formation of grain boundaries make little contribution to conduction. One possible interpretation of these data is that the concentration of ''bulk'' defects within the dielectric layer (point defects and Cl impurities, for example) produces a far greater trap density than that contributed by grain boundaries.

9. Limitation of HfO_2

Although HfO_2 as well as their silicates are becoming leading candidates for high-*k* gate dielectric application due to their thermodynamic stability in contact with Si, however, due to the weakness as an oxygen diffusion barrier of HfO_2 formation of interfacial SiO_2 rich layer in contact with Si substrate or polysilicon gate material is still a problem affecting the application. Formation of silicide at the interface without oxygen is another serious problem.

Resolving the limitation Using Alumina

Al_2O_3 is a well-known good oxygen diffusion barrier that may protect the Si surface from oxidation, and Al_2O_3 is thermodynamically stable in contact with Si. Similar to SiO_2, Al_2O_3 is also a good glass former; thus, if alloyed with HfO_2, their amorphous structure can be stabilized during high temperature annealing. In addition, Al_2O_3 has a large band gap (8.8 eV) and large band offset with Si. To take advantage of both HfO_2 and Al_2O_3, it is desirable to make multicomponent MaI_xO_y (M=Hf, Zr) films with high dielectric constant that are thermodynamically stable in contact with Si. Recent results on aluminates of Zr (Zr–Al–O) indicate that such material system exhibits encouraging gate dielectric properties.

$Zr_{0.62}Al_{0.38}O_{1.8}$ thin film in which the crystallinity starts to appear at 850 °C. Accommodation of Al_2O_3 layer with HfO_2 films in order to increase the interfacial stability with Si and some thermal stability studies on Hf–Al–O films have been reported recently. Electrical properties such as electron trapping and band alignment in amorphous Hf–Al–O have also been reported. However, the understanding of thermodynamic stability and interfacial structure of the Hf–Al–O thin film is still limited. The synthesis and characterization of ultrathin Hf–Al–O films for high-*k* gate dielectric application with equivalent oxide thickness less than 10 Å is discussed next

10. Advantage of Hf-Al-O structure

Al inclusion in HfO_2 has a direct effect on the crystallization temperature, leakage current, band gap, dielectric constant, and border traps. It has been found that the crystallization temp. is significantly increased by adding Al into the HfO_2 film. With an addition of 31.7% Al, the crystallization temperature is about 400 C–500 C higher than that without Al. This additional Al also results an increase of the band gap of the dielectric from 5.8 eV for HfO_2 without Al to 6.5 eV for Hf-Al-O with 45.5% Al and a reduced dielectric constant from 19.6 for HfO_2 without Al to 7.4 for Al_2O_3 without Hf. Considering the tradeoff among the crystallization temperature, band gap, and dielectric constant, it is estimated that the optimum Al concentration is about 30% for conventional self-aligned CMOS gate processing technology.

11. Pulse-Laser deposition (PLD) Technique for Thin Film formation of Hf-Al-O

The Hf–Al–O ultrathin films on p-type (100) Si substrate are deposited by pulse-laser deposition (PLD) Using specially designed target containing HfO_2 and Al_2O plates. In this process the laser frequency is set to 2 Hz and the target rotation is set to a speed in which HfO_2 and Al_2O_3 target is sequentially ablated only one pulse a time during laser ablation. Based on the experimental data, the HfO_2 and Al_2O_3 films growth rate for each pulse is about 0.2 Å which is much smaller than one single atomic layer. Therefore, the composite films grown by this method can be considered sublayer laminates of HfO_2 –Al_2O_3, and we can expect that such films are comparable with the films made using a target containing HfO_2 and Al_2O_3 particles.

The base vacuum the chamber is =5x10^{-5} Pa, and, in order to reduce the formation of interfacial SiO_2 layer, the films are deposited at relatively lower substrate temperature 550 °C. Si substrates are treated by a conventional HF-last process before film deposition leaving the hydrogen terminal surface. A KrF excimer laser (λ=248 nm) with laser fluence of 6 J/cm^{-2} used for the film deposition. In order to study its structure stability under high temperature, the as-grown films are rapid thermal annealed (RTA) at 1000 °C for 10 s at vacuum of 10^{-3} Torr. RTA under reduced oxygen pressure (5 Pa) is also performed at 500 °C for 1 min in order to compensate the oxygen loss during film deposition. The structure of the films and the interface with Si substrates before and after annealing is characterized by means of high-resolution transmission electron microscope (TEM) Using electron microscope equipped with energy dispersive x-ray (EDX) analysis. The chemical structure of the film is characterized using a Physical Electronics Quantum x-ray photoelectron spectrometer with a monochromatic Al $K\ \alpha$ (1486.7 eV) source. The scans are done at pass energy of 23.5 eV and a takeoff angle of 90°. All of the spectra are calibrated against C 1s peak (284.5eV) of adventitious carbon and plotted with normalized intensities.

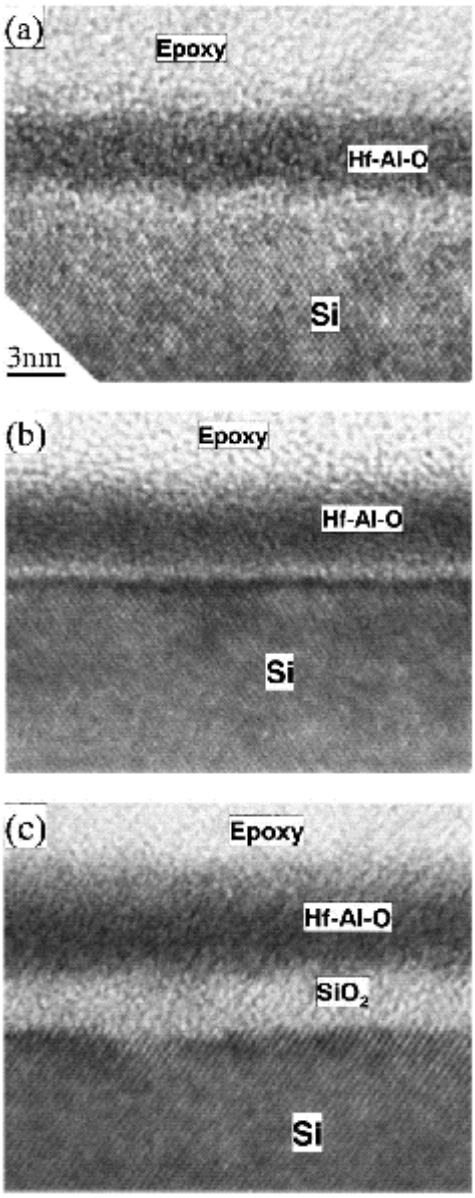

Fig.11 Cross-section TEM images of thin Hf–Al–O films on p-type(100) Si substrates with different annealing conditions. (a) As-grown film, (b) annealed at 500 °C for 1 min with oxygen partial pressure of 5 Pa, and (c) RTA at 1000 °C for 10 s.

12. Electrical properties of thin film formation by PLD

Electrical properties of the MOS capacitors with Pt dot electrodes are studied by C–*V* measurements using a impedance analyzer. Leakage current of the capacitors is characterized by means of Digital Electrometer. The electrode area is 2.5x10^{-3} cm^2 for both C–*V* and I–*V* measurement. EDX analysis of the as-grown Hf–Al–O films shows that films generally have a composition of $Hf_{0.14}Al_{0.25}O_{0.61}$. TEM examinations of different temp. annealed Hf–Al–O films reveals that the amorphous structure of the films is stable under all the annealing temperatures up to at least 1000 °C. Fig.11 shows TEM pictures of an ultrathin (about 38 Å) Hf–Al–O amorphous film grown on Si substrate before and after thermal annealing. In Fig11(a), the very thin white contrast interfacial layer in the as-grown sample indicates a possible SiO_2 rich layer formed during film deposition. After annealing at 500 °C for 1 min in oxygen ambient, there is no further oxidation of the Si substrate as shown in Fig.11(b). This indicates that the film has sufficient resistance to oxygen diffusion at this condition. It should be pointed out that the interface between Hf–Al–O film and epoxy is not sharp since both of them are amorphous structures. The Hf–Al–O film surface is very flat, in fact, as proved by atomic force microscope analysis that shows only 2 Å of rms roughness. No evidence of crystallization can be found within all the observed areas in the Hf–Al–O film after RTA performed at 1000 °C for 10 s. Figure 11(c) is a representative high-resolution TEM picture showing amorphous structure of the Hf–Al–O film after 1000 °C RTA. The interfacial layer formed as shown in Fig.11(c) is a SiO_2 layer due to further oxidation of Si during RTA since

the vacuum is not high enough for very high temperature annealing. The very recent report shows that the structural transition from amorphous to crystalline for the Al_2O_3–HfO_2 nanolaminates occurs at a temperature of 920 °C and the laminate is drastically broken. Therefore, the amorphous Hf–Al–O films under the deposition condition show much better thermodynamic stability compared to laminated structure. The amorphous Hf–Al–O thin film has much better property to block the oxygen diffusion. Fig.12 is a characteristic high frequency C–*V* curve of the 38 Å Hf–Al–O film with bias voltage from 26 to 4V. The accumulation capacitance is 9nF, and too much series resistance may cause the peak near the transition on the accumulation side. The relative permittivity of the Hf–Al–O film is calculated to be about 16 and the equivalent oxide thickness to SiO_2 is 9.2 Å for the sample annealed at 500 °C for 1 min in oxygen ambient. The inset in Fig.12 is a typical current density voltage curve of the MOS capacitor, and one can see that at 1 V gate bias voltage, the leakage current density is $4.6x10^{-3}$ A/cm^2, which is five orders of magnitude higher than that of 10 Å SiO_2 .

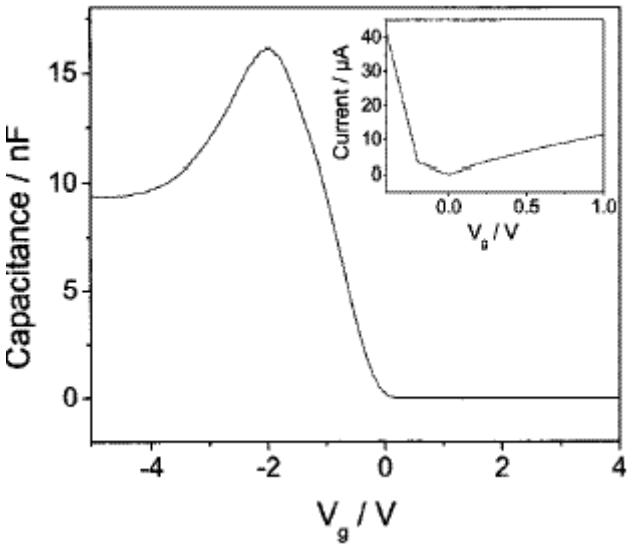

FIG. 12. Characteristic high frequency (MHz) C–*V* curve of the parallel plate capacitor with Pt dot electrode on annealed Hf–Al–O film. The inset shows a typical current density–voltage curve.

12. X-Ray Studies of the thin film

Formation of Hf–O and Al–O bonds is studied by x-ray photoelectron spectroscopy (XPS) analysis as shown in Fig. 13. Fig.13 shows the Al 2p peak at 74.2 eV indicating Al_2O_3 Fig. 13

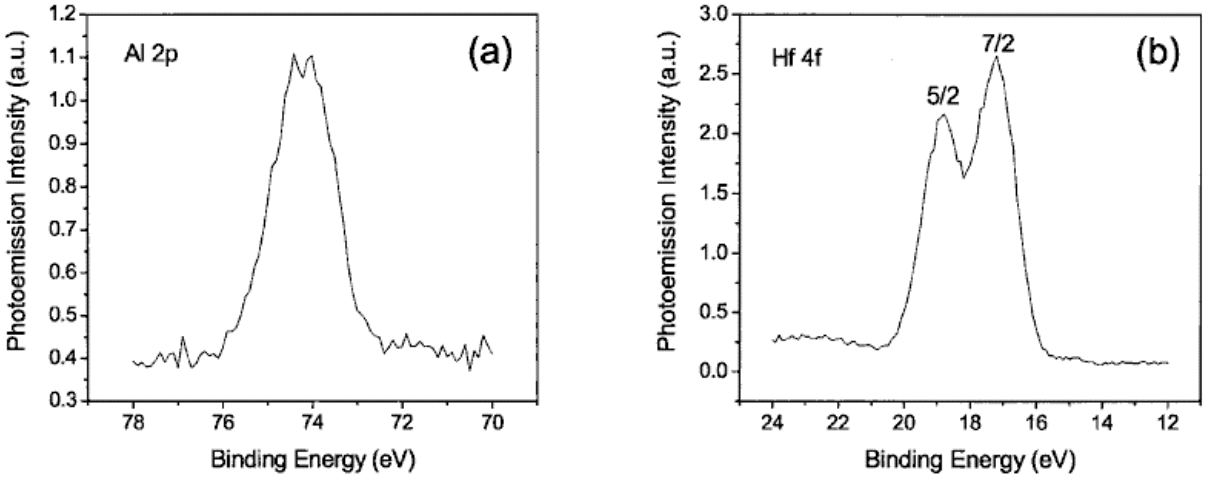

Fig.13 XPS spectrums of annealed Hf–Al–O ultrathin film on Si substrate. (a)Al *2p* spectra, (b) Hf 4 *f* spectra. The Hf 4 *f* (7/2) peak is 17.2 eV, separated by the 1.7 eV spin splitting from the Hf 4 *f* (5/2) peak at 18.8 eV.

formation in the film. The Hf 4 f peak is shown in Fig.13(b). It is worth noting that, compared to the reported Hf 4 *f* peaks (16.8 and 18.5 eV) for HfO_2, there is a 0.4 eV shift of Hf 4 *f* peaks toward higher binding energy for the Hf–Al–O film in our case. The core level peak positions of Hf 4 *f*, Al*2*p,and O *1*s, experience a shift to higher binding energy with the increase of Al_2O_3

concentration in the Hf–Al–O system. This shift may be attributed to the fact than Hf is a more ionic cation than Al in the Hf–Al–O system, and thus the charge transfer contribution changes with the increase of Al concentration.

In summary, ultrathin amorphous Hf–Al–O films have been deposited on p-type (100) Si substrates by PLD. TEM examinations of different temperature annealed Hf–Al–O films reveals that the amorphous structure of the film is stable up to at least 1000 °C annealing. Relative permittivity of 16 and an EOT of 9.2 Å have been achieved by a 38 Å amorphous Hf–Al–O film and the film presents very low leakage current of $4.6x10^{-3}$ A/cm^2. XPS analysis of the Hf–Al–O film shows the formation of Hf–aluminate in the film.

13. Conventional Modeling of the Gate Dielectric thin film

Conventionally since SiO_2 is used and it is grown thermally using dry oxidation as Gate Dielectric very good modeling for simulation is available and the most common model available is **Deal-Groove model** or **linear parabolic model.** In this model it is assumed that

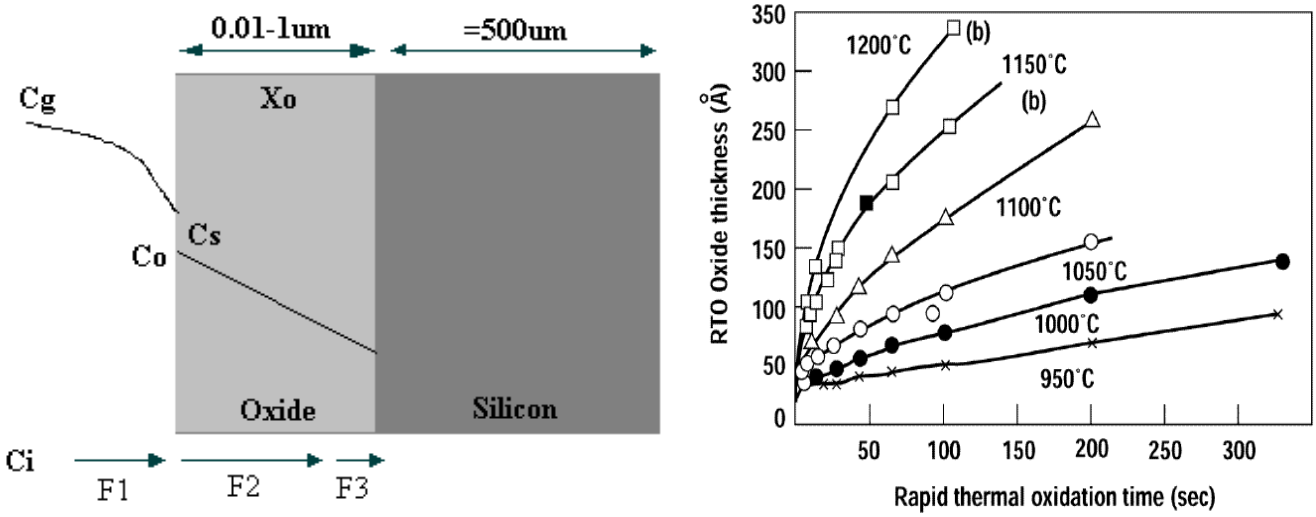

Fig.14 (a) Oxidant flux from the gas phase to the Si surface during thermal oxidation. The line represents the O_2 or H_2O conc. (b) T_{ox} as a function of time for RTA.

The linear parabolic growth law in the following form: $X_o^2/B+X_o/(B/A)=t+T$ where $T=(X^2_I+AX_I)/B$ In these expressions, X_I or T account for any oxide present at the start of the oxidation. They can also be used to provide a better fit to data in the "anomalous" thin oxide regime in dry O_2. Solving the parabolic equation leads to the following expression

$$X_o=B/A\{\sqrt{(1+(t+T)/A^2/4B)-1}\} \text{ where } X_o=B/A(t+T) \text{ or } X_o^2=B(t+T)$$

The reason for referring to B/A and B of the linear and parabolic rate constants are clear when the growth law is expressed in these forms. The linear tems will dominate for small X values. SiO_2 growth on a Si wafer therefore starts out a linear X versus t characteristics, which becomes parabolic as the oxide thickens.

14. High-k device modeling and transport for HfO_2

The incorporation of stacked structures and the layer within the stack that has the lower dielectric constant will limit the overall capacitance of the stack. However, the *minimization of interface states* may require suitable interfacial layers that serve as a transition region between the Si substrate and the dielectric. A graded composition throughout the dielectric permitting control of interfacial state formation preserves, to some extent, the high- k properties sought for the alternative gate dielectric in the gate stack.

Such effects are considered in modeling of potential gate stack materials, the model may or may not incorporate trap assisted tunneling mechanisms but should provide an indication of the trends associated with stack layers and scaling.

The incorporation of an interfacial SiO_2 layer (0.5 and 1.0 nm thick) as a part of a gate stack has the effect of electron injection through this interfacial layer from either the gate or the substrate and is also examined by simply changing the direction of the electric field. In addition to the expected reduction in the overall tunneling current, it is seen that the tunneling current changes substantially depending on the dielectric layer first encountered by the electron.

In an attempt to predict the effect of high- k gate dielectrics on transistor performance, gate dielectrics are modeled with various permittivities in a planar, bulk CMOS structure. It is found that the upper limit of permittivity would be limited to k~20 due to fringing field-induced barrier lowering at the drain region of the device. This phenomenon is a large concern, because a significant fringing field from the edge of a high-k dielectric could lower the barrier for transport into the drain enough to seriously degrade the on/off characteristics of the device.

Perhaps even more important is the issue of field penetration into the Si channel region. The inversion charge in the channel experiences an increasing electric field with increasing gate capacitance, regardless of the gate dielectric material. At a high enough electric field penetration through the gate dielectric, channel carriers will undergo increased scattering, ultimately leading to a decrease in mobility and drive current. Additionally, this inversion layer will have an associated capacitance in series with the gate stack and will also eventually limit the ultimate gate stack capacitance for any high- k dielectric.

15. Issues in High-k Dielectrics material properties and thin film formation

Since the High-k Gate Dielectrics are still under research and many issues needs to be addressed while selecting a suitable material as a substitute of conventional sio_2 some of this issues are discussed in brief

A. Permittivity and Barrier height

For many simple oxides, permittivities have been measured on bulk samples and in some cases even on thin films, but for the more complex materials (more elemental constituents), the dielectric constants may not be as well known. This discrepancy between calculation and

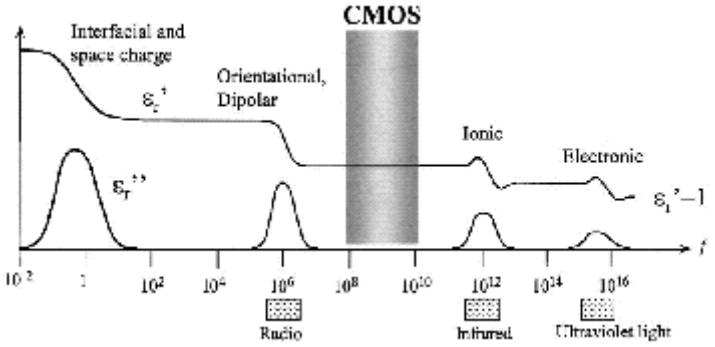

Fig. 15 The frequency dependence of the real (ε'_r) and imaginary (ε''_r) parts of the dielectric permittivity. In CMOS devices, ionic and electronic contributions are present .

measurement of k values can be attributed to many factors, including film thickness, method of film deposition, and local electronic structure within the dielectrics. It is clear that much more experimental data is needed for measurements of dielectric constant for these high- k dielectrics, including HfO_2 particularly below the 100 Å thickness regime.

There are two main contributions of interest to the dielectric constant which give rise to the polarizability: electronic and ionic dipoles (the molecular dipole contribution is not relevant to this study). Fig.15 illustrates the frequency ranges where each contribution is important, and also highlights the current frequency range for CMOS operation (100 MHz–10GHz). In general, atoms with a large ionic radius (e.g., high atomic number) exhibit more electron dipole response to an external electric field, because there are more electrons to respond to the field (electron screening effects also play a role in this response). This electronic contribution tends to increase the permittivity for oxides of elements with higher atomic numbers.

B. Thermodynamic stability on Si

For all thin gate dielectrics, the interface with Si plays a key role, and in most cases is the dominant factor in determining the overall electrical properties. Most of the high- k metal oxide systems investigated thus far have unstable interfaces with Si: that is, they react with Si under equilibrium conditions to form an undesirable interfacial layer. These materials therefore require an interfacial reaction barrier, Any ultrathin interfacial reaction barrier with t_{eq}<20 Å will have the same quality, uniformity and reliability concerns as SiO_2 does in this thickness regime. This is especially true when the interface plays a determining role in the resulting electrical properties. It is important to understand the thermodynamics of these systems, and thereby attempt to control the interface with Si.

In Hf-Si-O system fig. that the metal oxide HfO_2 and the compound silicate $HfSiO_4$ will both be stable in direct contact with Si up to high temperatures.

C. Interface Quality

A clear goal of any potential high-k gate dielectric is to attain a sufficiently high-quality interface with the Si channel, as close as possible to that of SiO_2. It is difficult to imagine any material creating a better interface than that of SiO2, since typical production SiO_2 gate dielectrics have a midgap interface state density D_{it} =2x10^{10} states/cm^2 . Most of the high- k materials (including HfO_2) show D_{it}~10^{11} –10^{12} states/cm^2 ,and in addition exhibit a substantial flatband voltage shift ΔV_{FB}>300 mV (possibly from fixed charge density ≥10^{12} /cm^2 at the interface).

HfO_2 has been previously reported as having high oxygen diffusivities. This is a serious concern regarding control of the interface once it is initially formed. Any annealing treatments which have an excess of oxygen present (either from the ambient or from a sidewall oxide, for example), will lead to rapid oxygen diffusion through the oxides, resulting in SiO_2 or SiO_2 -containing interface layers. So now Al is incorporate into HfO_2 to reduce this effect as is mentioned previously.

D. Film Morphology

Most of the advanced gate dielectrics studied to date are either polycrystalline or single crystal films, but it is desirable to select a material, which remains in a glassy phase (amorphous) throughout the necessary processing treatments. Most of the metal oxides (except Al_2O_3) will form a polycrystalline film either during deposition or upon modest thermal treatments: HfO_2 is no exception. Given the concerns regarding polycrystalline and single crystal films, it appears that an amorphous film structure is the ideal one for the gate dielectric (although some initial electrical results for a polycrystalline HfO_2 layer on an amorphous SiO_2 -containing layer look encouraging). This is yet another clear virtue of SiO_2. In The Hf–Si–O system is the only stable ternary crystalline compound is $HfSiO_4$. While it is possible that other ternary

crystalline compounds do exist, it is unlikely. Bulk thermodynamics therefore suggests that a phase field exists for relatively low levels of Hf in which $(HfO_2)_x(SiO_2)_{1-x}$ composition can be obtained which will remain amorphous and stable on Si up to high temperatures, without phase separating into crystalline MSiO4 or MO2 and SiO2 .

E. Gate Compatibility

A significant issue for integrating any advanced gate dielectric into standard CMOS is that the dielectric should be compatible with Si-based gates, rather than *require* a metal gate. Si-based gates are desirable because dopant implant conditions can be tuned to create the desired threshold voltage V_T for both nMOS and pMOS, and the process integration schemes are well established in industry. Nearly all of the potential advanced gate dielectrics investigated to this point, however, require metal gates.

Both boron and phosphorous dopant diffusion have been observed with Al_2O_3 gate dielectrics, which cause significant, undesired shifts of V_{Fb} and V_T whereas in HfO_2 the diffusion is comparatively smaller as compared to other Dielectrics being investigated.

F. Process Compatibility

A crucial factor in determining the final film quality and properties is the method by which the dielectrics are deposited in a fabrication process. The deposition process for the dielectric must be compatible with current or expected CMOS processing, cost, and throughput. Since all of the feasible deposition techniques available occur under nonequilibrium conditions, it is certainly possible to obtain properties different from those expected under equilibrium conditions. It is therefore important to consider the various methods for depositing the gate dielectrics.

PVD methods have provided a convenient means to evaluate materials systems for alternate dielectric applications. The damage inherent in a sputter PVD process, however, results in surface damage and thereby creates unwanted interfacial states. Additionally, device morphology inherent to the scaling process generally rules out such line-of-sight PVD deposition approaches. For this reason, CVD methods have proven to be quite successful in providing uniform coverage over complicated device topologies.

The reaction kinetics associated with film CVD deposition requires careful attention in order to control interfacial layer formation. The precursor employed in the deposition process must also be tailored to avoid unwanted impurities in the film as well as permit useful final compositions in the dielectric film. Indeed, a graded composition for dielectric films may be a key requirement in order to control interface state formation to a level comparable to SiO_2. The recent application of ALCVD methods for depositing and HfO_2 appears to provide much promise, where self-limiting chemistries are employed to control film formation in a layer-by-layer fashion. As discussed before, attention to the surface preparation and the resultant chemistry must be carefully considered.

G. Reliability

The electrical reliability of a new gate dielectric must also be considered critical for application in CMOS technology. The determination of whether or not a high- k dielectric satisfies the strict reliability criteria requires a well-characterized materials system. Preliminary projections for reliability, as determined by stress-induced leakage current (SILC), time-dependent dielectric breakdown, and mean time to failure measurements, appear to be encouraging HfO_2 films.

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