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Dynamic Threshold MOSFET on SOI for Low Power VLSI circuits

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Abstract

Considering Low Power applications Digital sub-threshold logic circuits have recently been proposed for applications in the ultra-low power end of the design spectrum, where the performance is of secondary importance. Basic Device operation of PD-SOI is discussed first and then to improve switching performance of the sub-threshold logic family with comparable energy/switching, use of sub-DTMOS (sub-threshold Dynamic Threshold MOS) transistors are studied. Added advantage of these devices is that the stability of sub-threshold DTMOS logic to temperature and process variations eliminates the need of additional stabilization scheme that may be required for regular sub-threshold MOS logic families to ensure proper operation in the sub-threshold region.

Introduction

Portable applications that traditionally required a modest performance are now dominated by devices that demand a very high performance. The demand for portability of these new systems limits their battery weight and size, placing a severe constraint on their power dissipation. Second, speed, density, and size of nonportable CMOS based systems have increased considerably in recent years. Thus, lower Consumption that was not a concern in these systems is now becoming a critical parameter. The most common approach for reducing power is power supply scaling. This is due to the fact that in CMOS digital circuits, delivered power is proportional to the square of power supply voltage where is the power consumed by one gate, is the total switching capacitance of the gate, is the power supply volt- age, and is the average cooperating frequency of that gate. Since power supply reduction below three times the threshold voltage will degrade circuit speed significantly, scaling of the power supply should be accompanied by threshold voltage reduction. However, the lower limit for threshold voltage is set by the amount of off-state leakage current that can be tolerated (due to standby power consideration in static circuits, and avoidance of failure in dynamic circuits and memory arrays), and ideally should be no less than 0.4 V. It is seen that if standard MOSFET's are used, a lower bound for power supply voltage or a larger leakage current become inevitable. To extend the lower bound of power supply to ultra-low voltages (0.6 V and below), we propose a Dynamic Threshold Voltage MOSFET (DTMOS) having a high at zero bias and a low Vt.

The increasing demand for portable applications has caused a significant growth of low-power design, from system level to device level. To achieve low-power requirement, various circuit design techniques have been employed, including voltage scaling and clock gating. These techniques work well in the medium-power, medium performance region of the design spectrum, where the delicate balance of power and delay is well maintained. Improved frequency performance through reduced capacitances, higher drive currents and a reduction in the interconnection length are key to SOI for *low power* digital and Analog applications. Noise and latch up are also minimized through reduced substrate coupling. Si resistors used in analog circuits have improved linearity w.r.to absolute voltages in many cases, since they don't form reverse biased diode to substrates. *Analog design* specially requires considerations of V_t variations, body-related effects and thermal management.

I-PD-SOI Circuit Operation

PD-SOI (partially Depleted Silicon On Insulator) is more reliably manufactured (either by SIMOX, Epitaxial Layer Transfer or wafer bonding), compared to fully depleted devices due to limitations in control of the very thin film thicknesses needed. Before exploring the various Dynamic threshold MOS Transistor the electrical behavior of PD-SOI devices where the body node of the device is left floating is being investigated.

(1) **Kink effect**: This results from the fact that there is to large sensitivity to drain bias, and more seriously, the drain conductance exhibits bias and frequency dependent variations, often of more than an order of magnitude within normal operating regimes. These problems can be reduced by the use of a body tie, at the cost of some additional area and parasitic capacitance. However, unavoidable series

resistance in the contact often makes this approach only a partial solution, and significant deviations from ideal behavior can be observed even when a body tie is present.
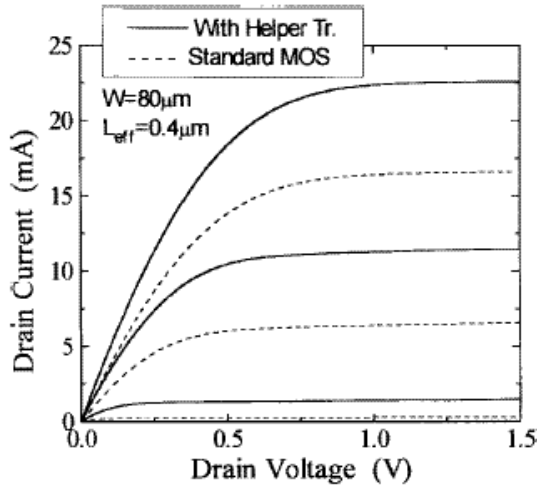

Fig.1. Demonstrating the Kink Effect.

(2) **Floating Body Effect**: Since the body of the PD-MOS is isolated from the bulk therefore it accumulates positive charges and reduces the t which has a serious concern for the increase in the off state current whereas since for low power a low value of Ioff is desired the body is normally tied to either Gate or the source to avoid the floating body effect. The floating body effect also has several advantages since there are two effects associated with it i.e. the AC effects and the DC effects. Due to the capacitive coupling the Vt of transistor reduces so the Id in ON state increases specially during switching and since it offers lower Ioff compared to the Conventional Bulk devices it results in the decrease in Power dissipation.

(3) **Self Heating of individual devices**: This arises from the poor thermal conductivity of the underlying buried oxide, and device channel temperatures can rise dynamically many tens of degrees above ambient during normal operation. Consequently, device characteristics become significantly modified, with negative output conductance often observable at higher drain currents. Such heating is not instantaneous, but has a transient response to bias changes. While there do exist some issues relating to accurate parameter extraction (insofar as the behavior *without* self-heating is not directly observable, and hence the electrical and thermal contributions are not easily separated). Thermal behavior is not generally

significant for digital circuits, due to the low mean power dissipations, and clock frequencies normally being well above the thermal time constant. Analog circuits, however, can be significantly affected. Output conductance's can be low or even negative at low frequencies and then rise with frequency, leading to unforeseen gain and phase changes. The *power dissipation* can also increase significantly due to self-heating.

After discussing the PD-SOI device operation focus on the Sub-DTMOS transistor operation since in the ultra-low power end of the design spectrum, where speed is of secondary importance, a more rigorous approach is warranted. Digital sub-threshold circuits have recently been proposed to meet the ultra-low power requirement. By operating in the sub-threshold region, digital sub-threshold circuits utilize the continuously owing leakage current as the switching current. The minute sub-threshold current makes it possible to achieve ultra-low power dissipation. However, the performance of the digital sub-threshold circuits is several orders of magnitude lower than their normal strong-inversion counterparts. Hence, sub-threshold circuits are applicable to only specific classes of applications where ultra-low power is of primary importance. Such applications range from the implantable pacemakers and defbrillators to the recently emerging wearable, wristwatch computers.

II-Circuits and Low Power Strategies.

The sub-threshold logic circuits using regular MOS transistors, is their extremely high sensitivity to the variation of temperature and process parameters. The exponential dependence of sub-threshold current on threshold voltage (Vth), which in turn depends on the temperature and process parameters, calls for additional stabilization scheme to ensure proper operation. To increase the robustness of the circuit, a self-adjusted threshold voltage (SAT) scheme is adaptoted as shown below. The technique monitors the change in leakage current and stabilizes it by applying appropriate bias to the substrate. A robust sub-threshold logic circuit thus can be achieved, however, this increases the design complexity to a significant extent. Fig.2 shows the Vt variation for such scheme. Another logic family using sub-threshold DTMOS transistors, which

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shows a significant improvement in delay and excellent stability to temperature and process variations while maintaining the same ultra-low power design constraint is also looked at.
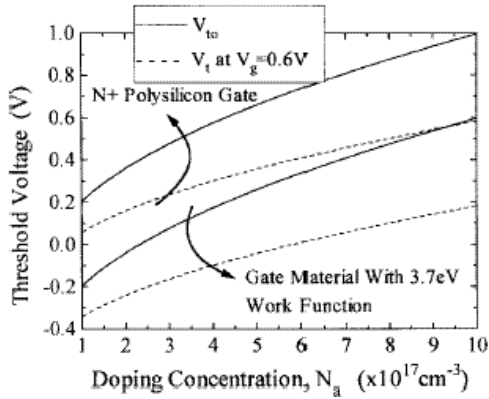

Fig.2 showing the Vt variation for N-DTMOS at Vgs=0, as a function of Silicon film doping concentration.

Sub-CMOS Logic With SAT Scheme

The leakage current of MOS transistor is extremely sensitive to the temperature and process variations, which in turn limit the robustness of the design. These variations result in Vth fluctuation, which has a strong exponential effect on the sub-threshold current. One way to handle this imitation is to stabilize the leakage current by means of establishing a feedback to the device. This is done through adopting a SAT scheme to sub-threshold CMOS circuits. The SAT scheme monitors the leakage current and stabilizes any fluctuation in the leakage current by automatically biasing the substrates of the transistors via a negative feedback loop (Fig.3). There are two main components of SAT scheme, namely the leakage current monitor (LCM) and the self-substrate bias (SSB) circuit (Fig.4).

LCM is used as a leakage current sensor and a control to the SSB circuit. SSB circuit contains a charge pump, which is powered by pulses
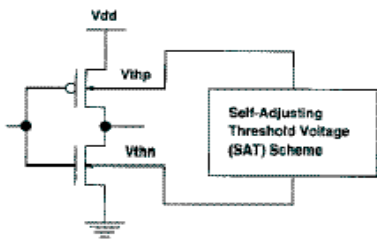

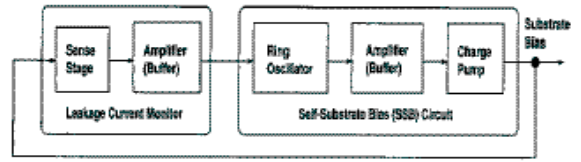Figure 3 : Self-Adjusting Threshold Voltage Scheme

Figure 4: Components of SAT scheme

generated from a ring oscillator. The charges accumulated from the pump are used to bias the substrate. SSB circuit works intermittently and is activated by LCM when needed. Once the target substrate bias is reached, the SSB circuit is deactivated. LCM constantly monitors the leakage current and corrects the substrate bias by reactivating the SSB circuit. Thus the LCM module analogously acts a thermostat, which regulates the temperature and process variations and the sets of fluctuation to the pre-specified tolerable range.

Dynamic Threshold MOS Transistor

Fig. 5 shows the operation of the device in the standard MOSFET mode, or in DTMOS mode: the body is either floated or grounded in the MOSFET mode. The gate is tied to the body in the DTMOS mode, shown in Fig. 2. Besides the four-terminal test device, DTMOS devices with hard local gate-to-body connections are also fabricated as shown in Fig. 3. This connection uses an oversized metal-to-P contact window aligned over a "hole" in the poly gate. The metal shorts the gate and the P region (for N-DTMOS). This contact requires minimal area and no additional processing steps. Standard CMOS, and DTMOS-based CMOS ring oscillators are also fabricated in the same process.
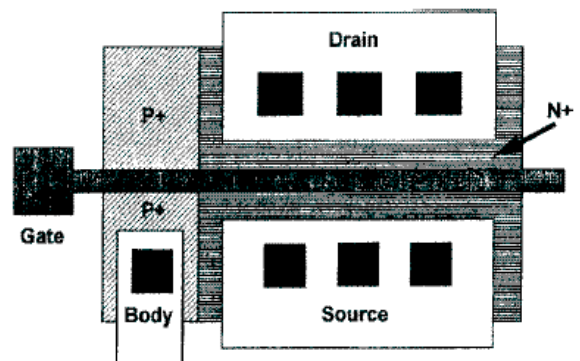

Fig. 5 Schematic of the body contact in SOI NMOS devices. A similar structure is used for SOI PMOS devices with N$^+$ and P$^+$ regions exchanged.
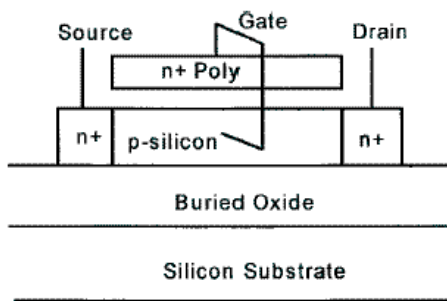
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Fig. 6 Cross section of an SOI NMOSFET with body and gate tied together.

The gate is tied to the body in the DTMOS mode, shown in Fig. 6. Besides the four-terminal test device, DTMOS devices with hard local gate-to-body connections are also fabricated. This connection uses an oversized metal-to- P contact window aligned over a "hole" in the poly gate. The metal shorts the gate and the P region (for NDTMOS). This contact requires minimal area and no additional processing steps. Standard CMOS, and DTMOS-based CMOS ring oscillators are also fabricated in the same process.

Discussion And Conclusion

DTMOS device structures can be improved in several fronts, some of which are discussed below. The DTMOS structure has extra parasitic capacitance around the gate-to-body contact. This capacitance adds to the total switching capacitance and degrades the DTMOS ac performance. Other methods of shorting the body to the gate that eliminate this capacitance are feasible. For example, it is not necessary to use the metal for shorting the body to the gate, as a buried contact concept can be exploited: after the gate oxidation a thin layer of polysilicon (approximately 20–30 nm) is deposited. Next, a mask is used to implant the selected area and to create a contact window by etching the polysilicon layer and the underlying oxide. Subsequently, a thick layer of polysilicon is deposited. This polysilicon layer will be shorted to the silicon film directly in the contact window. Body-to-gate connection at the device edge has the drawback that a wide device may have nonuniform threshold voltage along its width. Providing this connection at both edges of the device, and implementing a wide device as several narrower transistors will alleviate this problem. Also, the n p diode between the n -doped poly and p Si film region poses no problem since the voltage across it will be equal to zero in DTMOS.

In DTMOS, power supply voltage is limited to about 0.6 V or less because of the base current. To mitigate this limitation, an external-limiting scheme can be used: a small transistor is employed to provide the forward bias for the large MOSFET. The small "limiter" transistor clamps the forward bias to only 0.6 V. Although a harsh area penalty is imposed on minimum size devices, the proposed scheme works particularly well for large transistors, such as clock drivers and large buffers. It is experimentally demonstrated by the operation of this circuit. A separate bias voltage may be avoided for the transistor by making this device a depletion mode MOSFET and grounding its gate, or an enhancement device with the gate connected.

Thus MOSFET can have a high at to achieve low leakage and a low and to achieve high speed. This dynamic variability becomes more beneficial for *low power* operation at very low voltages. By tying the gate and the body of an SOI MOSFET together, a Dynamic Threshold Voltage MOSFET (DTMOS) is obtained. DTMOS has the theoretically ideal subthreshold swing and higher carrier mobility than the standard MOSFET. Furthermore, DTMOS threshold voltage drops as the gate voltage is raised, resulting in a much higher current drive than a conventional bulk or SOI MOSFET. As the ac and dc experimental and simulation results demonstrate, DTMOS is a good candidate for very low voltage operation. DTMOS also solves the floating body problems of SOI MOSFET's such as transient kink and stability. DTMOS can also be implemented in a bulk technology.

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