A Specification Review Report on

IEEE 802.11 MAC Chip

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Scope Of The Project:

To Design and Implement the MAC (Medium Access Control) architecture for Wireless LAN based on IEEE-802.11 Standard. The complete MAC architecture is to be divided into Host software (running on Host Processor) and hardware (FPGA to be used in the NIC card).

The partition in H/w and S/w is based on the time critical functions and logic resource requirements for different modules in the architecture. The design would be tested on Altera FPGA APEX20K, with Altera suite Quartus II, with Leonardo Spectrum Synthesis tool and ModelSim simulator. The design would be done in Verilog HDL. Efficient Test Benches needs to be designed for efficient Target Testing**.** Area, delay and power optimization need to be done. Proven design to be used for ASIC.

The task also includes the development of host driver, design document and hardware architecture document. The work is to be carried out at Ittiam Systems and CEDT.

Technical Specifications

- Fully compliant to IEEE 802.11 Standard 1999
- Timing Synchronization algorithms
- Compatible with IEEE 802.11 a/b/g, PHY (BB)
- Support for all LLC like SNAP and HDLC
- Complete system featuring dedicated hardware and software
- Flexible design to allows upgrade for 802.11e QoS and 802.11i Security provisions
- Portable STA or AP
- Both IBSS (Ad-hoc networks) or Infrastructure network support
- DCF & PCF (optional) operation
- Power Management & control
- WEP encryption
- Interface to allows simple bridging to a range of host interfaces
- Verilog HDL source code
- Synthesis and test scripts
- Test vectors & test benches
- Simulation and synthesis reports, user and reference manuals
- High quality design documentation that includes
- Hardware architecture Document
- Programming guide
- Design document
- Fully synthesizable and optimized for low gate count
- Considerations for easy ASIC integration

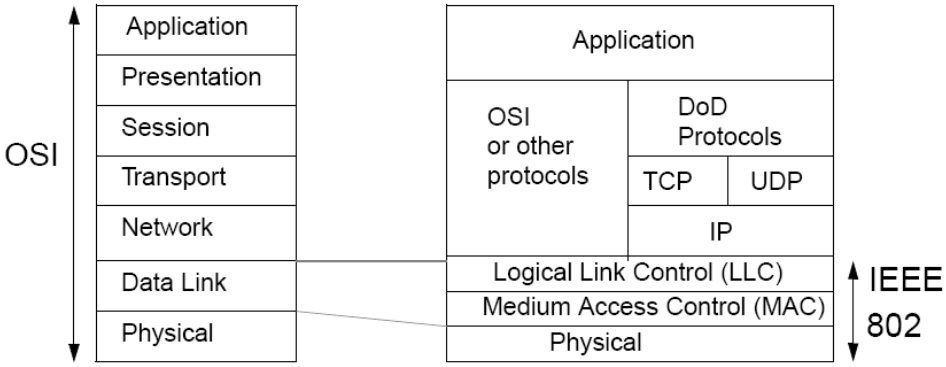
Deliverables

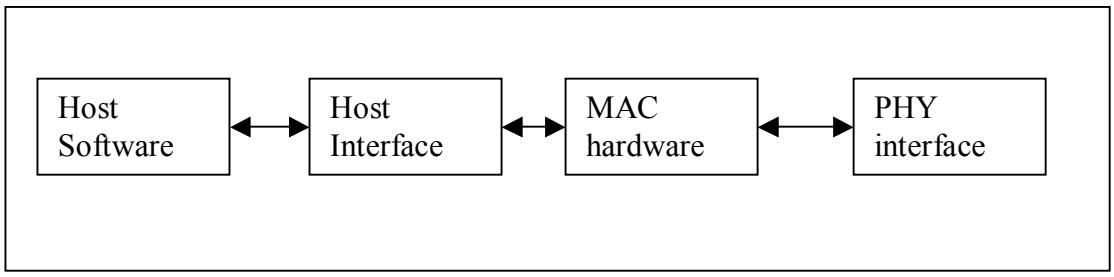
Hardware

• Verilog Synthesizable source code
• User Manual for hardware
• Test bench, Test Cases & Test Design Document
• Sample Synopsis scripts for synthesis

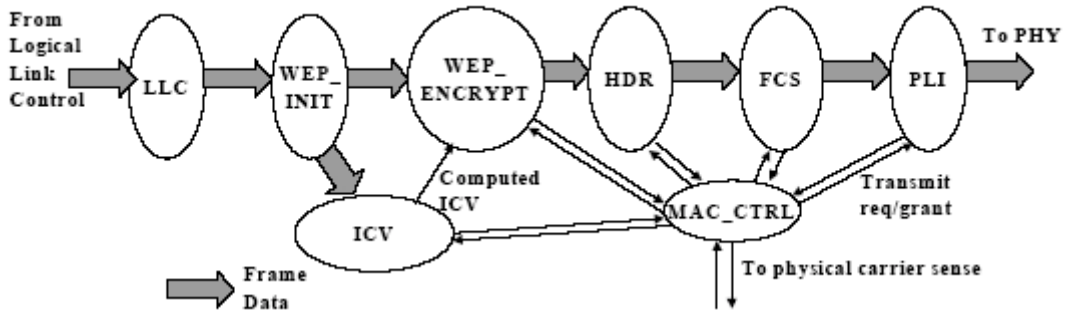
Software

• C Source Code
• Programming guide for Firmware
• OS support
• Porting guide for Firmware

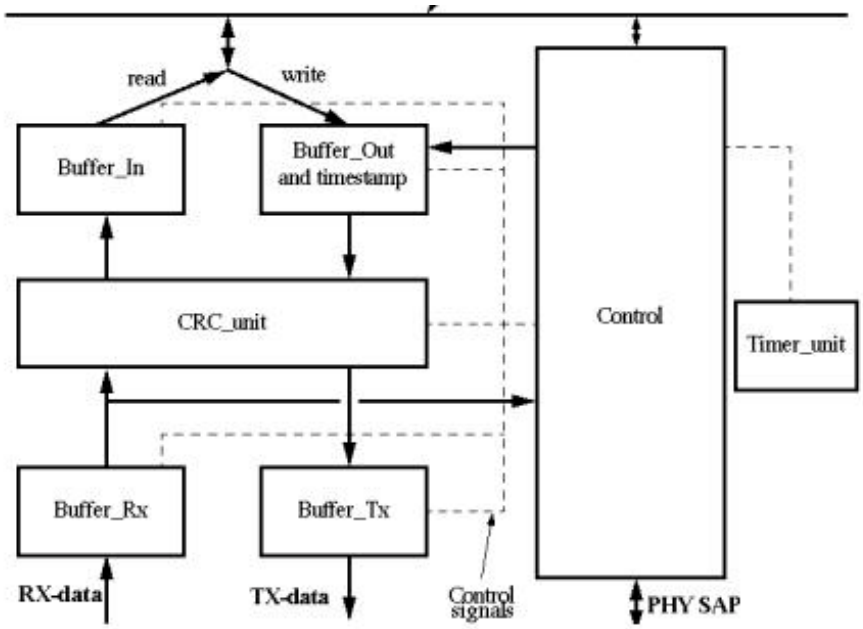




Functional Flow Graph



Functional Block Diagram



Identified Modules in 802.11 MAC

- PHY interface (Baseband Communication)
- Host Interface (LLC Interface)
- Timers and Clocks (Synchronization Logic)
- CRC generator
- WEP block (Encryption and Decryption)
- MLME (MAC Layer Management Entity)
- Data and Control Frame Module
- Virtual Carrier Sensing (NAV)
- State Machines (Tx & Rx)
- FIFO and Registers (Tx & Rx)
- Power Management
- DMA and Interrupt Controller

Estimated Project Time Plan

Task_Name	Duration	Start Date	Finish Date	Status
Pre-study phase	**70**	**25/08/03**	**20/11/03**	**60% Complete**
Familiarization with current standard for background	32	25/8/03	1/10/03	90% Complete
Understanding IEEE standard and References	24	25/9/03	25/10/03	60% Complete
Architectural block division according to functionality	23	10/10/03	10/11/03	Started
Partitioning blocks into Hardware and software	32	10/10/03	20/11/03	Started
Preparing Pre-study phase report	12	31/10/03	15/11/03	Awaiting Data
Learning Tools	85	1/9/03	15/12/03	Started
Development Stage	**102**	**01/01/04**	**30/04/04**	
Verilog HDL coding for hardware	75	1/1/04	30/3/04	New Task
Writing test vectors and test benches	28	15/3/04	15/4/04	New Task
Software coding and Interface Design	51	2/2/04	31/3/04	New Task
Preparation for testing and evaluation	14	15/4/04	30/4/04	New Task
Preparing Design Documents	18	10/4/04	30/4/04	New Task
Engineering and Optimization Stage	**28**	**01/05/04**	**31/05/04**	
Code Optimization	7	3/5/04	10/5/04	New Task
Automation of test benches	10	11/5/04	21/5/04	New Task
Resolving pre and Post Synthesis simulation	20	3/5/04	25/5/04	New Task
Final phase	**26**	**01/06/04**	**30/06/04**	
Final Report	12	1/6/04	14/6/04	New Task
Demo Evaluation and Expo	7	23/6/04	30/6/04	New Task