E3-227: Home Work 5 (Due 10/3/03)

Using DIOS process simulator and appropriate processing sequence and parameters, obtain the transistor structure that you had designed in HW-4. Start with a p-type Si wafer with $10^{16}/cm^3$ doping concentration. You can use the following file as a template:
/usr/packages/ISE/tcad/current/database/GettingStarted/Dios/GettingStarted_advanced/dio.cmd
and modify the flow in this file according to the one given in Table 1 of the enclosed paper which uses disposable spacer technique (pdf file enclosed with this email). In order to control the off state current below 0.1nA/μm , optimize and use an appropriate halo implantation dose. Don't change SSRC condition. You have to generate both NMOS device and PMOS device with this leakage constraint.

(a) For your optimized device, plot the doping concentration at the same locations as that of HW4.
(b) For the optimized NMOS and PMOS 0.1μm device, tabulate Ion, Ioff, and Vt .

With this process generated device as the reference, perform following simulations only for NMOS transistor:

(c) For the same set of 5 devices (used in HW4), generate linear and saturation Vt roll-off plots.
(d) Obtain the DC performance metric for this transistor design, i.e. plot Ioff vs Ion. which is generated through simulation on different channel lengths
(e) For the drain junction, obtain the junction capacitance as a function of Vd, by sweeping Vd from 0V to 1.5V. Gate, Source and Substrate are at GND. (Note: the junction capacitance is between drain and body terminal).

Home Work -5

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Using DIOS process simulator the NMOS transistor has been designed by optimizing halo implantation dose to 3.8e+13 and Energy=7Kev leakage current of 0.0804 nA/µm was obtained (keeping other parameters as given in the paper).

(a)

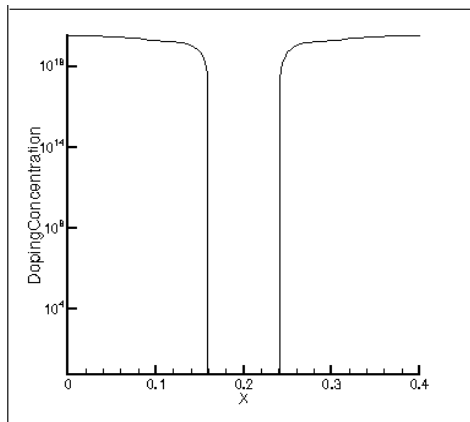


fig. (a) Doping Conc. For X=100A

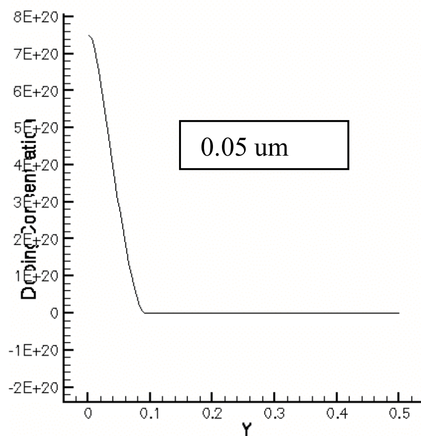


fig.(b) Doping Conc. For Y=0.05µm

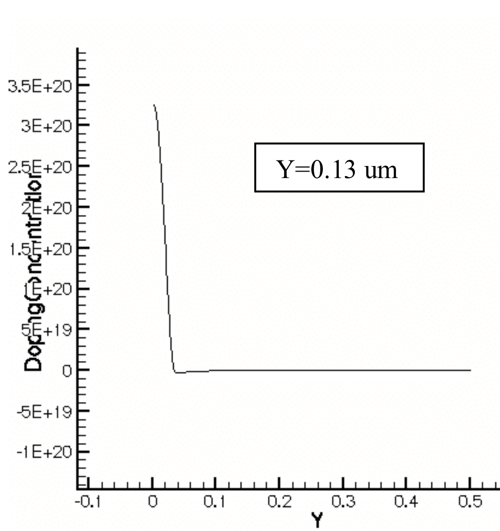


Fig. (c) Doping Conc. For Y=0.13µm

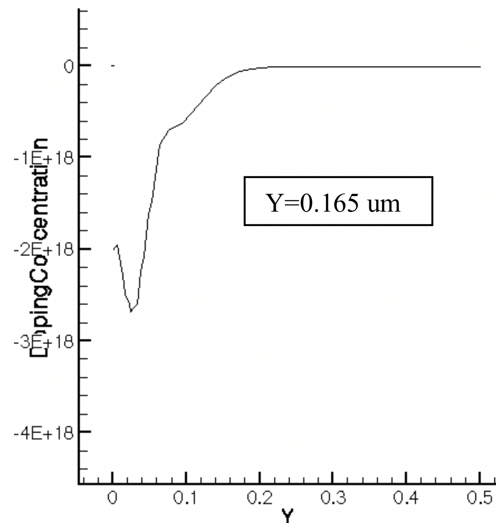


fig. (d) Doping Conc. For Y=0.165µm

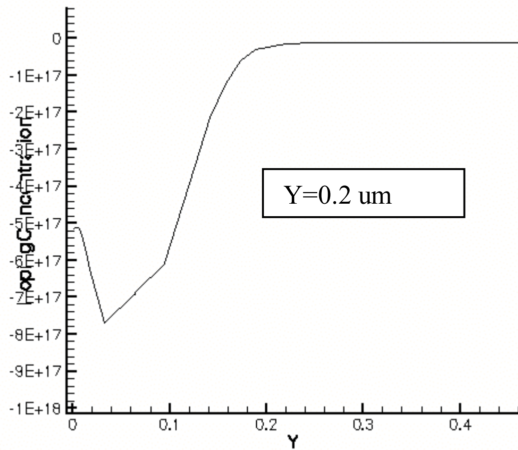
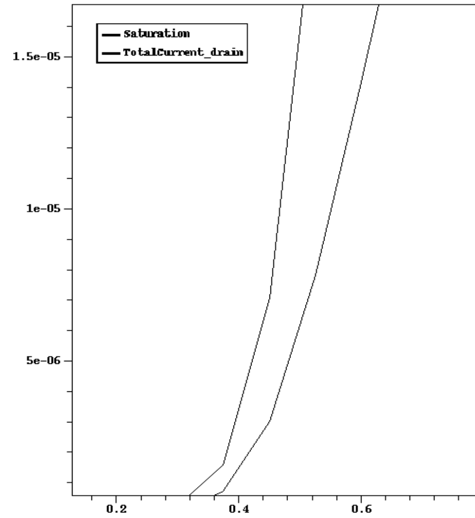


fig. (e) Doping Conc. For Y=0.2μm



fig(f) I_D vs. V_{GS} plot for 0.1 μm NMOS

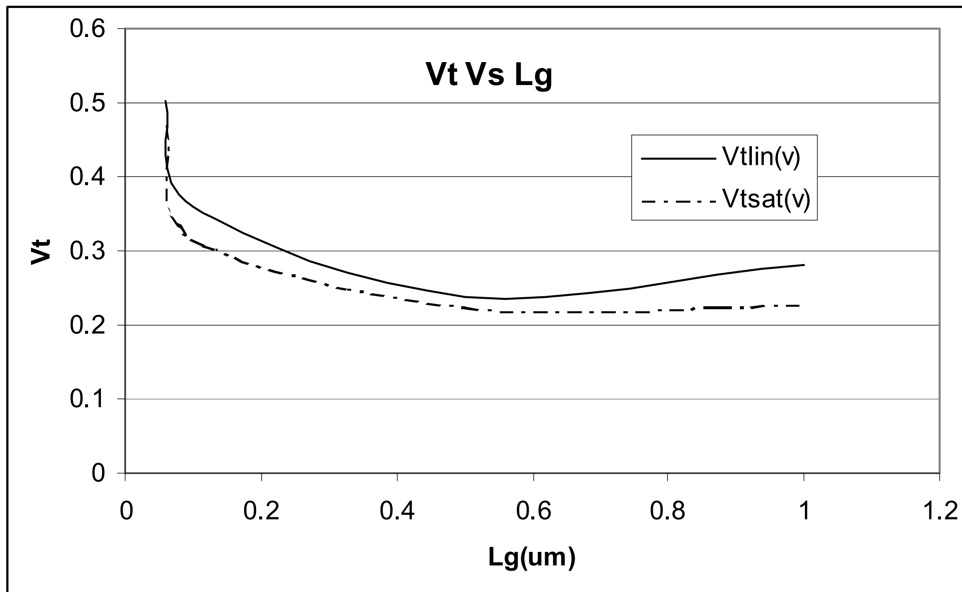
(b) For the optimized NMOS and PMOS 0.1μm device, tabulate Ion, Ioff, and Vt .

NMOS						PMOS					
I_{OFF} (pA)		I_{ON} (μA)		V_T (v)		I_{OFF} (A)		I_{ON} (A)		V_T (v)	
Lin.	Sat.	Lin.	Sat.	Lin.	Sat.	Lin.	Sat.	Lin.	Sat.	Lin.	Sat.
33.9	80.4	83.2	505	0.359	0.317						

For NMOS and PMOS the graphs are shown below
With this process generated device as the reference, perform following simulations only for NMOS transistor:

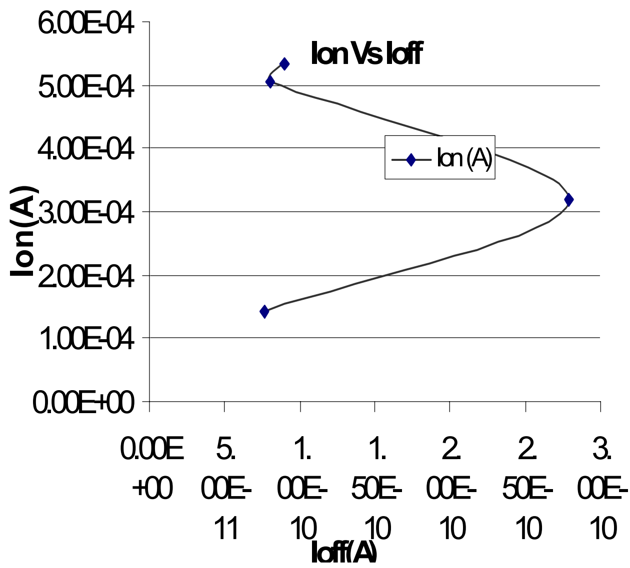
	Vt (v)		Linear		Saturation	
L_g(um)	**Vt_{lin}(v)**	**Vt_{sat}(v)**	**I_{off}(pA)**	**I_{on}(μA)**	**I_{off} (pA)**	**I_{on} (mA)**
0.06	0.504	0.466	3.19	100	90	0.535
0.1	0.359	0.317	33.8	83	80.4	0.505
0.2						
0.5	0.238	0.223	170	38	279.4	0.32
1.0	0.281	0.226	27.2	23.0	76.3	0.143

For the same set of 5 devices the linear and saturation Vt roll-off plots are shown in the fig.(g)

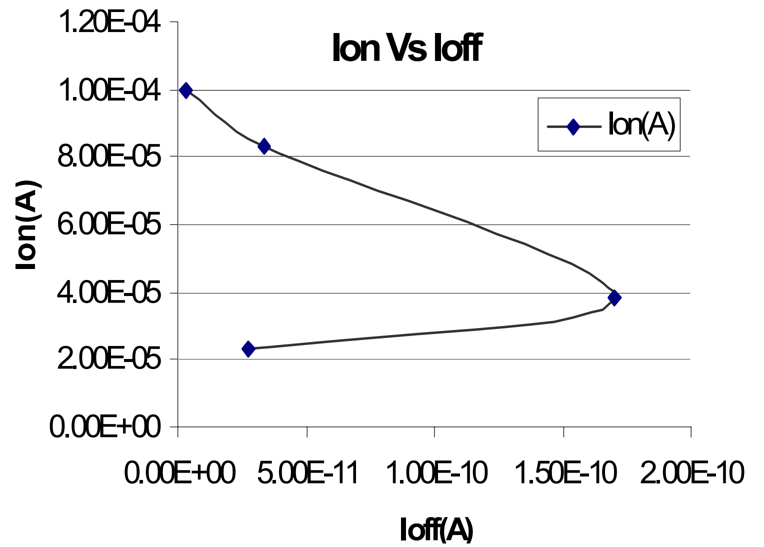


Fig(g) Vt Roll off plot

(d)the plot for Ioff vs Ion. on different channel lengths



fig(h)Ion vs. Ioff in saturation



fig(i)Ion vs. Ioff in Linear

(e)For the drain junction, the junction capacitance as a function of Vd is obtained by sweeping Vd from 0V to 1.5V. The graphs for Drain-Subs. Junction cpacitance is shown

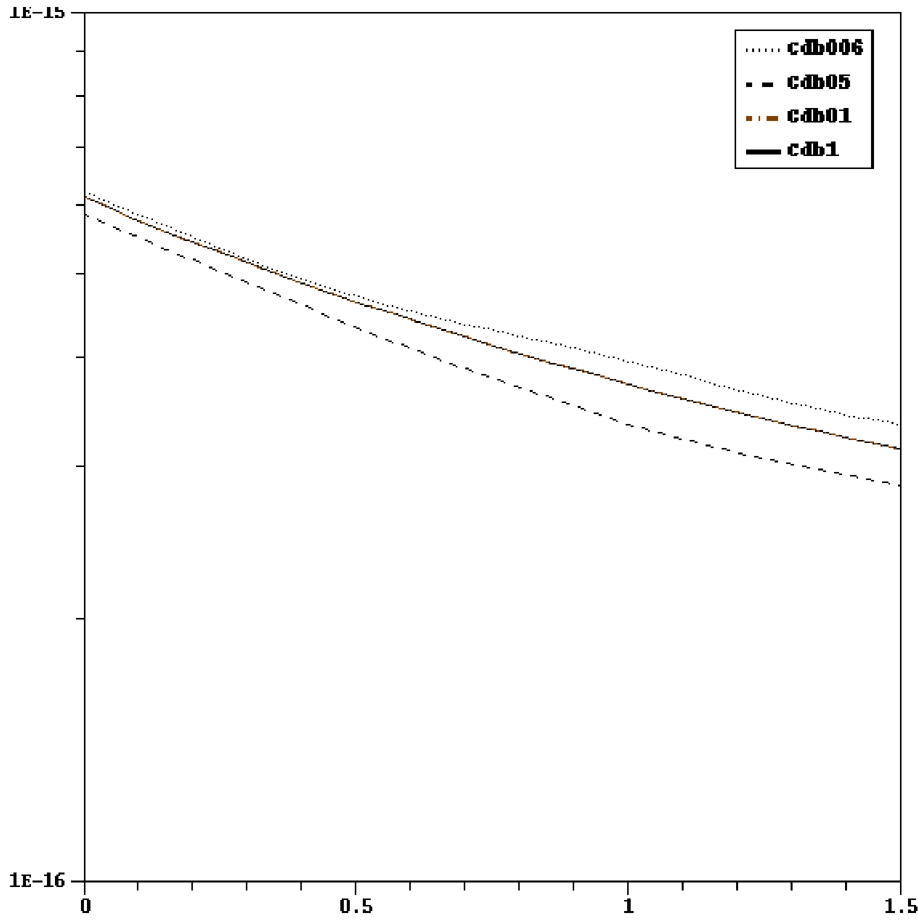


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Fig.(j) C_{DB} for diff. L_g's

Supplement to Home Work -5

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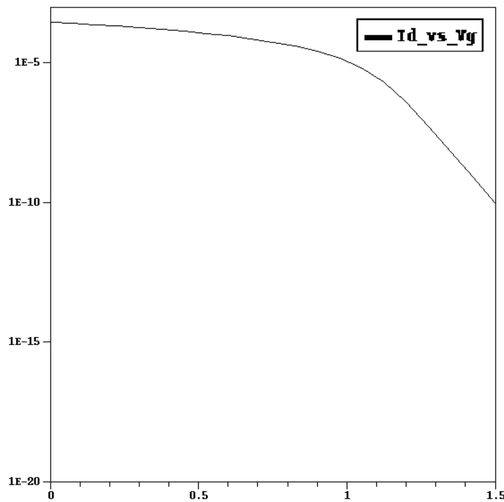
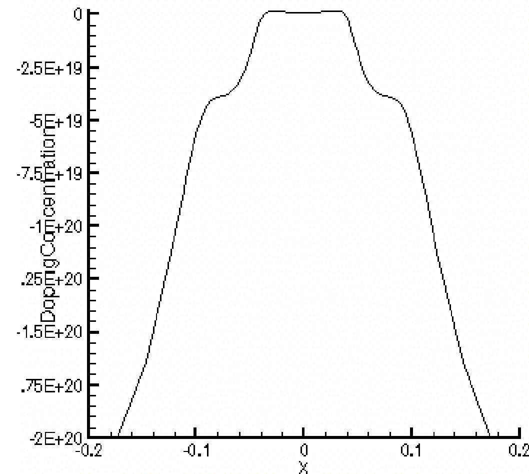
Using DIOS process simulator the PMOS transistor has been designed by optimizing halo implantation dose to 5.35e13/cm^2 and Energy = 30 Kev leakage current of 0.0919nA/µm was obtained (keeping other parameters as given in the paper).
The readings for NMOS 0.2µm are also enclosed with V_t roll off and I_{ON} vs. I_{off} plot.

(b) For the optimized NMOS and PMOS 0.1µm device, Ion, Ioff, and Vt . are tabulated:-

NMOS						PMOS					
I_{OFF} (pA)		I_{ON} (µA)		V_T (v)		I_{OFF} (pA)		I_{ON} (µA)		V_T (v)	
Lin.	Sat.	Lin.	Sat.	Lin.	Sat.	Lin.	Sat	Lin.	Sat.	Lin.	Sat.
33.9	80.4	83.2	505	0.359	0.317	2.12	91.9	235	65.9	-.43	-.307



Fig(a) I_d vs V_g char.



Fig(b)Doping Conc. at X=100Å

Fig.(c) Doping Conc. at Y=0.05µm

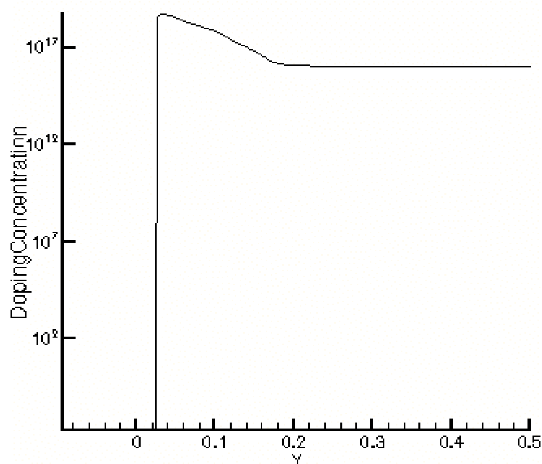
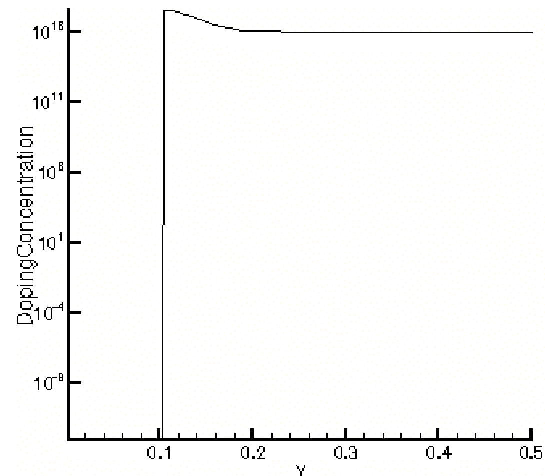
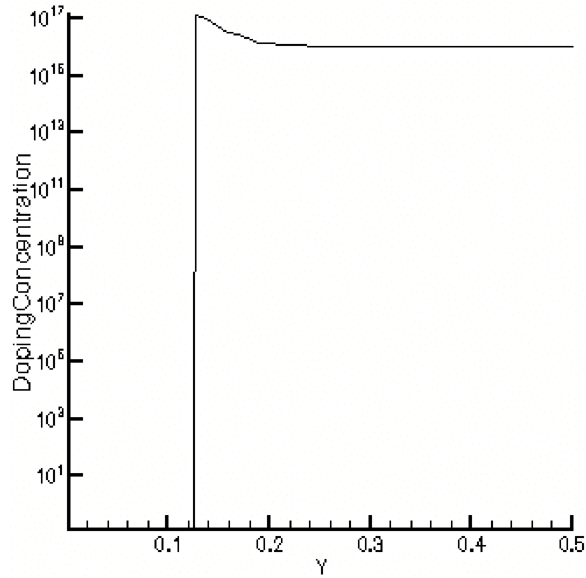
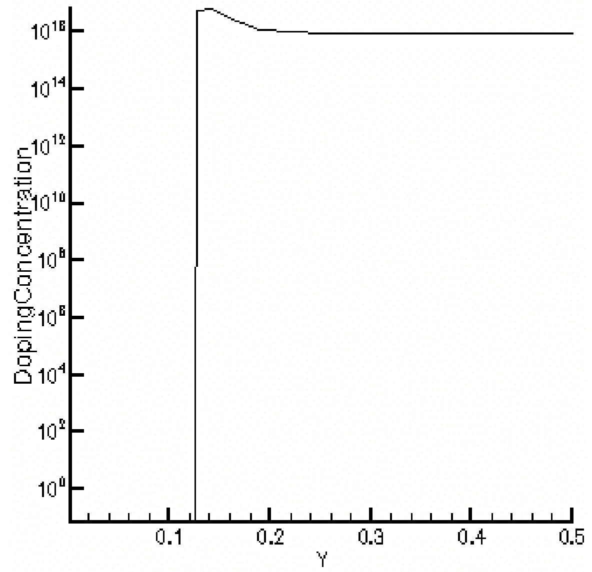


Fig (d) Doping Conc. at Y=0.13µm



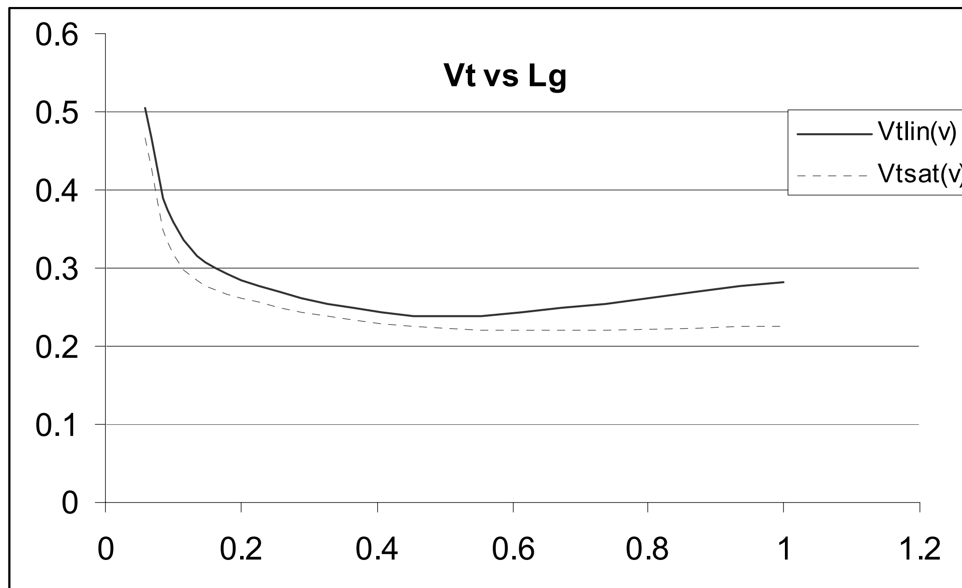


Fig(e) Doping Conc. at Y=0.165µm



Fig(f) Doping Conc. at Y=0.2µm

	Vt (v)		Linear		Saturation	
L_g(um)	Vt_{lin}(v)	Vt_{sat}(v)	I_{off}(pA)	I_{on}(µA)	I_{off} (pA)	I_{on} (mA)
0.06	0.504	0.466	3.19	100	90	0.535
0.1	0.359	0.317	33.8	83	80.4	0.505
0.2	0.284	0.261	251.3	67	418	0.469
0.5	0.238	0.223	170	38	279.4	0.32
1.0	0.281	0.226	27.2	23.0	76.3	0.143



Fig(g) Vt Roll off plot

Th.e plot for Ioff vs Ion. on different channel lengths is as shown in the figure

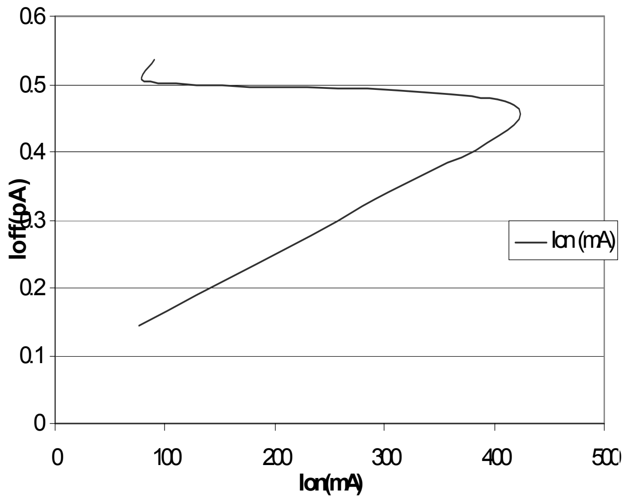


Fig.(h) Ion vs. Ioff in saturation

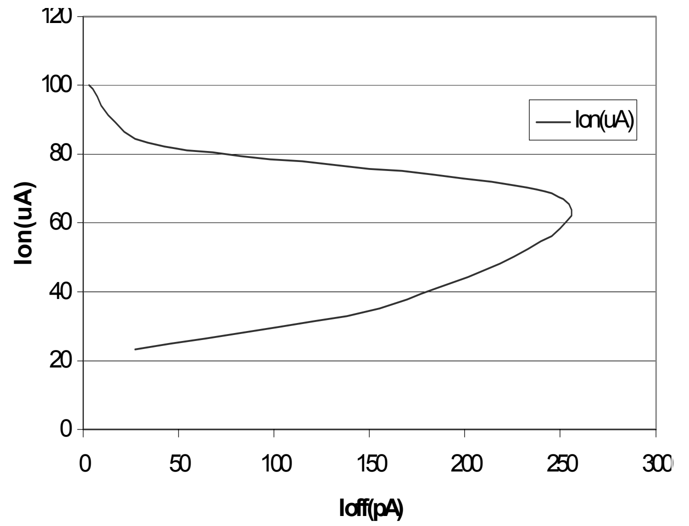
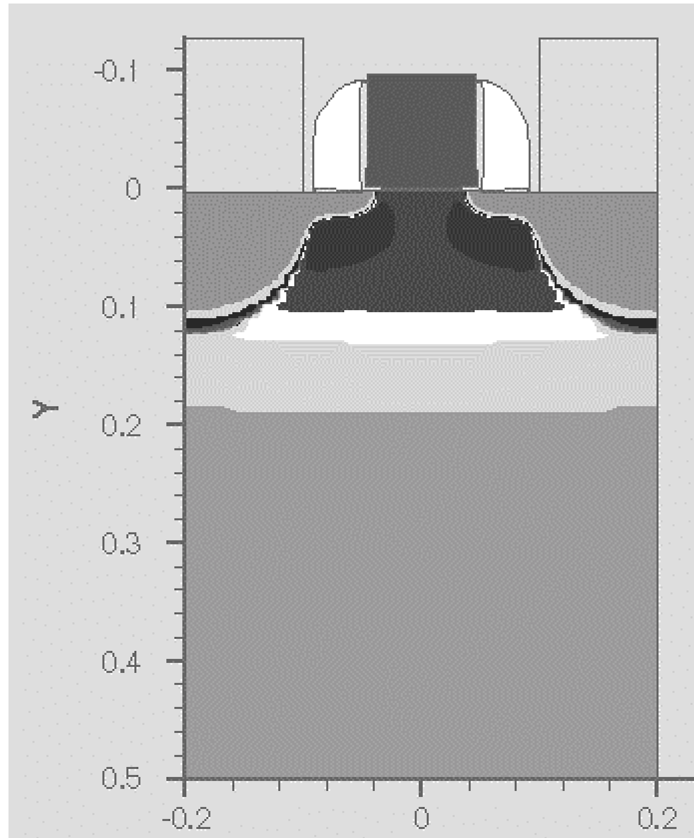


fig.(i) Ion vs. Ioff in Linear



Typical PMOS Device Structure as seen in Tecplot