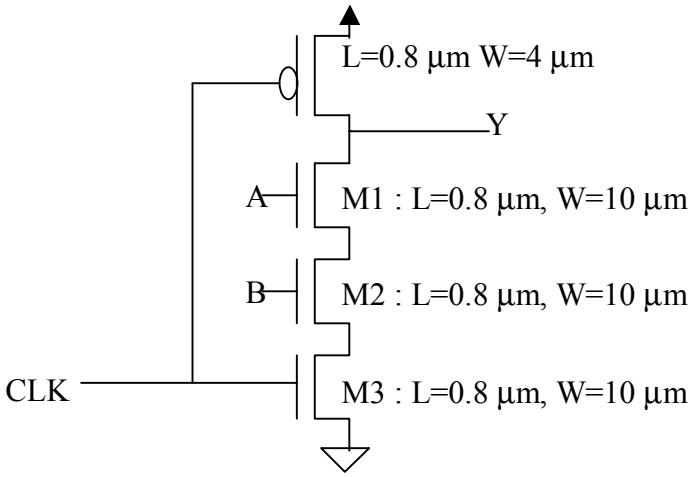
E0-284 : Home Work - 5

Due on 22-10-2002

(1) Consider a two input dynamic NAND gate shown in Fig.1 . The important figure of merit for this gate is high to low delay during evaluation phase (A=B=1) and also the noise at Y due to charge sharing during evaluation (A=1, B=0). For the circuit shown, calculate the falling delay (Tp_{HL}) when A=B=3.3V during evaluation. Use CLK rise time of 1pS. Also determine the effect of charge sharing i.e. the value of node voltage at Y (Vy) when A=3.3V and B=0V during evaluation phase.

(2) Repeat above exercise for following 2 modifications:
   (a) Connect a weak PMOS (L=2μm and W=1μm) between Vdd and Y, with its gate at ground.
   (b) Connect a weak PMOS (L=2μm and W=1μm) between Vdd and Y, however, the gate is driven by an inverter (NMOS : L=0.8μm and W=2μm ; PMOS: L=0.8μm and W=4μm) whose input is connected at Y.



(3) Consider the circuit configuration corresponding to Prob. 2(a). (i.e. dynamic NAND with grounded gate weak PMOS). Suppose that A=3.3V and B=0 and clock frequency is 10MHz (rise and fall time 1pS). Suppose that there is a noise pulse at B (during evaluation phase) whose duration is 10% of the clock period. Using simulation obtain the impact on node voltage Y as a function of the amplitude of the noise pulse. Use following values for the amplitude of noise pulse: 0.5V, 1V, 1.5V, 2V, 2.5V and 3V.

NOTE: You are required to demonstrate the simulations in the lab to the lab instructors. Further you are required to submit one page summary of your findings by 22nd October. If you submit more than one page report then you will be penalized for the extra pages that you submit.

HW-5

REPORT

Q.1

For the two input dynamic NAND gate when A=B=3.3V is **$Tp_{HL=}$ 0.1814ns**

The effect of charge sharing during the evaluation phase with the condition A=3.3V and B=0V is that the output voltage drops since with A High the transistor conducts & the initial V(Y)=3.3v is shared between the load capacitance & the output capacitance of the transistor(with gate input A) Also due to this the voltage at the source of this transistor rises to 2.6 volts which in ideal case should be zero.

Q.2

A) With weak PMOS (its gate at ground) when A=B=3.3V **$Tp_{HL=}$ 0.23995 nsec**
The Tphl is increased as compared to the Tphl without Weak PMOS. It is because the weak PMOS opposes the discharge of output capacitor.

In this case since there is a weak PMOS, which always conducts, therefore the output voltage doesn't drops below 3.3v due to charge sharing. Although the Transistors still share the charge but this extra charge (for V(Y)=3.3v) is supplied from the supply by weak PMOS.

B) With weak PMOS(the gate is driven by an inverter) when A=B=3.3V **$Tp_{HL=}$ 0.283 nsec.**
The Tphl is increased as compared to the Tphl with Only Weak PMOS. It is because the one inverter is connected at output stage which introduces its own output capacitor in addition.

However in this case the weak PMOS conducts only when V(Y)is High & thus keeps the V(Y)=3.3v.When the output is low this weak PMOS doesn't conducts & thus it reduces static power dissipation.

Q.3

For the noise pulse at B (during evaluation phase) with duration 10% of the clock period for varying noise levels at B As is shown in the table the value of output voltage starts reducing faster as the noise voltage level (at B) is increased. Also the duration for which the output voltage drops increases with noise voltage. This is due to the fact that during this noise voltage pulse is present it provides discharge path for the output.

Noise pulse at B(volts)	Output voltage (volts)	Time Duration for which the output goes low (nsec)
.5	2.88	7.76
1	0.15	13.15
1.5	0.068	14.59
2	0.0545	14.62
2.5	0.0484	14.62
3	0.045	14.82

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