E0-284 : Home Work - 4

Due on 8-10-2002

(1) Consider a 2 stage CMOS inverter with Ln=Lp=0.8µm and Wn=1.2µm and Wp=3.6µm. If Vin=0V, then determine the static power dissipation. If Vin is square wave with frequency of 100MHz with rise and fall time of 1pS, then what is the power dissipation? If the input rise and fall time is increased to 500pS, then what is the power dissipation?

(2) For the above circuit generate a plot of the power dissipation vs. frequency with Vdd as parameter. i.e. with Vdd=3.3V, plot P vs f for f varying from 100 Hz to 100 MHz. Then change Vdd to 3V, 2.5V, 2.0V, 1.5V, 1.0V and generate similar plots. For all the simulations in this problem use input rise and fall time of 1pS.

(3) Realize 2 input XOR gate using two different logic styles namely fully static CMOS logic and Pass gate logic (tiny XOR discussed in class). Also layout the 2 circuits using L-Edit. Compare the two implementations with respect to area , power, delay. For the power, delay calculations consider 4 different cases of input sequences: (All rise and fall times are 1pS)
   (a) Initial condition: A=B=1; then A changes from 1 to 0.
   (b) Initial condition: A=B=1; then B changes from 1 to 0.
   (c) Initial condition: A=B=0; then A changes from 0 to 1.
   (d) Initial condition: A=B=0; then B changes from 0 to 1.

NOTE: You are required to demonstrate the simulations in the lab to the lab instructors. Further you are required to submit one page summary of your findings by 8th October. If you submit more than one page report then you will be penalized for the extra pages that you submit.

Report:HW-04

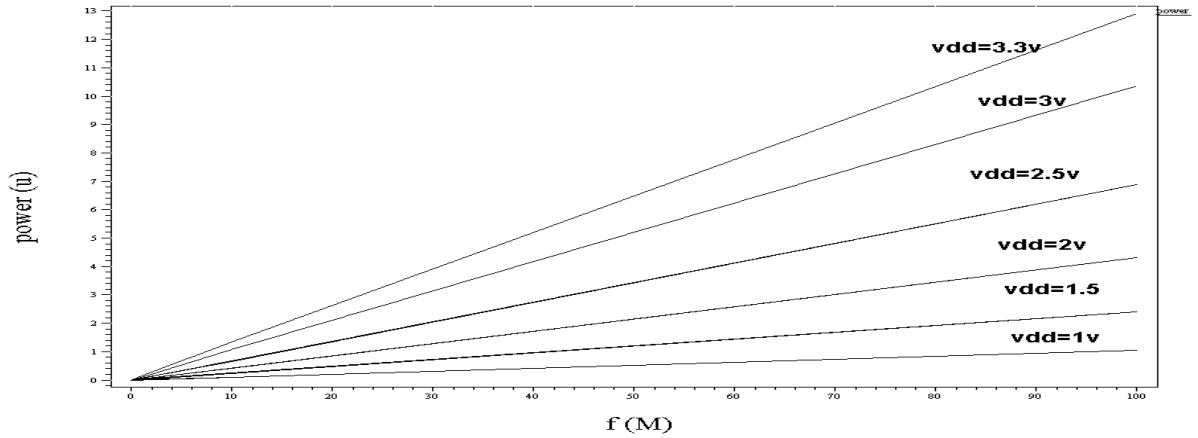
Q1

Ln=Lp=0.8µm and Wn=1.2µm and Wp=3.6µm f=100MHz

Static power dissipation	Dynamic power dissipation Rise time =fall time= 1psec	Dynamic power dissipation Rise time =fall time= 500psec
1.085416e-011 watts	1.809252e-005 watts	2.166708e-005 watts

Ideally the static power should be zero but it is not the case here as because of the subthreshold Leakage current an it is very less than dynamic power.

Q2



Q3

	(L edit)Pass gate logic		fully static CMOS	
Sequences	**Tplh**	**Power dissipation**	**Tplh**	**Power dissipation**
A=B=1 then A=0	.67715n	4.475uW	2.4622ns	7.095515 uW
A=B=1 then B=0	.72859n	4.35556 uW	3.2863ns	7.809971 uW
A=B=0 then A=1	.78762n	4.475 uW	4.6604ns	12.19751 uW
A=B=0 then B=1	.38044n	4.3556 uW	2.6176ns	9.216341 uW

	(tspice)Pass gate logic	
Sequences	**Tplh**	**Power dissipation**
A=B=1 then A=0	.1485n	1.27uW
A=B=1 then B=0	.16n	0.88 uW
A=B=0 then A=1	.1792n	1.27 uW
A=B=0 then B=1	.03744n	.88 uW

AREA:

PASS GATE LOGIC :- **active area**:1634 sq lambda / **total area**:-6390 sq. lambda

FULLY STATIC CMOS:- **active area**: 2653 sq lambda/ **total area**:-9936 sq. lambda

SUBMITTED BY
AGNISH JAIN (ME I MicroE)
HEMANT PARATE (ME I MicroE)