E0-284 : Home Work - 3

Due on 1-10-2002

(1) (a) Consider a 2 stage CMOS inverter with Ln=Lp=0.8μm and Wn=1.2μm and Wp=3.6μm. The second stage is loaded by a load capacitor of 100fF. This inverter is driven by a square wave input *Vin* with frequency of 100MHz with a rise and fall time of 1pS. Obtain the voltage waveform at the output of first and second inverter (*Vout1* and *Vout2*). Estimate Tp_{HL} and Tp_{LH}. (Note: for the second stage the propagation delay for Vout2 is defined with respect to *its input* which is Vout1). Determine the impact on the propagation delay if the rise and fall time is changed to 10pS , 100pS and 500pS.
(b) Suppose the width of all transistors in this 2 stage inverter is increased by a factor of 10. (L is not changed). What is the impact on propagation delay of first stage and second stage. (Use input with rise and fall time of 1pS). Do you expect them to change by same amount? Why or why not?

(2) Design a buffer to drive a large load capacitance of 1pF. Assume that the first stage has to be a minimum size inverter with matched N and P delays (i.e. for the first stage, choose Ln=Lp=0.8μm; and Wn=1.2μm and Wp=3.6μm. This inverter has a gate capacitance of about 13fF for the 0.8μm technology that you are using). Through simulations, estimate the optimum number of stages and the corresponding stage ratio which minimizes the propagation delay from input to the output of the buffer. What is the rising delay (Tp_{LH}), falling delay (Tp_{HL}) and average delay ($(Tp_{LH} + Tp_{HL})/2$. Use L-Edit to layout the buffer that you have designed. What is the area consumed by the buffer? If you use *folded transistor* layout for final stage of the buffer, how much delay improvement, if any, is obtained compared to the *non folded* layout?

(3) Skewing of transistors in gates refers to deviating from βn=βp condition. Depending on circuit application, skewing may be required to speed up the circuit if we are concerned only with the propagation delay of rising or falling edge through the gates. Consider the buffer that you have designed in (2).

(a) Suppose that we are interested in only the rising edge and not the falling edge. Then the widths of all transistors that come in the falling edge path can be decreased. i.e. the NMOS width of final stage (n^{th} stage), PMOS width of preceding stage ($n-1^{th}$ stage) can be decreased and so on… all the way to the first stage. Decrease the widths of appropriate N and P transistors in your buffer by a factor of 2. (The minimum width allowed in this technology is 0.8μm). What is the improvement in the rising edge delay and what is the degradation in the falling edge delay? How are you getting the improvement in rising edge without changing the transistors that come in the rising edge path? Also estimate the average delay.

(b) Suppose that we are interested in only the falling edge and not the rising edge. Then the widths of all transistors that come in the rising edge path can be decreased. i.e. the PMOS width of final stage (n^{th} stage), NMOS width of preceding stage can be decreased ($n-1^{th}$ stage) and so on… all the way to the first stage. Decrease the widths of appropriate N and P transistors in your buffer by a factor of 2. (The minimum width allowed in this technology is 0.8μm). What is the improvement in the falling edge delay and what is the degradation in the rising edge delay. How are you getting the improvement in falling edge without changing the transistors that come in the falling edge path? Also estimate the average delay.

NOTE: You are required to demonstrate the simulations in the lab to the lab instructors. Further you are required to submit one page summary of your findings by 1st October. If you submit more than one page report then you will be penalized for the extra pages that you submit.

REPORT : HW- 3

Q1.

	Output 1		Output 2	
Rise & fall time	Tphl(sec)	Tplh(sec)	Tphl(sec)	Tplh(sec)
1ps	3.4766e-010	2.6998e-010	2.3713n	1.2631n
10ps	3.1871e-010	2.6252e-010	2.3880n	1.3242n
100ps	3.9948e-010	2.5304e-010	2.3859n	1.2910n
500ps	4.3134e-010	3.4848e-010	2.3786n	1.1520n
Wnew=10xW Tr=tp=1ps	3.5135e-010	2.2915e-010	4.8303e-010	3.4853e-010

When changing the width & length to 10 times the tphl & tplh of first stage will not be affected since the first stage capacitor increases so the increase in current is nullified & delays remain essentially the same.However in the second stage since the load capacitor is very large so the change in cap. Is negligible but the current is increasing by 10 times so there is appreciable change in the delays

Q.2 From the readings of simulation optimum no. of inverters required for the Multiple stage Buffer are 4 for the PMOS transistors designed a(=3) times wider then the NMOS devices(where a=(W/L)p/(W/L)n).

No. of stages	(sec)	a=2.6	a=2.8	a= 3	a= 3.2	a=3.4
3 stage	Tplh	3.7763n	3.6377n	3.5471n	3.4886n	3.4589n
	Tphl	5.1030n	4.7908n	4.5618n	4.3931n	4.2773n
	Avg	4.443 n	4.213 n	4.054 n	3.941 n	3.687 n
4 stage	Tplh	3.9130n	3.8356n	**3.8240n**	3.8447n	3.8950n
	Tphl	3.7346n	3.7555n	**3.8087n**	3.8758n	3.9644n
	Avg	3.823 n	3.795 n	**3.816 n**	3.859 n	3.929 n
5 stage	Tplh	4.1891n	4.1697n	4.2252n	4.3072n	4.4323n
	Tphl	3.8250n	3.9006n	4.0067n	4.1268n	4.2647n
	Avg	4.007 n	4.034 n	4.115 n	4.2165 n	4.348 n

	Tphl (sec)	Tplh (sec)	TOTAL AREA	ACTIVE AREA
UNFOLDED	4.5291n	4.5624n	36562Sq.lamb	18482Sq. lamb
FOLDED	4.5095n	4.5471n	44709Sq.lamb	15384 Sq. lamb.

from simulation it is observed that ther is improvement in tplh & tphl by magnitude 0.0153n & 0.0196n sec .respectively.

Note:In L-edit every successive stages is scaled by a factor of 3.

Q.3

(a) tplh = 1.8065n sec tphl = 4.4829n sec

(b) tplh = 4.1614n sec **tphl = 2.1241n sec**

In case **(a)** we are scaling NMOS of final stage its gate cap. Cg reduces so the prev stage will discharge quickly (smaller input cap.)and PMOS of n-1th stage is scaled so n-2th stage will charge quickly through reduced cap. of n-1th stage pmos. In this way over all tplh will get improved but at cost of tphl which degrades because of reduced discharging and charging current of nth and n-1th stages and so on.

(b) Here just the opposite happens i.e the final stage PMOS Cg reduces(due toW/2) which causes quick charging the n-1th stage NMOS width reduced by half causes fast discharge & so on.

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