E0-284 : Home Work - 2

Due on 17-09-2002

(1) Simulate and plot the DC transfer characteristics of inverters with following specs. In all the cases the inverting device (pull down) has L=0.8µm and W=1.2µm.
   (a) Resistive load inverter such that V_{OL} < 0.4V for V_{in}=3.3V. What is the required value of the resistance?
   (b) Saturated NMOS load inverter such that V_{OL} < 0.4V for V_{in}=3.3V. What is the required W and L of saturated load transistor?
   (c) Grounded gate PMOS (Psuedo NMOS) inverter such that V_{OL} < 0.4V for V_{in}=3.3V. What is the required W and L of the load transistor?

(2) For the inverters in 1 (b) and (c) do the layout using LEDIT. Compare the areas of the inverters in two cases. Further, extract the schematic from layout and verify the functionality.

(3) (a) Simulate and plot the DC transfer characteristics of active load CMOS inverter with the inverting device (pull down) dimension of L=0.8µm and W=1.2µm. Choose load PMOS such that the V_{INV} point is at 1.65V (V_{dd}/2). What is the required W and L of the load transistor.
   (b) Now increase W of the load device and keep L constant to the value obtained in (a). Plot the effect of increasing W on the transfer characteristics.
   (c) Now increase L of the load device and keep W constant to the value obtained in (a). Plot the effect of increasing L on the transfer characteristics.
   (d) Using LEDIT layout the inverter in (a) and compare the area with the other inverters in (2).
   (e) Extract the schematic from the layout and verify the functionality.

(4) For the inverters in 1 (a), (b) , (c) and 3(a) estimate the noise margin for logic LOW and logic HIGH.

NOTE: You are required to demonstrate the simulations in the lab to the lab instructors. Further you are required to submit one page summary of your findings to me by 11th September. If you submit more than one page report then you will be penalized for the extra pages that you submit.

Report of Home-Work 2

Vol <0.4v ,Vin=0 to 3.3 v

	Spec of load	Voh v	min	Vol max	Vil max	Vih Min	Nmh	Nml
1a.**Resistive load**	R > **80.55**k	3.3	3.1	0.8	0.62	2.1	1.0	0.18
1 b. **Saturated** NMOS	W/L=**0.595**, W=1.2u L=2u	3.3	2.39	0.85	0.38	1.67	0.72	0.47
1 c. Grounded PMOS	W/L=**1.065** W=1.2u L=1.2u	3.3	2.9	0.71	1.15	2.25	0.65	0.44
3 a. CMOS (at Vinv)	W/l=3.0 W=3u L=0.8u	3.3	2.93	0.34	1.42	2.08	0.85	1.08

Ans.1a-The required value of R=81k

b-The load transistor is saturated NMOS for which the W= 1.2u& L=2u

c-The load transistor is Gnd. Gate PMOS for which the W= 1.2u & L=1.2u

Ans-2 a.Using L-Edit for Q1b ie. Saturated NMOS

Area of transistor= 121+242+275=638sq.um

b.Using L-Edit for Q1c grounded PMOS

Area of transistor=230+110+110+220 =670 sq. um

From the above area calculation the Load ,when saturated NMOS, occupies smaller area as well as sharper transition of transfer curve than the Psuedo NMOS Inv. therefore the former is preferred then latter. Using L EDIT the layout is drawn and the functionality is verified.

Ans-3 a. In the CMOS the W=3um and the L=0.8 um for Vinv condition

b. Effect of increasing W keeping L constant for a CMOS inverter :-

If W of load MOS is increased then the high noise margin will decrease (because the VIHmin will increase and VOHmin will be nearly the same as before, so noise margin high =|VOHmin-VIHmin| so noise high margin will decrease), and the noise margin low will increase (because the VILmax will increase while VOLmax is still nearly the same as before, so noise margin low=|VILmax-VOLmax| will increase).

The V-inv voltage of the cmos inverter will increase on increasing the W of PMOS keeping L constant.

c. Effect of increasing l keeping w constant for a cmos inverter :-

If L of load MOS is increased then the high noise margin will increase (because the VIHmin will decrease while the VOHmin is still nearly the same as before, so noise high margin=|VOHmin-VIHmin| will increase) and the noise low margin will decrease (because the VILmax will decrease, while the VOLmax is still nearly the same as before so noise low margin=|VILmax-VOLmax| will decrease).

The V-inv voltage of the CMOS inverter will decrease on increasing the L of PMOS keeping W constant.

d. Using L-Edit for CMOS

Area of transistor= 176+240+220+100=736 sq.um

e. using L EDIT the layout is drawn and the functionality is verified.

Ans-4 The noise margin obtained in the inverters is shown in the table above.

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