E0-284 : Home Work - 1

Due on 3-9-2002 by 5:00pm in the lab

NOTE: In this lab assignment you should use the E284N and E284P MOS transistor models provided to you in the lab. Further you should use 3.3V as power supply voltage in all your simulations for the rest of the course.

(a) For N & PMOS transistor with W=10μm and L=0.8μm, obtain the family of Id-Vg characteristics with Vds fixed at 0.1V and with body voltage as a parameter which varies from Vbs= +0.5V to –3V for NMOS in steps of 0.5V and Vbs= -0.5V to +3V for PMOS in steps of 0.5V. From these Id-Vg characteristics extract and tabulate the threshold voltage for N & PMOS transistors as a function of Vbs. Using this information of threshold voltage dependence on Vbs, extract the body effect factor for both the transistors. How does this value compare with the SPICE parameter value γ in your model file?

(b)Repeat the exercise in (a) by fixing Vds=3.3V instead of 0.1V. (W=10μm and L=0.8μm). Again obtain the values of threshold voltage and body effect factor. Are they different compared to (a) or the same? Do you expect them to be the same? If yes why and if no why not?

(c) For N & PMOS transistors obtain Id-Vds characteristics for Vg=3.3V. What is the Vd value at which the transistor enters the saturation region?

(d) You generate another set of model files (E284N2 and E284P2) by making the following changes:
Increase Vt0 by 10%, Increase Uo by 10%, Decrease Gamma by 10%.
Suppose that E284N/E284P corresponds to 0.8 micron technology from Foundry A and E284N2/E284P2 corresponds to 0.8 micron technology from Foundry B. Then if you are given a choice to pick one of these technologies to prototype your design, which one will you choose. Justify your answer with appropriate set of simulations and reasoning.

NOTE: You are required to demonstrate the simulations in the lab to the lab instructors. Further you are required to submit one page summary of your findings. If you submit more than one page report then you will be penalized for the extra pages that you submit.

Report: E0-284 HW1

Table-1

|Vds| =.1	NMOS	PMOS
Vbs	Vt (v)	Vt (v)
0.5	0.66	-0.20975
0	0.66	-0.20975
-0.5	0.685	-0.2101
-1	0.704	-0.23635
-1.5	0.716	-0.30698
-2	0.723	-0.31183
-2.5	0.728	-0.30951
-3	0.73	-0.32472

Table-2

|Vds| =3.3	PMOS	NMOS
Vbs (v)	Vt (v)	Vt (v)
-0.5	-0.49032	0.24177
0	-0.49032	0.25127
0.5	-0.50445	0.27147
1	-0.51451	0.29675
1.5	-0.52111	0.30462
2	-0.5252	0.30812
2.5	-0.52759	0.31911
3	-0.52909	0.3211

Ans.1 The table-1 above shows the variation of threshold voltage with Vbs for Vds=.1v in an NMOS & PMOS Transistor resp. The avg. value of Gamma obtained from these readings are 0.10231 for NMOS & 0.0567 for PMOS.
This value differ for that given in the model file of Level-3. The reason is "short channel effect "since L=0.8um in which the secondary effects come into picture & the simple quadratic equation no longer holds good. This is because of the short channel effect where as model parameters are defined for long channel.

Ans.2 The table-2 shows Vt vsVbs. Here Vt decrease due to channel length effect (DIBL) with increasing Vds. Gamma in this case is coming out to be 0.0964 and 0.112 for NMOS and PMOS respectively which is different from prev. values ,the reason being we are calculating gamma using level 1 equation, which ignores this dependence Vt on Vds.

Ans.3 NMOS Pinch-off Voltage is coming out to be 1.3v and for PMOS it's –1.2v which is less than the value obtained by (Vds=Vgs–Vt),because of velocity saturation.(short channel effect)(i.e. mobility in decreases due to increasing elec. field)

Ans.4 In foundry2 (changing the values in Model file) we get less current as compared to that obtained in foundry1 from the graph for same voltages therefore from Low Power dissipation point of view foundary2 is better as compared to that in foundry1.As far as speed of inventor is concerned, the decrease in speed is compensated by increasing mobility.

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