E3-238: Home Work 3 (Due 23/10/03)

1. Design a two-stage OP-AMP shown in Fig. 1. Determine W, L for all devices and the value of compensation capacitor (Cc) for the following specifications:
Open loop gain > 2500
Phase Margin > 45^o
Static power dissipation < 330 μW
Slew rate : As high as you can achieve.

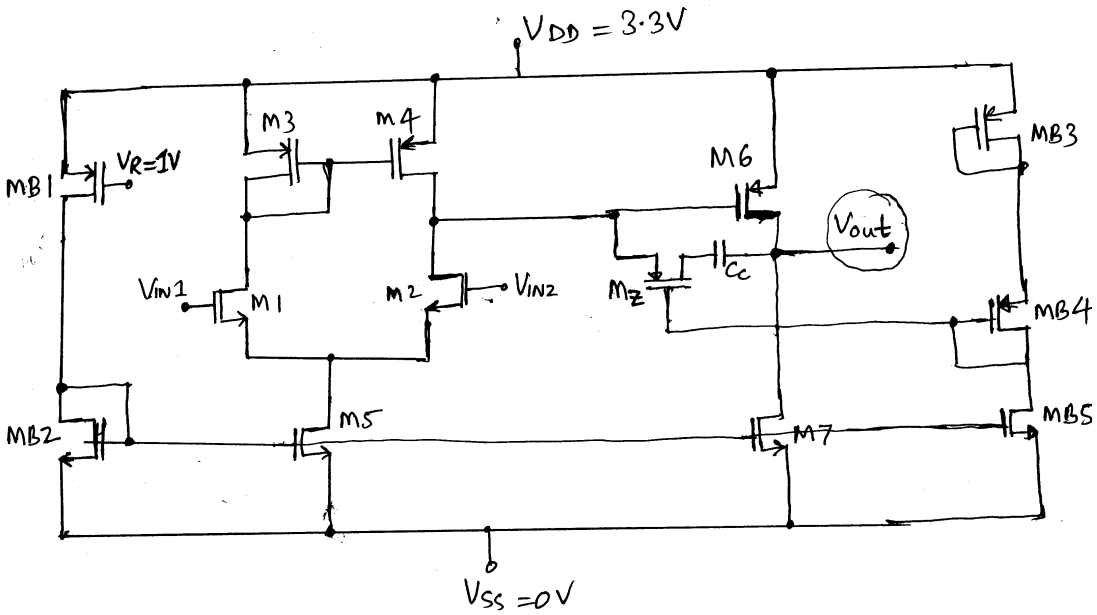
(Design guideline: For the maximum slew rate, try and utilize entire static power budget to bias the first and second stage. I.e. you have a total of 100μA bias current budget. You can allocate 60μA to M5 and 30μA to M7. Use rest of the 10μA for MB1, MB2 branch and MB3, MB4, MB5 branch. Then use appropriate W and L for first and second stage to get required gain. Then use appropriate Cc and nulling transistor for pole splitting and zero cancellation).

Characterize the following parameters through SPICE simulation:

A. Determine the systematic input offset voltage if any. (Note: If you use Vdd=3.3V and Vss=0V, then you should ideally get Vout=1.65V for Vin1=Vin2=1.65V. This is equivalent to putting Vdd=1.65V, Vss=-1.65V and then the ideal case would be Vout=0 for Vin1=Vin2=0V. In order to get the offset with Vdd=3.3V, use Vin1=1.65V and sweep Vin2 around this value to make Vout=0). For all the subsequent questions, bias the OP-AMP using external DC voltage to cancel this offset.
B. Plot open loop differential gain versus frequency (both magnitude and phase plot) using AC simulation. What is the unity gain bandwidth and what is the phase margin through simulation? What is the frequency of the dominant pole?
C. Plot open loop common mode gain and CMRR versus frequency
D. Using pole-zero analysis obtain all the poles and zeros of the OP-AMP for "differential response". Is this consistent with the results obtained in 2?
E. Characterize the step response of the OP-AMP and thereby obtain the slew-rate. Obtain the step response for the following step inputs at Vin2:
    a. 1μV (b)1mV (c)1V
F. Obtain PSRR (as a function of frequency)
G. Connect a variable capacitance load at the output of the OP-AMP. Find the C_L at which the phase margin vanishes to zero.

(Fig. 1 is in the second page)

Fig. 1 2 stage OP AMP WITHOUT BUFFER



M1 – M4 : Diff amp (I amplifying stage)
M5 : provides Iss for Diff Amp.
MB1 and MB2 : Form Current mirror ckt along with M5 to produce Iss
M6 – M7 : II amplifying stage
Mz : Nulling transistor
Cc : Compensation capacitor
MB3–MB5 : Biasing transistors for Mz
VIN1 : Inverting I/p (–)
VIN2 : Non Inverting I/p (+)

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2. Use the two stage OP-AMP designed in **1**. for comparator application. Suppose that the NMOS input transistors have mismatch in their threshold voltage. The transistor M1 has 5% higher VTH0 than nominal and transistor M2 has 5% lower VTH0 than nominal. (Create two more SPICE model files for NMOS transistor CMOSN_SLOW and CMOSN_FAST corresponding to these two values of VTH0. All other

parameters will remain similar to nominal model. Then, in your SPICE input file, M1 and M2 must reference these new model files instead of nominal model file.).

When Vin2=1.65V, the comparator transfer function with respect to Vin1 will not be symmetric about 1.65V due to the transistor mismatch. Estimate the minimum input differential voltage that can be amplified correctly (for both Vin<1.65 case and Vin>1.65V case).

Use input series cancellation and then estimate the minimum input differential voltage that can be amplified correctly (for both Vin<1.65 case and Vin>1.65V case)

Use output series cancellation and then estimate the minimum input differential voltage that can be amplified correctly (for both Vin<1.65 case and Vin>1.65V case)

E3-238: Home Work 3

Submitted by:
Agnish Jain (02172)
Hemant Parate (02195)
Rupesh Bartunia (02035)

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The Design is a two stage OPAMP as per the given problem. In order to meet the power dissipation criteria the currents are also chosen as suggested. The design flow used for the 1st stage and 2nd stage is described below.

1st Stage

The first stage of op-amp is a differential input, single ended output with active current load. The sizes and overdrive voltages have been chosen as follows:

MB1: To support 5µA current with V_g = 1v, the calculated W/L was 3.5/13.5, but as observed in the results the current is half then expected, which is due to mobility degradation (since high V_{sg}) so the W/L were increased to 3.5/27.5 which gives I_d = 5.014µA.

MB2: Since Id = 5µA and since its G and D are shorted which were also connected to gate of other (Current Mirror) transistors, so V_{gs} is chosen as 180mV which yields W/L = 11/3.5

M5: Since I_d = 60µA and Vgs = 180mv the calculated W/L was 132/3.5 (12 times MB2), but the I_d obtained with this W/L was 64.46µA, so W/L was reduced to 123/3.5 (which is later adjusted to 121.9/3.5 to meet offset requirement as explained later) to obtain I_d = 59.23µA.

M1, M2: This are differential pair transistors and I_d from each one is 30µA, one requirement for them is to reduce mismatch which can be done by larger W/L, the V_t is more since they are affected from body effect. Here we require the output at drain of M2 (M1) as 2.2 v in order to drive the 2nd stage so correspondingly W/L were chosen as 42/3.5.

M3, M4: In the current source load transistor also I_d = 30µA and V_{sg} (= V_{ds}) = 1.1v (M3) was chosen so sizes were calculated to be 116/3.5 But from simulation V_{sg} was 1.24V. So they were resized to 123.5/3.5.

The output voltage of this stage is taken at 2.2V to get the final output at 1.65V. After simulation it was found to be 2.077V. The gain for first stage is 184.

Transistor	W/L		I_d (µA)		V_{gs} (V)	g_m(µA/V)
	Calculated	*Simulated*	*Calculated*	*Simulated*	*Simulated*	*Simulated*
MB1	3.5/27.5	3.5/13.5	5	5.014	2.3	7.266
MB2	11/3.5	11/3.5	5	5.014	0.95	45.02
M5	132/3.5	121.9/3.5	60	58.48	0.95	470.4
M1, M2	42/3.5	42/3.5	30	29.24	1.062	222.6
M3, M4	116/3.5	123.5/3.5	30	29.24	1.244	228.7

Table-1

2nd Stage

In order to get A_v > 2500 the second stage needs to have a gain of at least 2500/184 > 15. The current for 2nd stage is set to 30µA. Transistor sizes:

M7: Size of M7 = 66/3.5(6 times MB2), but is sized to 57/3.5 (actually is later adjusted to make output at 1.65v)

M6: The Common Source amplifier is designed to provide I_d = 30µA, sufficient gain and V_o=1.65v. Firstly we simply size it to be same size to that of M6 (since Id is same for both) i.e. 116/3.5

Transistor	W/L		I_d (µA)		V_{gs}(V)	g_m(µA/V)
	Calculated	*Simulated*	*Calculated*	*Simulated*	*Simulated*	*Simulated*
M6	116/3.5	115.5/13.5	30	29.33	1.224	229.5
M7	57/3.5	57/3.5	30	29.33	0.95	252.2

Table – 2

Differential Gain, A_{OL} = 93.71dB (A_{v1}= -184 and A_{v2} = -229)
Phase Margin (PM)= - 47° f_{3db}=34.67KHz, f_u= 72.44MHz
The poles are observed at p_1 = 34.67KHz p_2 = 3.6MHz

Pole Splitting and Zero Cancellation:

As observed the PM was negative, to make it positive we performed pole splitting and Zero Cancellation using C_c and R_z (realized as Mz) as mentioned below:

By formula $C_c=g_{m1}/(2\pi f_u)$ where f_u is the unity gain freq. By simulation g_{m1} was 222.6µA/V. Now we can set f_u at the location of second pole (p_2) (to make the PM of A_{OL} approx 45^0). To give a little more margin f_u was set to 3MHz. C_c was then calculated as 11.8pF. The obtained PM was quite low i.e. 1.57° with f_u=8MHz.
Due to presence of Zero at frequency g_{m6}/C_c, f_u of the opamp and location of the zero occur close together. Since the zero is in the right half S plane, PM is further degraded. So Zero cancellation is done using R_z in series with C_c.

The value of R_z can be approximated to $1/g_{m6}$ (where g_{m6} from simulation was 229.88µA/V) i.e. 4.35k. With R_z=4.35k and C_c = 12pF when the PM obtained was 74.5°, which is > 45°. So we adjusted R_z and C_c as 2.5pF and 4.35k and got PM=51°.

Since R_z is realized with PMOS transistor in triode region in which the channel resistance, $R_z = 1/(\beta(V_{sg}-V_{thp}))$ so setting it to $1/g_{m6}$ (to track the inverse of g_{m6} over PVT variations), we sized Mz as the same dimensions of M6 i.e. $(W/L)_{Mz}$ = 116/3.5.

To bias Mz we also need to use MB3, MB4, MB5 transistors in series, by setting I_d in MB3-5 branch = 5µA, the dimensions were

$(W/L)_{MB3}$ = 4/3.5 $(W/L)_{MB4}$ = 21.4/3.5, $(W/L)_{MB5}$ = 11/3.5.

Using these values the PM obtained was 35.67°. In order to make PM > 45°, C_c and Mz were varied, so finally we got PM as 55.26° at $(W/L)_{Mz}$=85/3.5 (Ron = 2.52k) and C_c = 12pF.

In order to meet output voltage, gain, PM the transistor sizes were frequently changed which resulted into difference in the following ratio

$$\frac{(W/L)3}{(W/L)6} = \frac{(W/L)4}{(W/L)6} = \frac{(W/L)5}{2*(W/L)7}$$

This ratio should be mate in order to minimize the systematic offset, so the transistor sizes were tuned to meet this ratio as close as possible without affecting other parameters. The final sizes of this transistors are thus as shown in the table 1.
Total I_d obtained is 97.75 µA and Static Power Dissipation of 322.26µW.

1. Characterization of parameters SPICE simulation:

(A) Systematic input Offset Voltage Calculation
After tuning the transistors the output observed was 1.415V, which is less than 1.65V. So an external bias of 4.92μV is required at Vin2 to cancel the offset voltage (This value is obtained by using Vin1=1.65V and sweeping Vin2 around this value). The frequency response remains nearly the same as in fig.4.

(B) The open loop differential gain versus frequency (both magnitude and phase plot) is as shown in fig.4.
The open loop gain (at DC) is 93.57 dB, f_u (unity gain bandwidth) obtained is 3.14Mhz; Dominant Pole (p_1) is 63 Hz, and the PM is 180 + (-124.74) = 55.26^o.

(C) The open loop common mode gain and CMRR versus frequency are plotted as shown in fig.5 and fig. 6 respectively. The A_{OLCM}(at DC) is – 816.4m dB and CMRR is 94.57 dB.

(D) The poles and zeroes observed from the open loop frequency response of differential gain are as follows:
P_1 = 63 Hz. Z_1 = 5.36 Mhz. P_2 = 31.62Mhz. Z_2 = 316.2Mhz.
As can be observed the dominant pole is at 63 Hz. And the first Zero is at a frequency greater then f_u.

(E) Step response of the OP-AMP for 1μV (b) 1mV, and (c) 1V are as plotted in fig.7 and fig.8. The PSRR is given in table 3. (Theoretically it should be I_{ss}/Cc =5V/μs). It is observed that as the magnitude of step input falls the Slew Rate as drops.

Voltage	1v	1mV	1μV
SR	5.55 V/μs	23.06 mV/μs	.236μV/μs

Table - 3

(F) The Power supply noise in the OP-AMP can come either from V_{dd} or V_{ss} and it has different characteristics in the two cases. So PSRR for corresponding V^+ and V^- variations on V_{dd} and V_{ss} at DC are 108.57 dB and 104.5dB. They are plotted in fig.9 and fig.10 respectively.

(G) By connecting a variable capacitance load (C_L) (in pF to nF range) at the output, PM for different C_L is noted and the minimum PM obtained by simulation is 5.3^o with C_L = 1nF.

2. Comparator Circuit:

Due to V_t mismatch g_m, I_d G and D voltage of both transistors in differential pairs are not identical and hence gain is different. By fixing the V_{in1} at 1.65V and changing V_{in2} around the 1.65V offset voltage was found to be V_{off} = 77.81212mV(exact). This voltage is required at V_{in2} to restore V_{out} at 1.65 for V_{in1}=V_{in2}= 1.65V.

(A) When Vin1 is varied from 0 to 3.3V, ideally V_{out} should switch to 3.3 when V_{in2} crosses 1.65 V, but due to V_t variations, V_{out} is observed to switch at 1.728V resulting into V_{off} =78mV. The V_o vs. V_{in2} plot is shown in Fig.11. The previous sweep (at +ve input around 1.65V) also what we got is confirmed from here.

(B) Input Series Cancellation: It is used to perform offset voltage cancellation. Here the OPAMP is used with a capacitor C_o = 1pF and 3 switches realized as Pass transistors. V_{in2} varies from 0 - 3.3V, the switching is plotted and shown in Fig 12. It can observed that V_{out} = 1.6985V so V_{off} = 48.5mV which is less than that observed in (a) but could not be removed completely due to charge sharing and discharging of the capacitor due to delay between switching the switches.

(C) Output Series Cancellation: Since A_{OL} > 93dB and the offset is in few mV so the capacitor have to store A_{OL}*V_{off}, hence the output goes into saturation and we cannot get the exact value. During the simulation output saturates and hence the offset cancellation can't be observed in this case.

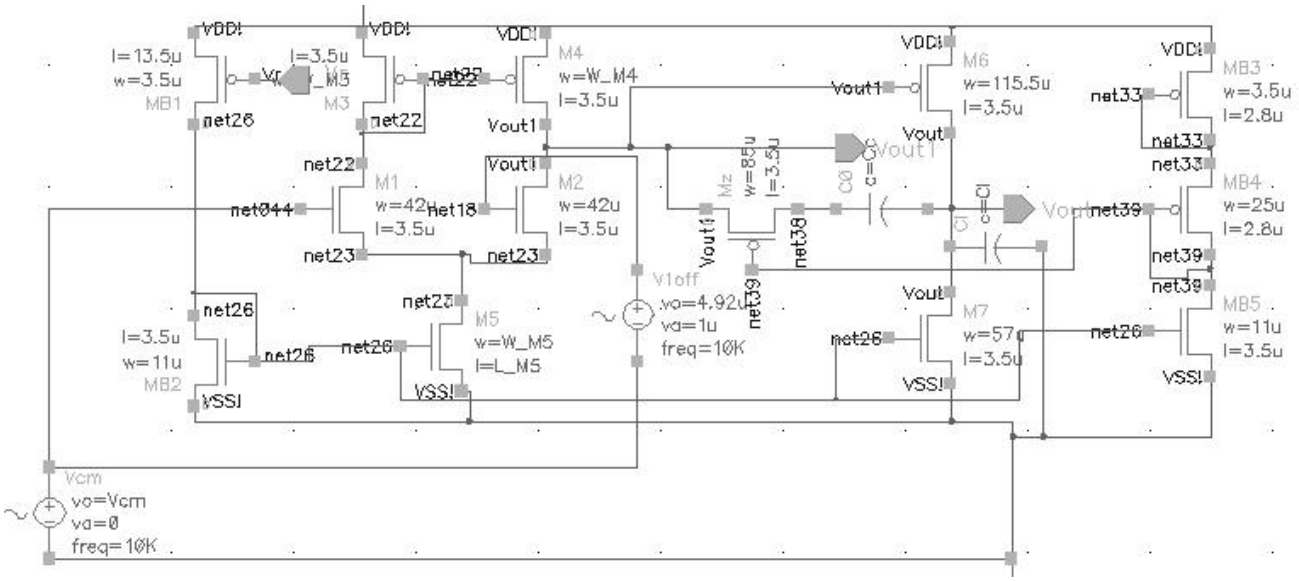

Fig. 1 Circuit Diagram of two stage OPAMP.

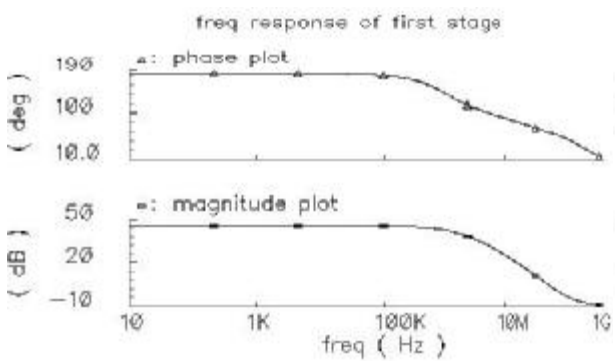

Fig.2 Frequency Response of Differential stage

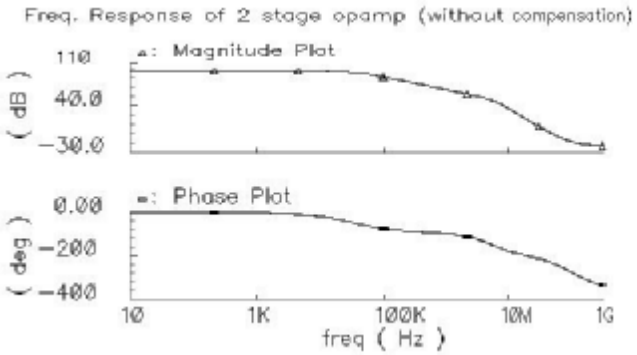

Fig.3 Frequency Response of cascaded two stages

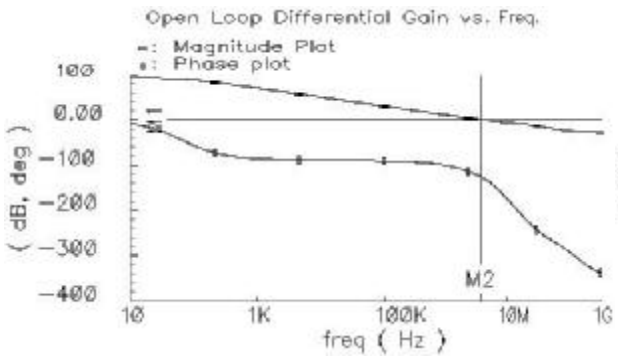

Fig.4 Open Loop Freq. Response with compensation

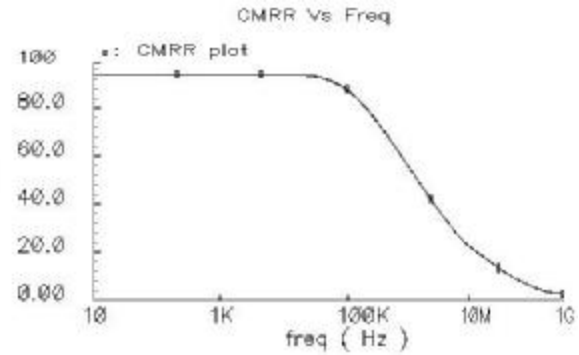

Fig.5 CMRR vs. Freq. plot

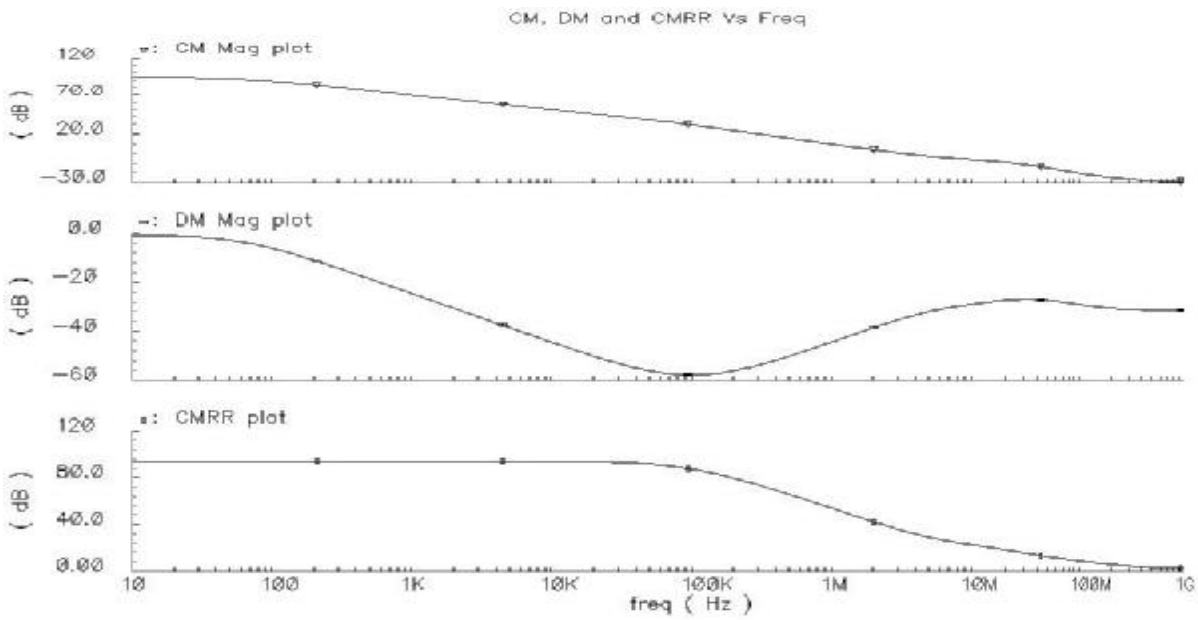

Fig. 6 CM, DM, and CMRR of OPAMP

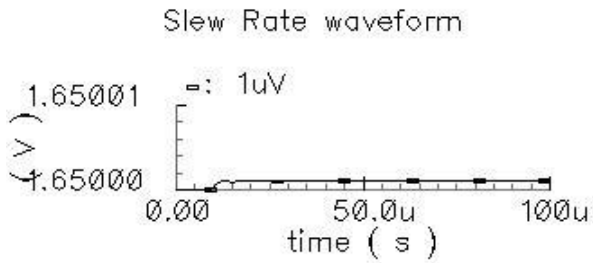

Fig.7 Slew Rate Calculations for 1µV input

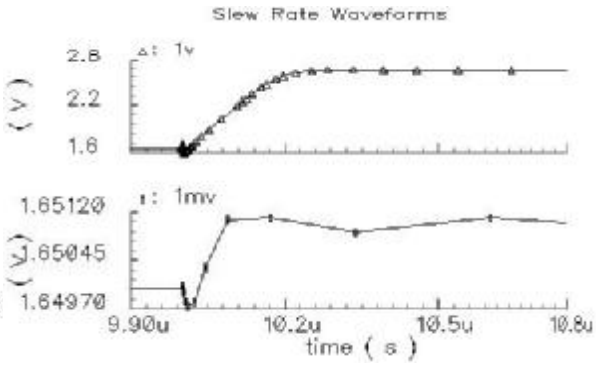

Fig.8 Slew Rate Calculations for 1mV, 1V input

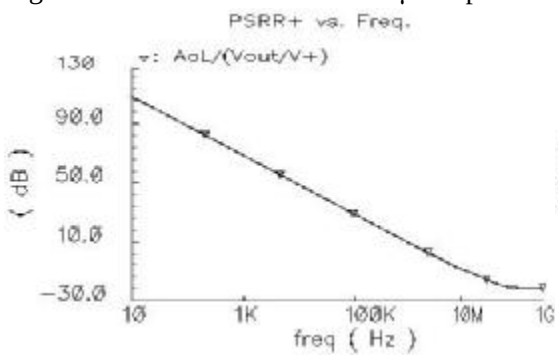

Fig. 9 Positive PSRR vs. Freq. plots

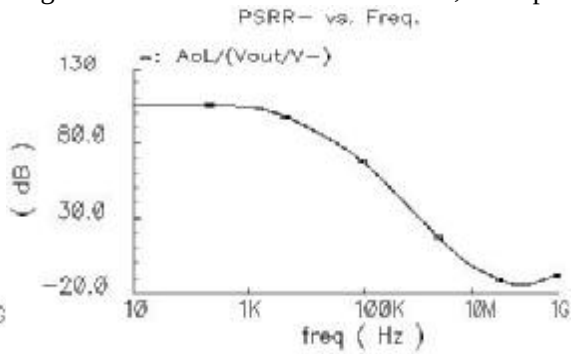

Fig. 10 Negative PSRR vs. Freq. plots.

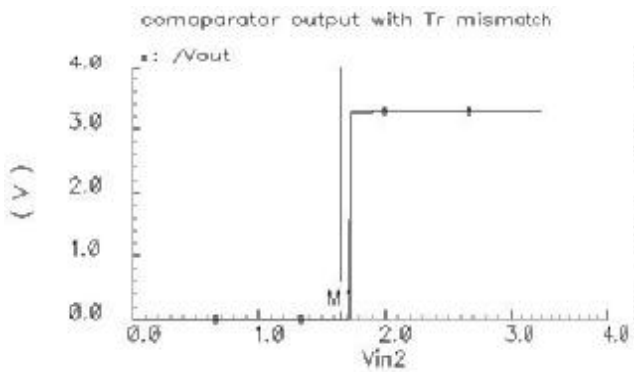

Fig.11 Comparator Output with V_t mismatch

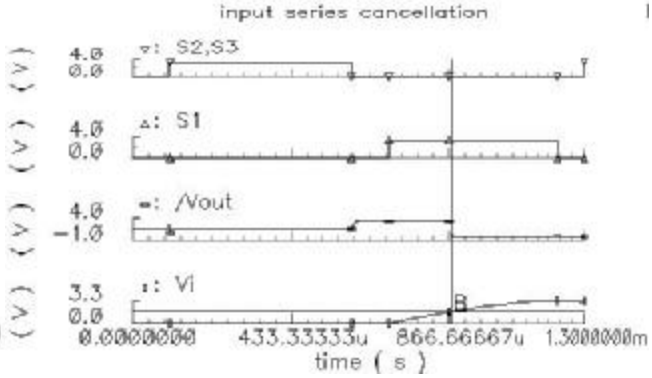

Fig.12 input series cancellation for Comparator