E3-238: Home Work 2 (Due 29/9/03)

1. Consider the amplifier that you designed in HW#1 with constant current source load. Suppose that the amplifier is driven by a source whose resistance is non-zero. What is the upper limit on this resistor so that the bandwidth of the amplifier does not fall below $0.5f_{3DB}$, where f_{3DB} is the bandwidth that you had obtained earlier. Plot the corresponding frequency response.
2. For the source resistance obtained in (1), design a cascode configuration, which restores the bandwidth to f_{3DB} with identical low frequency gain. Plot the frequency response of the amplifier
3. Consider a source follower, which is driven from a source with a resistance obtained in (1). The amplifier drives a 50 ohm resistor at its output. Obtain the frequency response. Further, using SPICE simulation, obtain the input and out put impedance of the amplifier as a function of frequency. Plot both the magnitude and the phase plot. (*For output impedance, short the input voltage source*)
4. Design a Cascode current mirror and Wilson current mirror to provide an output constant current of 10µA. For the reference current, use a constant current source element of 5µA. The current mirror should be able to support maximum output voltage swing. Characterize the output current of the mirror as a function of output voltage. Obtain the output impedance of the current mirror as a function of frequency. *(*To find output impedance, open circuit the reference current source)*
5. For the same specification given above, design a regulated cascode current mirror. The design should also include the mirroring circuit along with the negative feedback circuit. Characterize the output current of the mirror as a function of output voltage. Obtain the output impedance of the current mirror as a function of frequency. *(*To find output impedance, open circuit the reference current source)*
6. One of the issues in current mirrors is matching of reference and mirror transistor. Suppose that the reference and mirror NMOS transistors have threshold voltage mismatch, which is random in nature with a Gaussian distribution. Both the devices have *nominal* VTH0 given in model file. But when a large number (millions) of such mirrors are fabricated, the VTH0 values of these two transistors vary randomly about the nominal value. The relative variation (*rel_variation*) is 10% of nominal value, which occurs at *sigma=3*. (i.e. 3σ variation is 0.1VTH0_nominal). Using Monte Carlo simulation, obtain the distribution of the output current around the nominal value of 10µA, for both the current mirrors in (4). Use 20 and 200 iterations for Monte Carlo analysis and report the impact of number of iterations on the output current distribution.

   (Note: You have to go through the Parametric Analysis chapter in T-SPICE Pro Tutorial and also .param command syntax in T-SPICE User Guide, in order to do this simulation.

   If you are using Cadence Spectre, then go through similar sections in the Cadence manual.)

** To find output impedance of a circuit, short the input voltage source and open the input current source*

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Q1. The amplifier designed in home work1 with constant current source load has f_{3DB} = 1.57Mhz. (It was indicated to be 118.1 KHz. in the report, which was very low so it was redesigned). Now for $0.5f_{3DB}$= 785khz. The maximum value of R_{src} = **343k.** The circuit parameters are as given in table:

Transistor	W/L	Vgate	Vds	Id
Load (PMOS)	73/3.5	2.18	-2.991	6.85µA
Driver (NMOS)	10/3.5	1.005	308.6m	6.85µA

Table-1

The freq. Response for the above circuit is plotted in the Fig.1 (where M1 marker specifies the f_{3DB}).

Q2. With R_{src} = 343k the cascode amplifier is designed (keeping other transistor parameters identical as in Q1) as follows:

Transistor	W/L	Vgate	Vds	Id
Load (PMOS)	73/3.5	2.18	-2.957	6.86µA
Cascode	3.5/2.8	3.1	37.22m	6.86µA
Common Src.	10/3.5	1.005	306.2m	6.86µA

Table-2

The gate bias for the cascode is quite high i.e. 3.1 v, which is required for restoring the BW. The width of CG transistor was also sweeped but since the capacitance increases with area so it cannot be made large.

Q3. For the source follower with R_L = 50Ω the freq. response, input and output impedance w.r.to freq. is plotted in fig. 3 (a), 3 (b) and 3 (c) respectively. The Z_o value (at low freq.) = 160Ω. The inductive behavior of Z_o can be observed at higher freq.

C_{gd} = 281.8fF, C_{gs} = 3.11pF and g_{m1} = 4.417m.

So $1/g_m$ = 159.9Ω, Pole: $1/R_sC_{gs}$ = 0.937Mhz and Zero: g_{m1}/C_{gs1} = 1.42Ghz which are also observable.

Q4 & Q5. For designing the current mirrors three circuit configurations are simulated. The current obtained in these cases is as shown in the table-3. The Io vs. Vo and Zo vs. freq. plot are shown in fig. 4.1, 4.2, 4.3 and fig5.

Parameters	Cascode CM	Mod. Cascode CM	Wilson CM	Regulated Cascode
L	3.5u	3.5u	3.5u	3.5u
W ratio	56u/28u	56u/28u, W/4 Tr=7u	56u/28u	56u/28u
Io(µA)	10.36u	8.91u	10.36u	10.36u
V_{omin}	942.7m	334.4m	1.008	212.6m

Table-3

In cascode CM the V_{omin}= 2ΔV+Vt = 942.7m whereas for mod. cascode it is reduced to 2ΔV = 334.4m but the I_o value is dropped in this case. I_o for all the configurations is not exactly 10µA, the reasons common to all mirrors include the Channel Width Effect which was observed from the simulation results since by increasing proportional W ratios the current reached value closer to 10µA. V_{omin} is minimum in regulated cascode CM.

Q6. The distribution of no. of iterations vs. Io for the modified cascode and modified wilson current mirror are plotted in fig. 6.1 and 6.2 resp. from the fig. can be inferred that as the no. of iterations increases the center value of I_o is achieved more no. of times. Also the I_{omax} and I_{omin} are also tabulated in Table – 4.

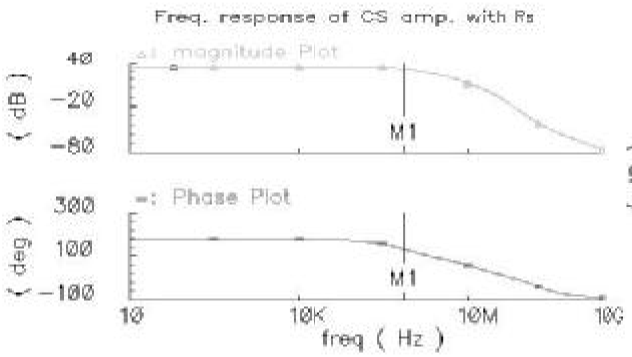


Fig.1. Freq. Response of the CS amp. With R_{src}.

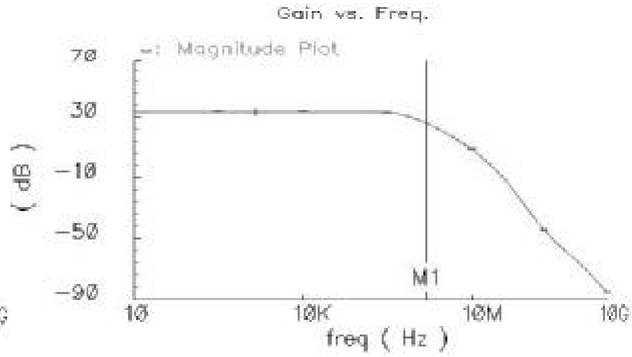


Fig. 2. Freq. Resp. of cascode amp. With R_{src}

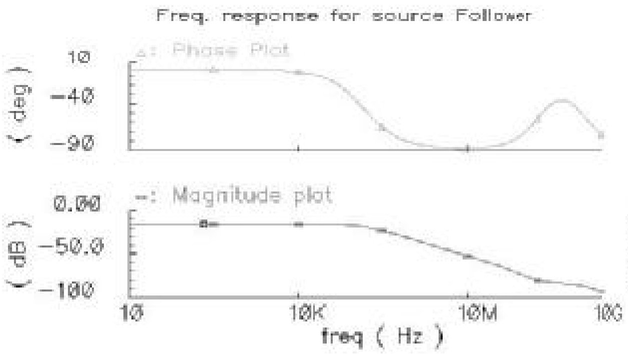
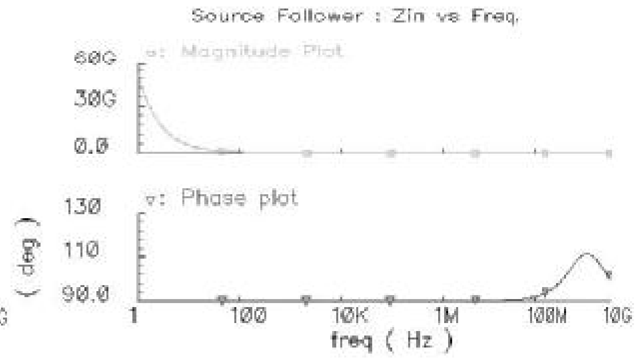


Fig.3 Source follower, (a) Freq. Response.



(b) Input impedance vs. Freq.

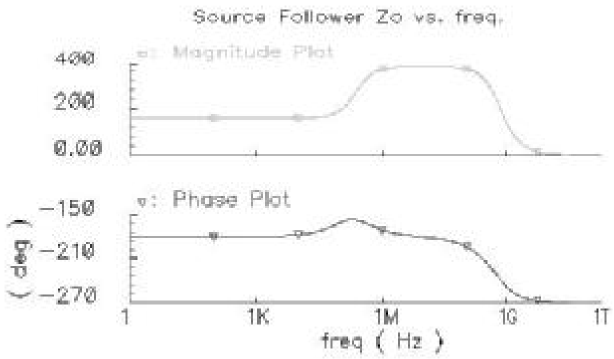


Fig.3 (c) Output impedance vs. Freq.(Mag. and Phase)

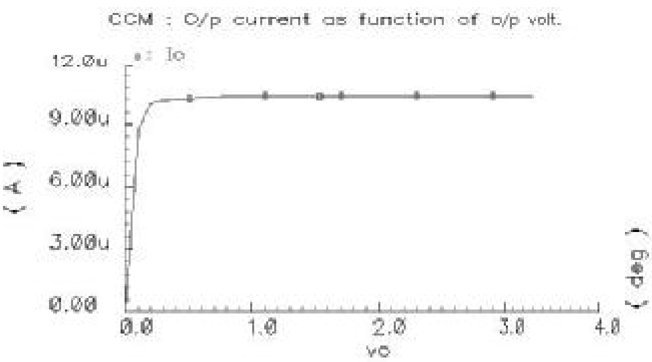
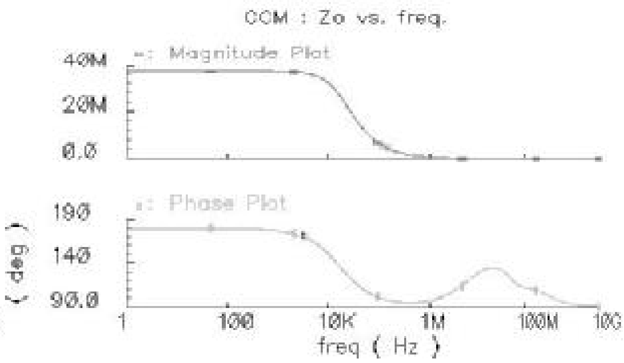


Fig. 4.1 Cascode Current Mirror (a) Io vs. Vo plot,



(b) Output impedance vs. Freq.

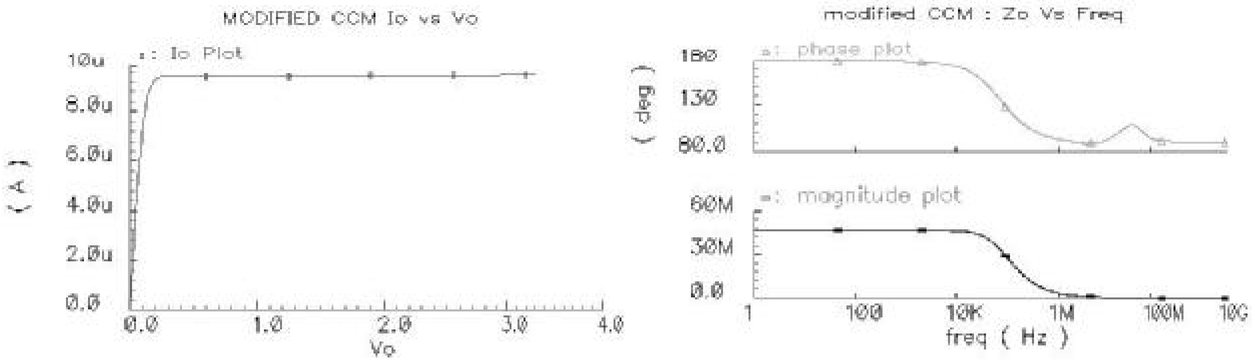


Fig.4.2 Modified Cascode Current Mirror (a) Io vs. Vo plot, (b) Output impedance vs. Freq.

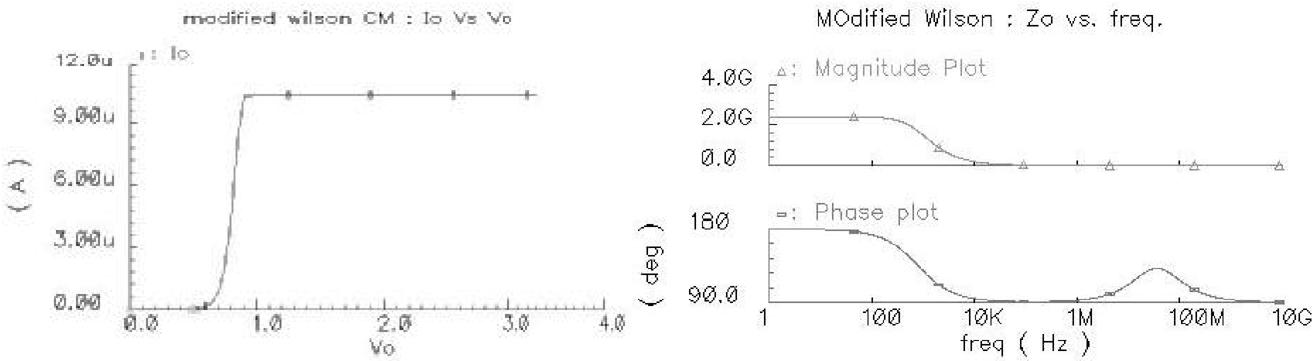


Fig. 4.3 Modified Wilson Current Mirror (a) Io vs. Vo plot, (b) Output impedance vs. Freq.

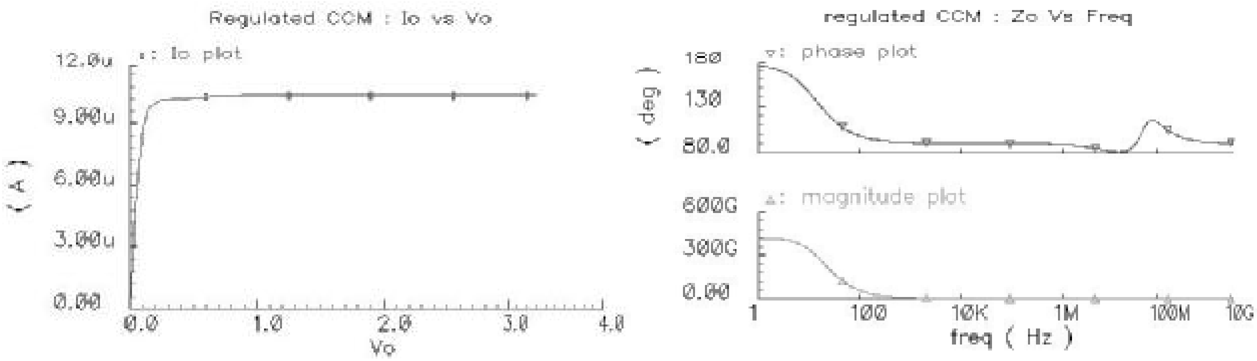


Fig. 5 Regulated Cascode Current Mirror (a) Io vs. Vo plot, (b) Output impedance vs. Freq.

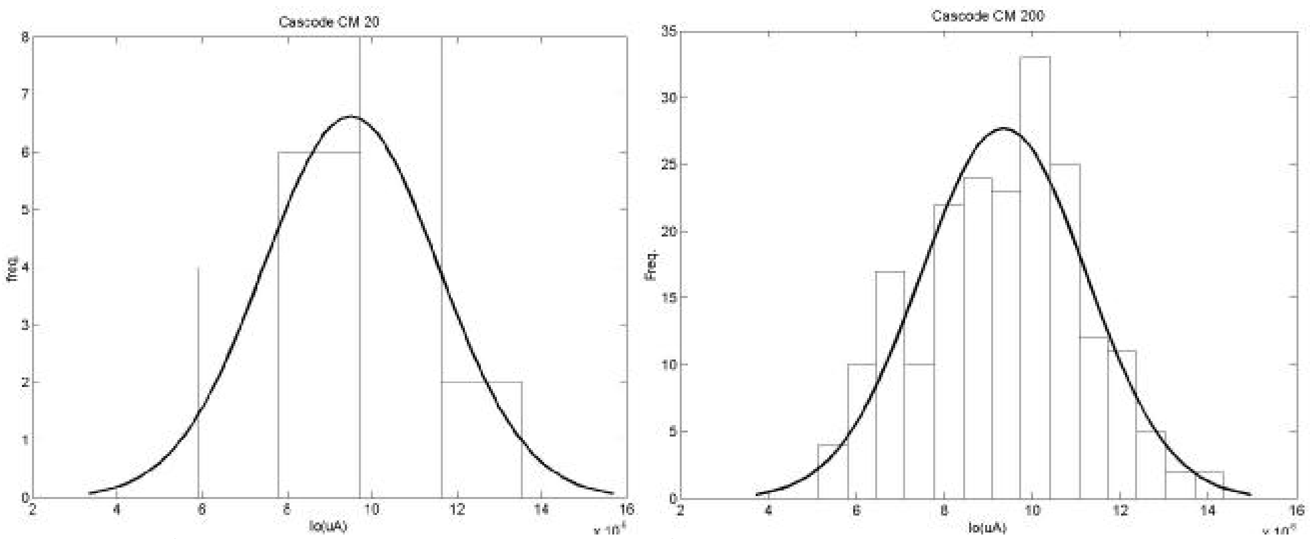


Fig. 6.1Modified Cascode CM monte carlo Analysis for (a) 20 (b) 200 iterations respectively.

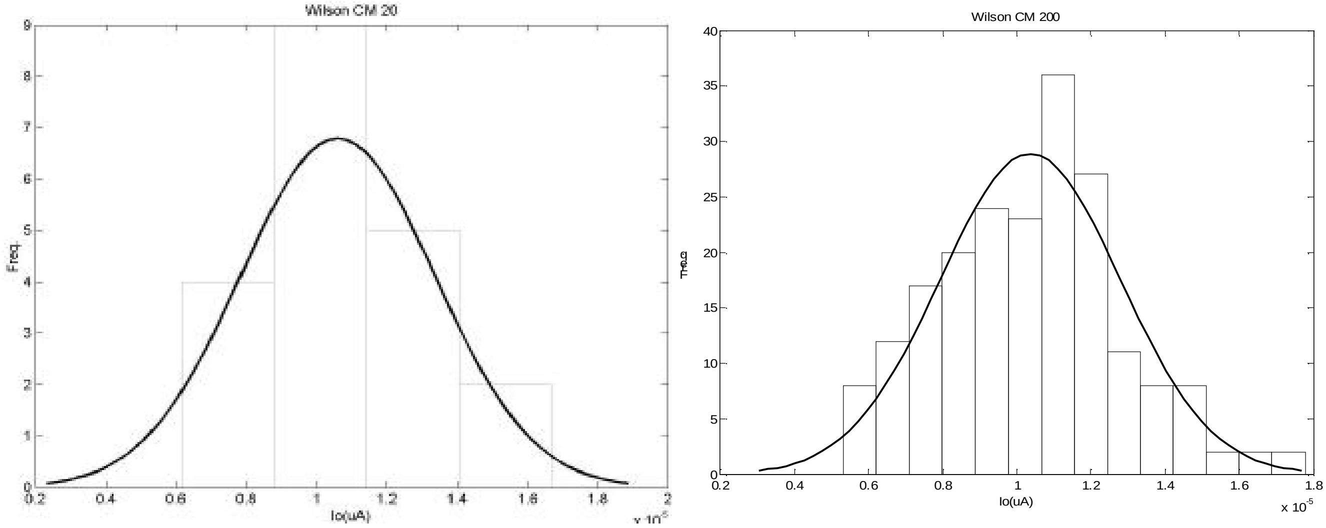


Fig. 6.2 Modified Wilson Current Mirror Monte Carlo Analysis for (a) 20, (b) 200 iterations respectively.

Current	Modified Cascode CM (Iterations)		Modified Wilson CM (Iterations)	
	20	200	20	200
Io Max. (µA)	14.51	14.45	17.77	17.88
Io Min (µA)	5.85	5.15	6.21	5.30

Table-4