E3-238: Home Work 1 (Due 5/9/03)

For this home work and all the subsequent home work assignments, you will be using the AMI 0.7 μm technology offered through Europractice/MOSIS.
The typical N and P transistor models are enclosed. (Note that there are two flavours of PMOS transistors in this technology: high Vt (-1.00V) which can go down to 0.7μm channel length and low Vt (-0.75V) which can go down to 1.2μm channel length). Choose the power supply voltage as 3.3V.

Design a common source amplifier with a **low frequency** gain of 50 for the following 4 different configurations. Indicate the required DC biasing conditions and the transistor sizes for each of the configurations:

1. Resistance load
2. Diode connected NMOS load
3. Current source load (PMOS)
4. Current source load with source degeneration

Note: Low frequency gain implies, the capacitance can be neglected in gain calculation

Analysis to be performed using SPICE (for all the configurations):

1. Using DC analysis (.DC or .OP) verify whether you get required output bias current and voltage for your input DC biasing condition. Generate a table indicating the SPICE results vs. your expected results.
2. Using AC small signal analysis (.AC) obtain the gain (both magnitude and phase) vs frequency plot. What is the unity gain bandwidth? Submit the plots.
3. Using Pole-Zero analysis (.PZ) obtain poles and zeros of transfer function. Can you approximate it as a single pole transfer function? If so, how does the value of dominant pole compare with the 3DB frequency value from the plots in part 2.
4. Estimate the non-linearity using the harmonic analysis. This can be done with transient analysis (.TRAN) followed by the Fourier analysis (.FOUR). Define the input to be a sine wave with frequency 1MHz. Perform the analysis for 4 different *peak to peak* input amplitude: 1mV, 5mV, 10mV, 50mV. (The Amplitude that you specify in the SPICE input deck will be half of peak to peak amplitude). Note that the transient analysis should be performed for at least one cycle, i.e. in this case you can perform the analysis for 1μs. Further the maximum step size should be less than 0.01 times the period of the input, i.e. in this case specify the step size (TSTEP) and maximum step size (TMAX) to be 10ns. Compare the 4 different configurations in terms of the harmonic distortion. Submit a table comparing the harmonic distortion for the 4 different input amplitudes. Also submit the plot showing output waveform for an input peak to peak amplitude of 50mV.

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**********************************************************************************
* C07MA & C07MD N TYPICAL MODEL
*
* RELEASE 3.2 (FOR MORE INFORMATION, READ THE MODELS.INFO FILE)
* 1, Nature NDMOS model added,
*    Subcircuit NNDMOS4 defining the NNDMOS model
* 2, polydiode model added, model name is DPL.
*
* Update of leakage models by ZN, 29/09/99
**********************************************************************************
*
.MODEL NMOS NMOS LEVEL   = 49
+TNOM    = 27          TOX     = 1.75E-8       XJ      = 2.5E-7
+NCH     = 1.7E17      NSUB    = 4E16          VTH0    = 0.76
+K1      = 0.8219166   K2      = -8.54312E-3   K3      = 11.1089581
+K3B     = -1.9786631  W0      = 1E-6          NLX     = 3.751355E-8
+DVT0W   = 0           DVT1W   = 0             DVT2W   = -0.032
+DVT0    = 5.2254747   DVT1    = 0.590721      DVT2    = -0.05
+VBM     = -5          U0      = 635.6142994   UA      = 1.983902E-9
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+UB     = 1E-21         UC     = 4.667652E-11   VSAT    = 9.5E4
+A0     = 0.9331753     AGS    = 0.1339124      B0      = 0
+B1     = 0             KETA   = -2.746786E-5   A1      = 0
+A2     = 1             RDSW   = 1.573286E3     PRWG    = 6.719929E-6
+PRWB   = -1E-3         WR     = 1              WINT    = 6.065442E-8
+LINT   = 2.87042E-8    DWG    = -1.268839E-8   DWB     = 1.654199E-8
+VOFF   = -0.15         NFACTOR = 0.6887273     CIT     = 0
+CDSC   = 0         CDSCD  = 0              CDSCB   = 0
+ETA0   = 0.08          ETAB   = -0.07          DSUB    = 0.56
+PCLM   = 1.0175962     PDIBLC1 = 0.032818      PDIBLC2 = 2.506552E-3
+PDIBLCB = -1E-6        DROUT  = 0.6067512      PSCBE1  = 3.356583E8
+PSCBE2  = 5E-5         PVAG   = 0.0168906      DELTA   = 0.01
+ALPHA0  = 5E-7         BETA0  = 26             RSH     = 65
+MOBMOD  = 1            PRT    = 159.2464225    UTE     = -1.9522848
+KT1    = -0.4126334    KT1L   = 7.244799E-9    KT2     = 2.671323E-3
+UA1    = 8.353648E-11  UB1    = -2.12098E-19   UC1     = -5.6E-11
+AT     = 3.3E4         NQSMOD = 0              WL      = 0
+WLN    = 1             WW     = 0              WWN     = 1
+WWL    = -5.30182E-20  LL     = 0              LLN     = 1
+LW     = 0             LWN    = 1              LWL     = 0
+AF     = 1             KF     = 3E-28          CAPMOD  = 2
+CGDO   = 4E-10         CGSO   = 4E-10          CGBO    = 3.35E-10
+CJ     = 5E-4          PB     = 0.73           MJ      = 0.35
+CJSW   = 2.8E-10       PBSW   = 0.8            MJSW    = 0.21
* leakage
*+DIOLEV  = 2               JS     = 1.3E-07   JSW = 7E-14
* leakage temperature
*+LIS=3                              XTI = 2                         N = 1
* Area computation, then junc cap and junc leakage computation
*+ALEV = 3                  DCAPLEV = 0
* Access resistance equations
*+ RLEV = 4
* channel charge partition
+XPART   = 0
* Elmore constant
+ELM    = 5
* HIGH  VT , MINIMUM CHANNEL LENGTH IS 0.7  micron
.MODEL PMOS PMOSHVT LEVEL   = 49
+TNOM   = 27            TOX    = 1.75E-8        XJ      = 3E-7
+NCH    = 1.7E17        NSUB   = 4E16           VTH0    = -1.00
+K1     = 0.563991      K2     = 0              K3      = 16.3317811
+K3B    = -2.9202228    W0     = 1.23464E-6     NLX     = 9.69545E-8
+DVT0W  = 0             DVT1W  = 0              DVT2W   = -0.032
+DVT0   = 3.5648008     DVT1   = 0.3898843      DVT2    = -0.0284121
+VBM    = -10           U0     = 235.7724356    UA      = 2.964616E-9
+UB     = 1.419129E-18  UC     = -7.00385E-11   VSAT    = 1.1E5
+A0     = 0.4590784     AGS    = 0              B0      = 0
+B1     = 1.407805E-9   KETA   = -0.047         A1      = 0
+A2     = 1             RDSW   = 3E3            PRWG    = 2.024978E-3
+RSH    = 94            PRWB   = 7.428781E-5    WR      = 1
+WINT   = 10.669321E-8  LINT   = 1.9089522E-8   DWG     = -1.478082E-8
+DWB    = 1.561823E-8   ALPHA0 = 0              BETA0   = 30
+VOFF   = -0.126            NFACTOR = 0.7324039     CIT     = 0
+CDSC   = 0             CDSCD  = 7.69E-4        CDSCB   = 8.2E-4
+ETA0   = 9.999059E-4   ETAB   = -1.999936E-4   DSUB    = 0.998946
+PCLM   = 2.6025265     PDIBLC1 = 1             PDIBLC2 = 2.853174E-4
+PDIBLCB = 0            DROUT  = 0.3837047      PSCBE1  = 4.249266E8
+PSCBE2  = 5E-5         PVAG   = 3.8222424      DELTA   = 0.01
+MOBMOD  = 1            PRT    = 216.4347715    UTE     = -1.2989809
+KT1    = -0.4521998
+KT1L   = -2.091783E-8  KT2    = -0.040013
+UA1    = 3.100822E-9   UB1    = -1E-17         UC1     = -8.35439E-11
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+AT      = 3.289E4       NQSMOD  = 0           WL      = 0
+WLN     = 1             WW      = 0           WWN     = 1
+WWL     = -2.33876E-20  LL      = 0           LLN     = 1
+LW      = 0             LWN     = 1           LWL     = 0
+CAPMOD  = 2             CGDO    = 1.0E-10     CGSO    = 1.0E-10
+CGBO    = 3.35E-10      CJ      = 6.0E-4      PB      = 0.9
+MJ      = 0.51          CJSW    = 3.6E-10     MJSW    = 0.35
+AF      = 1             KF      = 5.0E-30
* leakage
*+DIOLEV  = 2             JS      = 1.4E-7    JSW = 9E-14
*+LIS     = 3             XTI = 0.5             N = 1
* other switch
*+XPART   = 0          ALEV    = 3         RLEV    = 4
*+DCAPLEV = 0          ELM     = 5
*
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*******************************************************************************
* LOW VT , MINIMUM CHANNEL LENGTH IS 1.2 micron
* C07MA & C07MD P TYPICAL MODELS
* RELEASE 3.1 (FOR MORE INFORMATION, READ THE MODELS.INFO FILE)
*
* Revision 04
* Update of leakage model, ZN, 29/09/99
*******************************************************************************
*
*
.MODEL PMOS PMOSLVT LEVEL   = 49
+TNOM    = 27          TOX     = 1.75E-8       XJ      = 3E-7
+NCH     = 1.7E17      NSUB    = 4E16          VTH0    = -0.75
+K1      = 0.5763327   K2      = -7.618274E-5  K3      = 12.5198711
+K3B     = -2.0178793  W0      = 1E-6          NLX     = 2.8637E-7
+DVT0W   = 0           DVT1W   = 0             DVT2W   = -0.032
+DVT0    = 1.2931187   DVT1    = 0.2232876     DVT2    = -0.05
+VBM     = -10         U0      = 240.0573045   UA      = 3.136845E-9
+UB      = 8.554621E-19  UC    = -8.15437E-11  VSAT    = 1.1E5
+A0      = 0.4590784   AGS     = 0             B0      = 0
+B1      = 1.407805E-9 KETA    = -0.047        A1      = 0
+A2      = 1           RDSW    = 3.175369E3    PRWG    = -1E-3
+PRWB    = 3.030043E-5 WR      = 1             WINT    = 1.231493E-7
+LINT    = 2.1605E-9   DWG     = -2.015732E-8  DWB     = 1.475983E-8
+RSH     = 94          ALPHA0  = 0             BETA0 = 30
+VOFF    = -0.1403129  NFACTOR = 0.7291071     CIT     = 0
+CDSC    = 0       CDSCD   = 0             CDSCB   = 2.2E-4
+ETA0    = 9.999059E-4 ETAB    = -1.999936E-4  DSUB    = 0.998946
+PCLM    = 2.6025265   PDIBLC1 = 1            PDIBLC2 = 2.853174E-4
+PDIBLCB = 0           DROUT   = 0.3837047     PSCBE1  = 4.249266E8
+PSCBE2  = 5E-5        PVAG    = 3.8222424     DELTA   = 0.01
+MOBMOD  = 1           PRT     = 216.4347715   UTE     = -1.2989809
+KT1     = -0.4521998  KT1L    = -2.091783E-8  KT2     = -0.040013
+UA1     = 3.100822E-9 UB1     = -1E-17        UC1     = -8.35439E-11
+AT      = 3.289E4     NQSMOD  = 0             WL      = 0
+WLN     = 1           WW      = 0             WWN     = 1
+WWL     = -3.26045E-20  LL    = 0             LLN     = 1
+LW      = 0           LWN     = 1             LWL     = 0
+CAPMOD  = 2           CGDO    = 1.0E-10       CGSO    = 1.0E-10
+CGBO    = 3.35E-10    CJ      = 6.0E-4        PB      = 0.9
+MJ      = 0.51        CJSW    = 3.6E-10       MJSW    = 0.35
+AF      = 1           KF      = 5E-30
* leakage
*+DIOLEV  = 2              JS      = 1.4E-7    JSW = 9E-14
*+LIS     = 3           XTI = 0.5               N = 1
* other switch
+XPART   = 0
*+ALEV    = 3         RLEV    = 4
*+DCAPLEV = 0
+ELM       = 5
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E3-238: Home Work 1

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Date 8/9/2003

Table 1.

Results		Resistor load	Diode load	Current source	CS with source degeneration
|Av|	**Theoretical**	40	50	50	50
	Simulated	24.1	0.186	3.12	232
	Desired for Av= 50	38.4	9.98	49.48	52.3
Id (Amp)	**Theoretical**	5µ	30u	7µ	5u
	Simulated	5.89µ	175u	7µ	5.411µ
	Desired for Av= 50	2.873 u	125 u	13.92 n	3 u

		Driver	Load	Driver	Load	Driver	Load	Driver
W/L	Expected/Theory	30.1/3.5	2.8/2.8	7000/2.8	75/3.5	1.2/3.5	74.4/3.5	43.4/3.5
	Desired for Av= 50	42/3.5	2.8/2.8	560/2.8	1/3.5	1/3.5	424/3.5	15.4/3.5
Vds (V)	**Theoretical**	1.8	**-1.7**	**1.6**	-1.65	1.65	1.0-2.2	1.63-2.3
	Simulated	1.179	**-3.286**	**13.99m**	-0.16	3.16	-1.801	1.44
	Desired for Av= 50	0.426	-2.966	0.333	-0.154	3.14	-3.081	0.203
Vgs (V)	**Theoretical**	0.86	0.783		-1.12	0.78	-1.1	0.85
	Simulated	0.86	0.783		-1.12	1.56	-1.1	0.845
	Desired for Av= 50	0.783	0.85		-1.12	0.766	-1.1	0.875
Rs(ohm)	Expected/Theory	--					10K	
	Desired for Av= 50	--					4.95k	
Rd(ohm)	**Expected**	360k						
	Desired for Av= 50	1M						

Table 2.

Configuration	Pole frequency (Hz)	Zero frequency (Hz)
Resistive load	3M	40M
Diode connected load	3.4M	12M
Constant current source load	60K	500K
CCS source degeneration	900K	8M

Table 3.

Harmonic Distortion	Resistor load	Diode load	Current source	CS with source degeneration
1mv (p-p)	0	0	0	0
5mv (p-p)	0	0	0	0.14
10mv (p-p)	.004	0	0.026	0.184
50mv (p-p)	.207	0.89	.09	0.179
Bandwidth	9.27M	254.86M	118.1K	1.37M
UGB	--	--	1.926M	71.58M

(Small values in m and μ have been assumed to be 0)

In table 2 the pole and zero frequency have been tabulated from the transfer function(magnitude/phase) plots which is an approximation.

In the simulations performed, since the Id equation that is used in theoretical calculations is of second order while the one used by simulator is of higher order, the current varies and due to which the dc operating point also shifts. Also Since the exact values of parameters like λ, β, γ etc. is not known accurately. These parameters also vary with bias conditions. The Vth and Id in turn depend upon these parameters so the accurate calculations for the dc operating point is difficult to be done theoretically. This is valid for almost all configurations. Specific reasoning that apply to the given problems are as follows

CS Amplifier with Resistive load (Fig.1)
Reasoning: Since $A_v = g_m R_d$ and $g_m = 2I_d/(Vgs-Vth)$ & $R_d=(V_{dd}-V_{out})/I_d$, both oppose each other for same I_d. larger R_d & g_m is desired but R_d is limited by output swing & g_m limited by I_d. So there is maximum beyond which we can't increase A_v. If we increase one of these, other decreases since both are related to I_d. The **UGB** couldn't be found since the transfer response didn't cross 0db.

CS Amplifier with Diode connected load (Fig.2)
Reasoning: In active load (diode connected) common source amplifier the large gain is not possible. We know that current through the load is same as current through driver transistor i.e. $\mathbf{I_{DM1}=I_{DM2}}$ Also the small change in the current requires the large voltage drop across the diode. The output voltage is given by $\mathbf{V_{out}=V_{DD}-V_{dsload}}$ So as the V_{DSload} increases Vout decreases so gain reduces. Now in this case the gain depends on W/L ratio of driver and Load. If we increase the W/L of driver to increase the gain, the current will also increase, responded by increase in V_{DSload}. So by increasing W/L after one value does not reflect much in the gain. The **UGB** couldn't be found since the transfer response didn't cross 0db.

CS Amplifier with current source (PMOS) load (Fig.3)
Reasoning: The current is very low so the bandwidth as well as UGB also decreases. V_{DS} is also high so there is clipping for ac signaling. It is quite sensitive to bias as well as Width variations. Thus the bias point and I_d also varies therefore the gain is sensitive to input swings. Thus there is nonliterary in this circuit. As the BW for this circuit is small soothe transient response at 1Mhz. is not settled as is clear in fig. 3a.

Current source load with source degeneration (Fig.4)
Reasoning: The gain is less sensitive to the bias variations compared to the current source (PMOS) load configurations then too the variation in gain is significant for 10mv change in gate overdrive for driver NMOS.

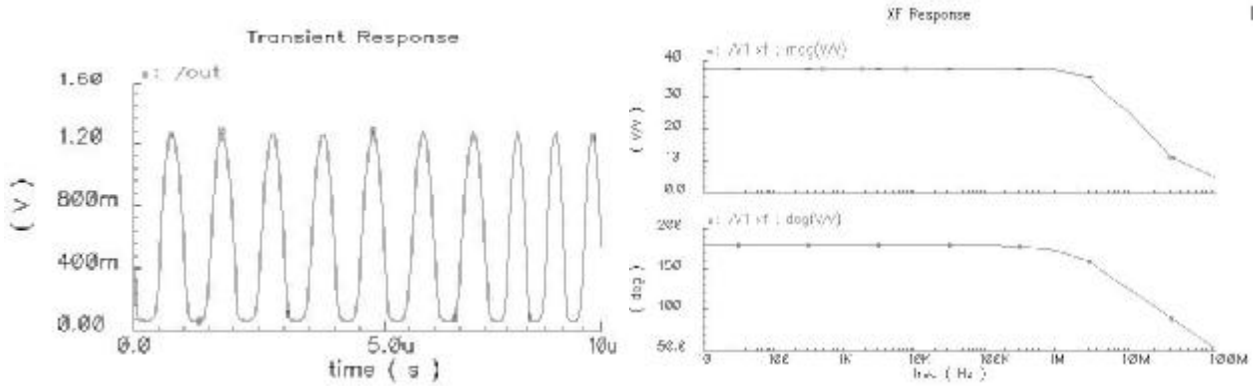

Fig. 1 CS amplifier with Resistive Load (a) Transient response for $V_{in(p-p)}$= 50mv. & freq. = 1Mhz.
(b) Magnitude and Phase plot w.r.to freq.

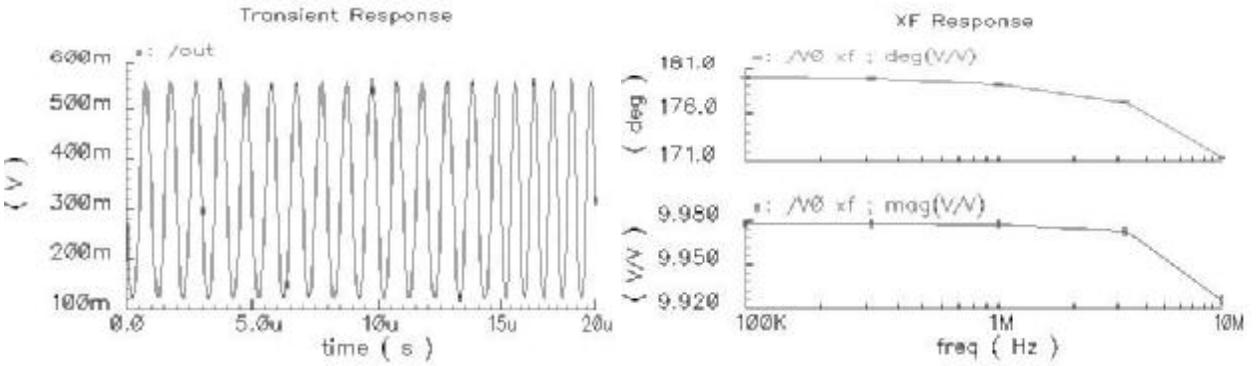

Fig. 2 CS amplifier with Diode as a Load (a) Transient response for $V_{in(p-p)}$= 50mv. & freq. = 1Mhz.
(b) Magnitude and Phase plot w.r.to freq.

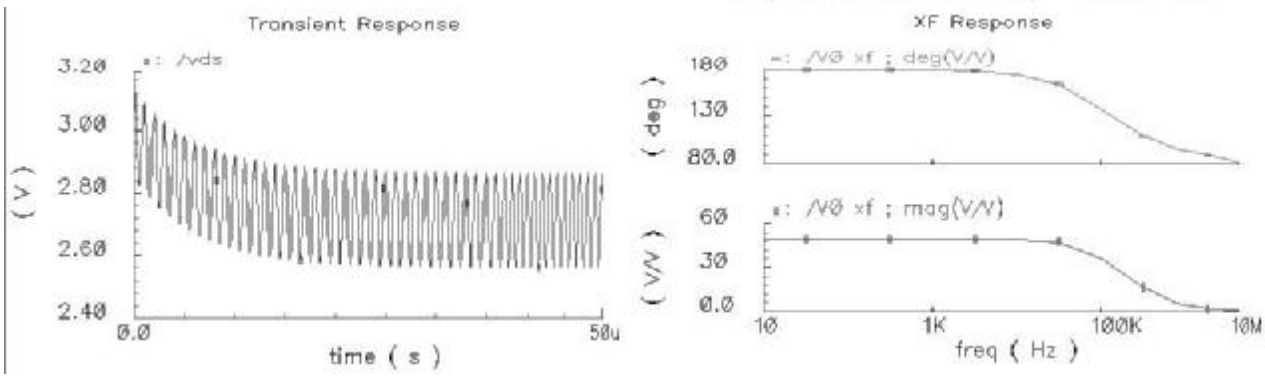

Fig. 3 CS amplifier with Current source load (PMOS) (a) Transient response for $V_{in(p-p)}$= 50mv. & freq. = 1Mhz. (b) Magnitude and Phase plot w.r.to freq.

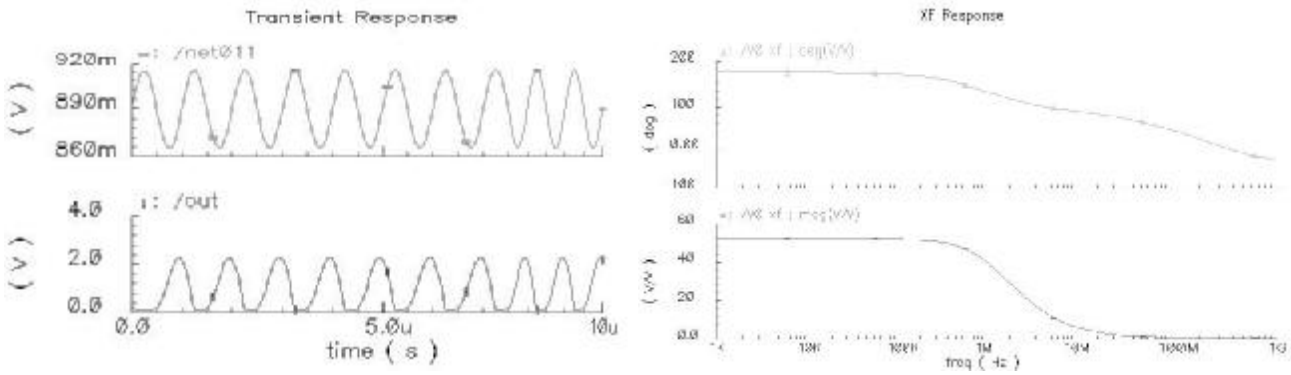

Fig. 4 CS amplifier with Current source load with source degeneration (a) Transient response for $V_{in(p-p)}$= 50mv. & freq. = 1Mhz. (b) Magnitude and Phase plot w.r.to freq.