


Institute for Applied Information Processing and Communications (IAIK) GRAZ UNIVERSITY OF TECHNOLOGY

# Nanotechnologies

## Effects of Shrinking CMOS Technology

Institute for Applied Information Processing and Communications (IAIK) — VLSI Group  
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## Motivation

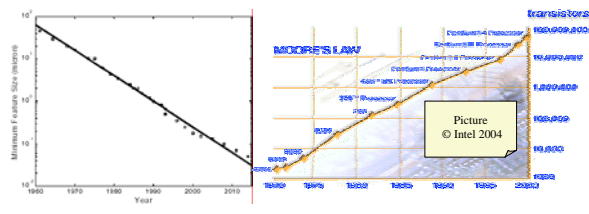
- Deep sub-micron (DSM)
  - 0.25  $\mu\text{m}$ , 0.180  $\mu\text{m}$ , 0.130  $\mu\text{m}$
- Nanotechnologies
  - 90 nm (0.090  $\mu\text{m}$ ), 65 nm, 45nm
- Shrinking of process technologies
  - Higher integration
    - More transistors per area
  - Higher clock speed
  - Lower power consumption

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## Scaling and complexity

- Minimum feature size
- Number of transistors



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## Evolution of technology DRAM

Year	2003	2005	2007	2010
Transistors	153 M	243 M	386 M	773 M
feature size [nm]	100	80	65	45
VDD [V]	1.0	0.9	0.7	0.6
Clock [MHz]	3100	5200	6700	11500
Power [W]	150	170	190	218

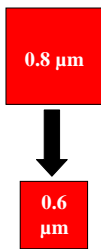
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## Scaling

### Scaling Models

- Full Scaling (ideal)
  - Dimensions and voltage scale
  - Constant electric field
- Fixed voltage Scaling
  - Only dimension scale (historic)
- General scaling
  - Dimensions and voltage scale
    - With different factors



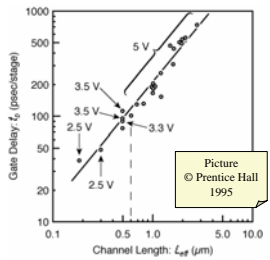
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## Scaling

### Propagation delay

- Technology gets faster
  - Even with lower VDD



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## Scaling

### Supply voltage

- Voltage reduction necessary
  - $VDD_{max} \cong L_{min}[\mu] * 10 [V]$ 
    - $L_{min} = 0.18 \mu m$ :  $VDD_{max} = 1.8 V$
  - For reliability: hot-electron effect, gate oxide
  - Limits gain
  - Lowers noise margins
  - Lowers power:  $P = f * C_L * VDD^2$

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## Scaling

### Threshold voltage

- Threshold voltage
  - Process dependant
  - Is scaled slower than VDD
- Delay
  - Improved
- Leakage
  - Increased: ~ 12 times / 100 mV  $V_T$ 
    - Increases exponentially with lower threshold voltage
  - Higher sub-threshold currents

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## Scaling

### Threshold voltage

The graph plots Relative scale (y-axis, 0.0 to 1.0) against  $V_{dd}/V_t$  (x-axis, 0.0 to 5.0). Four curves are shown:
 

- Delay ( $V_t=0.75$ ): Solid line, starts at 1.0 and drops to ~0.15 at  $V_{dd}/V_t = 2.0$ .
- Delay x Energy ( $V_t=0.75$ ): Dashed line, starts at 1.0 and drops to ~0.3 at  $V_{dd}/V_t = 2.0$ .
- Delay ( $V_t=0.35$ ): Dotted line, starts at 1.0 and drops to ~0.15 at  $V_{dd}/V_t = 2.0$ .
- Delay x Energy ( $V_t=0.35$ ): Dash-dot line, starts at 1.0 and drops to ~0.3 at  $V_{dd}/V_t = 2.0$ .

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## Scaling

### Devices

- Scaled dimensions
  - Minimal gate length scaled down
  - Gate oxide thickness scaled down
- Current density remains nearly constant
  - $I_{d,sat} = 900 [\mu A / \mu m]$
- Capacitances
  - Smaller gate capacitance
  - Relatively larger diffusion capacitance
- Performance
  - Will improve slower
    - to prevent leakage current

Picture © Intel Corp.

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## Scaling

### Threats

- Disadvantages of Nanotechnologies
  - Variability
    - Variation of process parameters
  - Leakage
    - Static power consumption
  - Interconnect
    - Delays signals
    - Consumes power

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## Leakage

- Static power consumption
  - Sub-threshold currents
    - Exponential growth of currents
      - By lowered threshold voltages
      - By increased temperature
  - Gate oxide leakage
    - Tunneling effects
- Depends on circuit area
  - Memories consume much power

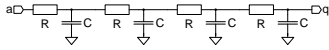
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## Interconnect

- Chip area increases
  - Number of wires increases
  - Average wire length increases
- Electrical length increases
  - Transmission lines
  - Increasing faster than physical length




**Interconnect increases Delay and Power consumption!**

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## Interconnect Parasitics

- Wires are not ideal
  - Capacitance
  - Resistance
  - Inductivity
- Performance
  - Degraded
- Power
  - Wires consume power
- Reliability
  - Electro migration
  - Signal integrity
  - Inductive supply noise

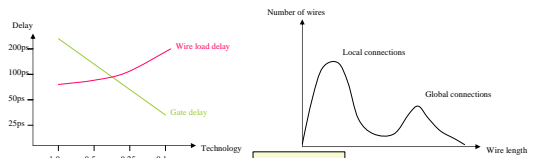


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## Interconnect Parasitics

- Interconnect delay
  - Supercedes gate delay



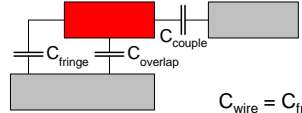
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## Interconnect Parasitics: capacitance

- Overlap capacitance
- Fringing capacitance
- Coupling capacitance



$$C_{\text{wire}} = C_{\text{fringe}} + C_{\text{overlap}} + C_{\text{couple}}$$

$$C_{\text{plate}} = C_{\text{OX}} * W * L$$

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## Interconnect Capacitance Typical Values

- 0.25  $\mu\text{m}$  overlap capacitance [aF/ $\mu\text{m}^2$ ]

	Sub	Poly	Met1	Met2	Met3	Met4
Sub	113	37	18	13	9	8
Poly		53	16	10	7	6
Met1			35	15	9	7
Met2				39	16	10
Met3					44	16
Met4						39

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## Interconnect Capacitance Crosstalk

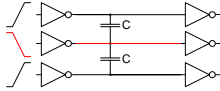
- Less interconnect spacing
  - Capacitance increases
    - Plate capacitor formula:  $C = \epsilon * A / d$
  - Crosstalk
    - Voltage spikes couple to neighboring wires
  - Delay variation: Miller effect

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## Interconnect Capacitance Miller effect

- Neighboring signal
  - Influences signal delay
    - Neighboring signals switch in opposite direction
      - Both capacitor terminals switch in opposite direction
      - Effective voltage doubled -> additional charge needed



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## Interconnect Capacitance Solutions

- Low-k dielectrics:
  - Reduced capacitance

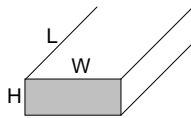
[ $\mu\text{m}$ ]	0.25	0.18	0.13	0.1	0.07	0.05
K	3.3	2.7	2.3	2.0	1.8	1.5

- Copper interconnect
  - Wire thickness can be reduced

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## Interconnect Parasitics: Resistance

- $R = \rho * L / (H * W)$
- Sheet resistance
  - $R_0$
  - $R = R_0 * W / L$
- 0.25  $\mu\text{m}$  sheet resistance
  - N+: 4.9 Ohm / square
  - P+: 3.5 Ohm / square
  - Poly: 4.2 Ohm / square
  - Metal: 0.07 Ohm / square



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## Interconnect Parasitics: Resistance

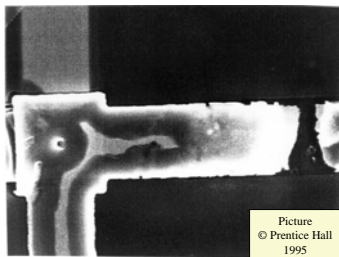
- Influence of wiring increases with smaller processes
- Up to 90% of delay at 0.35  $\mu\text{m}$
- New tools to cope with interconnect
  - „Design for interconnect“ DFI

**Estimate interconnect impact early!**

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## Interconnect Resistance Electro Migration

- Limit average current  $I_{av}$
- Increase wire width
- Peak current
  - Max  $10 I_{av}$



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## Interconnect Resistance Solutions

- Classic metal layers
  - Aluminum ( $2.65e-8 \Omega/\text{m}$ )
- DSM material for Met1, Met2: Tungsten
  - Copper would diffuse into diffusion area
- DSM top metal layers (Met3, Met4, ...)
  - Copper ( $1.67e-8 \Omega/\text{m}$ )
    - 40% resistance reduction
    - VDD and GND distribution
    - Clock signal distribution
    - Lower sensitivity to electro migration

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## Nanotechnology Impact Methodology


- Floor-planning
  - Timing driven
- Synthesis
  - Prediction of interconnect influence
    - Wire-load model
- On-chip buses
  - Segmentation
- Parasitic extraction
  - RC-model for wires instead caps only
  - LRC-models for nanotechnologies
- Testability: Built-in self-test (BIST)
  - At speed testing, "cheap" test equipment

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## Nanotechnology Impact Cost

- Non-recurring cost (NRE)
  - NRE cost increased
    - ~1M US\$ for mask-set and probe card
    - Design iterations are costly
- Test cost
  - Grows two times faster
    - Than manufacturing cost



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## Nanotechnology impact Logic Style

- CMOS
  - Good logic style for DSM
  - Withstands
    - Low supply voltage
    - High threshold voltage
- Domino logic
  - Alternative to CMOS
- Pass-gate logic
  - infeasible
- Transmission gate logic
  - less attractive
- Series transistors
  - Very slow
    - Due to reduced VDD
- Circuit technique
  - Similar to high-speed circuits
    - Logic decomposition
    - Pipelining
  - Synchronous clocks
    - difficult

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## Nanotechnology CMOS Process Example

- 0.13  $\mu\text{m}$  TSMC process (0.08  $\mu\text{m}$   $L_{\text{eff}}$ )
  - 200k – 300k gates /  $\text{mm}^2$
  - VDD = 1.00 V, 1.20 V, or 1.50 V
  - Vt = 0.27 V, 0.35 V, 0.58 V
  - Delay = 14 ps, 19 ps, 25 ps
    - IO voltage: 2.5 V or 3.3 V (optional)
    - Multiple Vt (optional)
    - Operation frequency > 1 GHz
  - 8 layer copper / low-k interconnect
  - MPW run: 2.400.- € /  $\text{mm}^2$  (5\*5 mm = 61.000 €)
    - For comparison: 1  $\text{mm}^2$  @ 0.35  $\mu\text{m}$ : 720 €

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## Conclusion

- DSM process technology
  - Enables multi million transistors circuits
- Requires additional attention during design
  - Impact of interconnect
  - Testability

Scaling will continue at least 10 years!

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