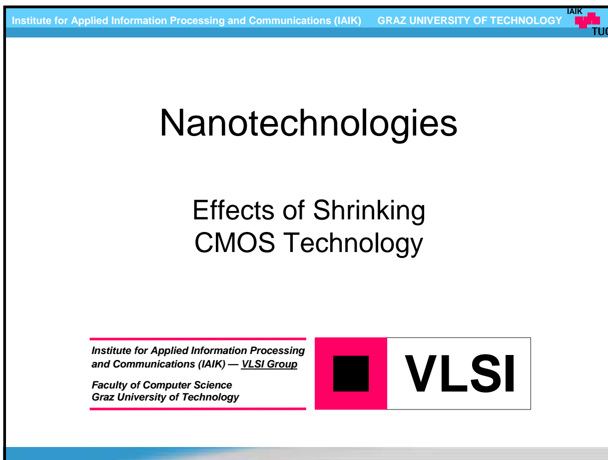
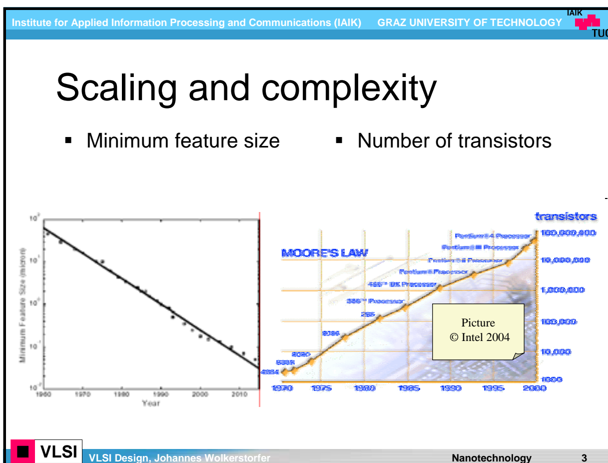


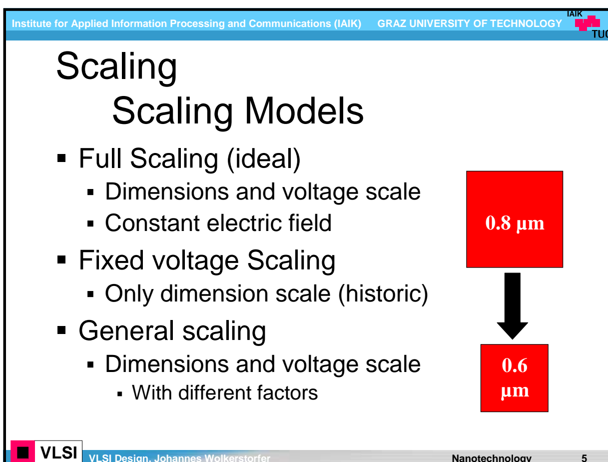
Motivation

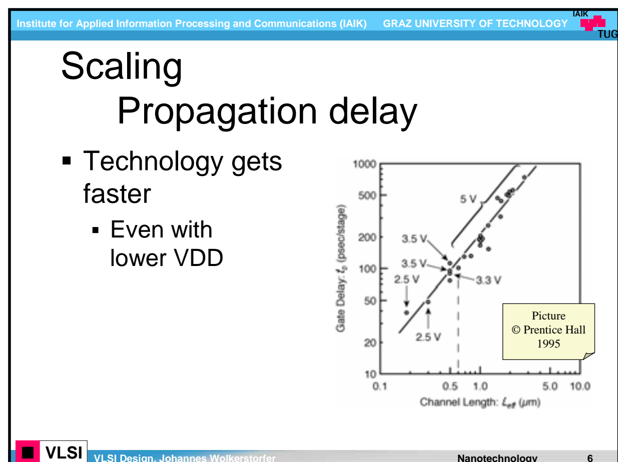
- Deep sub-micron (DSM)
  - 0.25 µm, 0.180 µm, 0.130 µm
- Nanotechnologies
  - 90 nm (0.090 µm), 65 nm, 45nm
- Shrinking of process technologies
  - Higher integration
    - More transistors per area
  - Higher clock speed
  - Lower power consumption



Evolution of technology
DRAM

Year	2003	2005	2007	2010
Transistors	153 M	243 M	386 M	773 M
feature size [nm]	100	80	65	45
VDD [V]	1.0	0.9	0.7	0.6
Clock [MHz]	3100	5200	6700	11500
Power [W]	150	170	190	218





Scaling
Supply voltage

- Voltage reduction necessary
  - $VDD_{max} \cong L_{min}[\mu]*10$ [V]
    - L_{min} = 0.18 µm: VDD_{max} = 1.8 V
  - For reliability: hot-electron effect, gate oxide
  - Limits gain
  - Lowers noise margins
  - Lowers power: $P = f*C_L*VDD^2$

Scaling
Threshold voltage

- Threshold voltage
  - Process dependant
  - Is scaled slower than VDD
- Delay
  - Improved
- Leakage
  - Increased: ~ 12 times / 100 mV V_T
    - Increases exponentially with lower threshold voltage
  - Higher sub-threshold currents

Scaling
Threshold voltage

© Wolfgang Mayerwieser

Scaling
Devices

- Scaled dimensions
  - Minimal gate length scaled down
  - Gate oxide thickness scaled down
- Current density remains nearly constant
  - $I_{d,sat}$ = 900 [µA / µm]
- Capacitances
  - Smaller gate capacitance
  - Relatively larger diffusion capacitance
- Performance
  - Will improve slower
    - to prevent leakage current

Picture © Intel Corp.

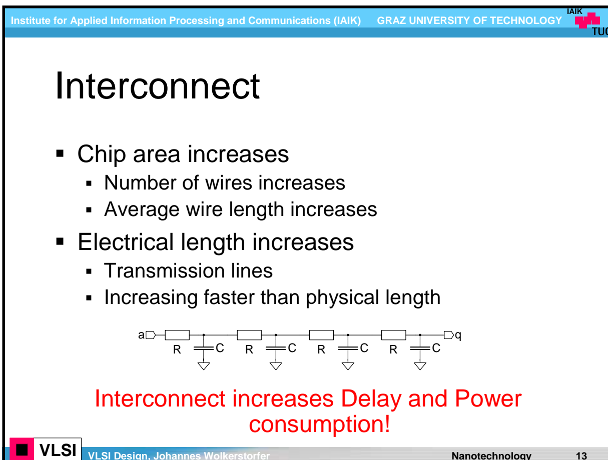
Scaling
Threats

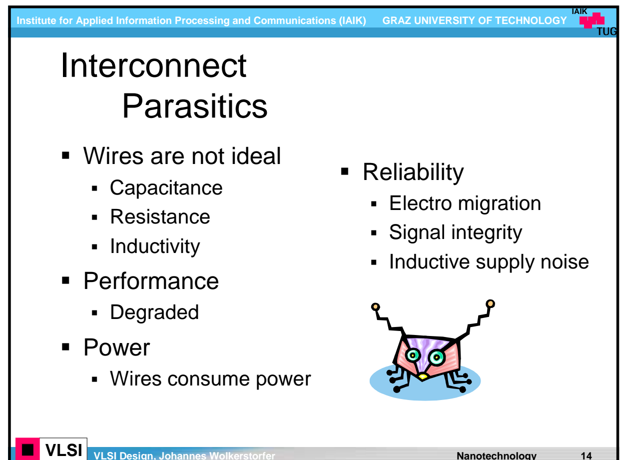
- Disadvantages of Nanotechnologies
  - Variability
    - Variation of process parameters
  - Leakage
    - Static power consumption
  - Interconnect
    - Delays signals
    - Consumes power

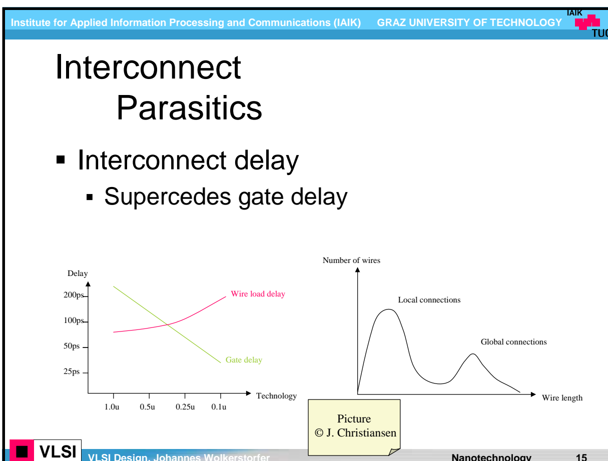
Leakage

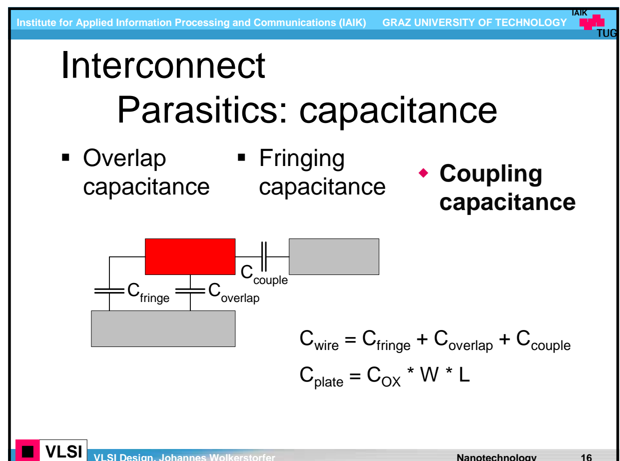
- Static power consumption
  - Sub-threshold currents
    - Exponential growth of currents
      - By lowered threshold voltages
      - By increased temperature
  - Gate oxide leakage
    - Tunneling effects
- Depends on circuit area
  - Memories consume much power

Picture © Prentice Hall 1998









Interconnect Capacitance Typical Values

- 0.25 µm overlap capacitance [aF/µm²]

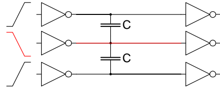
	Sub	Poly	Met1	Met2	Met3	Met4
Sub	113	37	18	13	9	8
Poly		53	16	10	7	6
Met1			35	15	9	7
Met2				39	16	10
Met3					44	16
Met4						39

Interconnect Capacitance Crosstalk

- Less interconnect spacing
  - Capacitance increases
    - Plate capacitor formula: $C = \varepsilon * A / d$
  - Crosstalk
    - Voltage spikes couple to neighboring wires
  - Delay variation: Miller effect

Interconnect Capacitance
Miller effect

- Neighboring signal
  - Influences signal delay
    - Neighboring signals switch in opposite direction
      - Both capacitor terminals switch in opposite direction
      - Effective voltage doubled -> additional charge needed



Interconnect Capacitance
Solutions

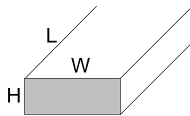
- Low-k dielectrics:
  - Reduced capacitance

[µm]	0.25	0.18	0.13	0.1	0.07	0.05
K	3.3	2.7	2.3	2.0	1.8	1.5

- Copper interconnect
  - Wire thickness can be reduced

Interconnect
Parasitics: Resistance

- $R = \rho * L / (H * W)$
- Sheet resistance
  - R_0
  - $R = R_0 * W / L$
- 0.25 µm sheet resistance
  - N+: 4.9 Ohm / square
  - P+: 3.5 Ohm / square
  - Poly: 4.2 Ohm / square
  - Metal: 0.07 Ohm / square



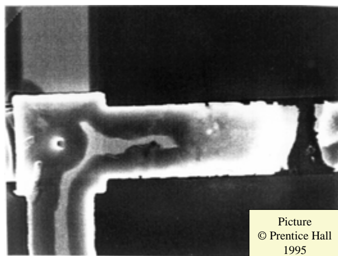
Interconnect
Parasitics: Resistance

- Influence of wiring increases with smaller processes
- Up to 90% of delay at 0.35 µm
- New tools to cope with interconnect
  - „Design for interconnect“ DFI

Estimate interconnect impact early!

Interconnect Resistance
Electro Migration

- Limit average current I_{av}
- Increase wire width
- Peak current
  - Max 10 I_{av}



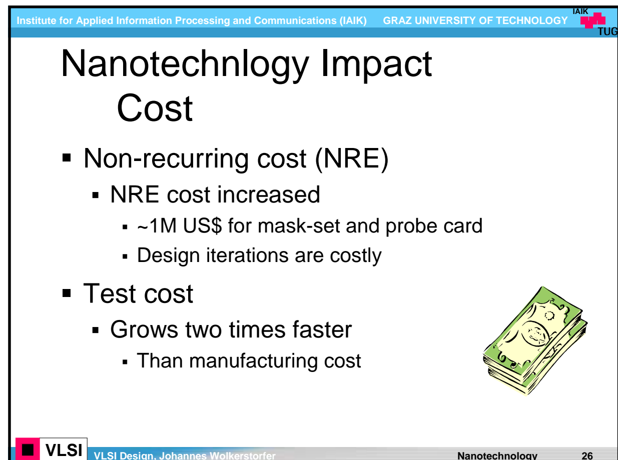
Picture © Prentice Hall 1995

Interconnect Resistance
Solutions

- Classic metal layers
  - Aluminum (2.65e-8 Ω/m)
- DSM material for Met1, Met2: Tungsten
  - Copper would diffuse into diffusion area
- DSM top metal layers (Met3, Met4, …)
  - Copper (1.67e-8 Ω/m)
    - 40% resistance reduction
    - VDD and GND distribution
    - Clock signal distribution
    - Lower sensitivity to electro migration

Nanotechnology Impact Methodology

- Floor-planning
  - Timing driven
- Synthesis
  - Prediction of interconnect influence
    - Wire-load model
- On-chip buses
  - Segmentation
- Parasitic extraction
  - RC-model for wires instead caps only
  - LRC-models for nanotechnologies
- Testability: Built-in self-test (BIST)
  - At speed testing, "cheap" test equipment



Nanotechnology impact Logic Style

- CMOS
  - Good logic style for DSM
  - Withstands
    - Low supply voltage
    - High threshold voltage
- Domino logic
  - Alternative to CMOS
- Pass-gate logic
  - infeasible
- Transmission gate logic
  - less attractive
- Series transistors
  - Very slow
    - Due to reduced VDD
- Circuit technique
  - Similar to high-speed circuits
    - Logic decomposition
    - Pipelining
  - Synchronous clocks
    - difficult

Nanotechnology CMOS Process Example

- 0.13 µm TSMC process (0.08 µm L_{eff})
  - 200k – 300k gates / mm²
  - VDD = 1.00 V, 1.20 V, or 1.50 V
  - Vt = 0.27 V, 0.35 V, 0.58 V
  - Delay = 14 ps, 19 ps, 25 ps
    - IO voltage: 2.5 V or 3.3 V (optional)
    - Multiple Vt (optional)
    - Operation frequency > 1 GHz
  - 8 layer copper / low-k interconnect
  - MPW run: 2.400.- € / mm² (5*5 mm = 61.000 €)
    - For comparison: 1 mm² @ 0.35 µm: 720 €

Conclusion

- DSM process technology
  - Enables multi million transistors circuits
  - Requires additional attention during design
    - Impact of interconnect
    - Testability

Scaling will continue at least 10 years!