Investigation of "A Signed-Digit Architecture for Residue to Binary Transformation", Simulation and Literature survey

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Introduction

There has been interest in Residue Number Systems (RNS) as a basis for computational hardware since the 1950s [16], due to the inherent properties of RNS such as parallelism, modularity and carry-free operations.

Unfortunately, other arithmetic operations like division, comparison and sign detection are hard [4]. For this reason, it is necessary to convert the results of RNS calculations back to a weighted number system such as binary.

Available Methods

- Chinese Remainder Theorem
- Mixed-Radix Conversion
- Core function [5]

Presentation Structure

- Concept overview
- Theorems
- Converters – two-modulus and three-modulus
- Simulation
- Performance Analysis
- Literature Survey
- Conclusions

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Concept overview

- The moduli set is introduced

$$S^k = \left\{2^m - 1, 2^{2^0 m} + 1, 2^{2^1 m} + 1, 2^{2^2 m} + 1, \ldots, 2^{2^k m} + 1\right\}$$

- This moduli set has the useful property that the multiplicative inverses used in the CRT will be powers of 2.
- Modulo operations can be replaced by input bit positioning in hardware and an end-around carry operation.
- The trade-off is that the conjugate moduli that give this benefit result in subtraction operations being required and signed digits are used here.

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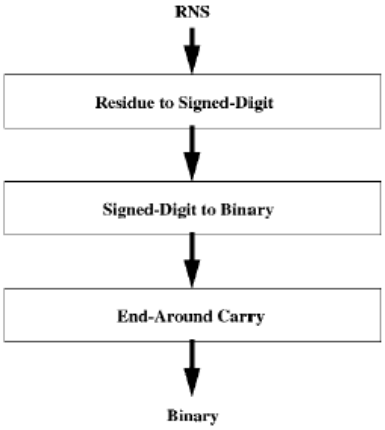
Three-stage R-B conversion



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Theorems

the k+2 members of S^k are relatively prime.

$\gcd(2^{2^j m}+1,\ 2^{2^k m}+1) = 1$, for all k>j.

$\left|N_i^{-1}\right|_{m_i}$ is always a power of two.

- Shown for the first modulus
- Shown for the rest, of the form

$$m_i = 2^{2^{i-2} m} + 1$$

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Notation

Let $\left|X\right|_m$ be "X modulo m"

let $\left|X^{-1}\right|_m$ be the multiplicative inverse of $\left|X\right|_m$

let $M = \prod m_i$

let $N_i = M/m_i$

let gcd(x, y) be the greatest common divisor of x and y.

Theorem: the k+2 members of S^k are relatively prime.

Proof: First it is shown that gcd($2^m - 1$, $2^{2^j m} + 1$) = 1. Since $\left|2^m\right|_{2^m-1} = 1$ (it is one more than the modulus), it is implied that $\left|2^{2^j m}\right|_{2^m-1} = \left|\left(2^m\right)^{2^j}\right|_{2^m-1} = 1$, because each modulus of 1 multiplied together 2^j times will still equal 1. As a result, $\left|2^{2^j m} + 1\right|_{2^m-1} = 2$. If there is a divisor $x \neq 1$ where $\left|2^m - 1\right|_x = \left|2^{2^j m} + 1\right|_x = 0$, then $\left|2\right|_x = 0$, which means that x=2. However, this is a contradiction, since all moduli are odd numbers.

2. It is shown that gcd($2^{2^j m}+1$, $2^{2^k m}+1$) = 1, for all k>j. Since $\left|2^{2^j m}\right|_{2^{2^j m}+1} = \left|-1\right|_{2^{2^j m}+1}$ (it is one less than the modulus), it is implied that $\left|2^{2^k m}\right|_{2^{2^j m}+1}$ = (via exponent algebra) $\left|\left(2^{2^k m}\right)^{2^{k-j}}\right|_{2^{2^j m}+1} = \left|(-1)^{2^{k-j}}\right|_{2^{2^j m}+1}$ (just multiplied 2^{k-j} times); and = 1. As a result, $\left|2^{2^k m}+1\right|_{2^{2^j m}+1}$ = 2, since the inner term is one more than that which had modulus 1. Similarly, if $\left|2^{2^j m}+1\right|_x = \left|2^{2^k m}+1\right|_x = 0$, then $\left|2\right|_x = 0$, which is a contradiction. QED.
Note that, thanks to the conjugate moduli, the range of the moduli set S^k is [0,M), where $M = (2^m-1)(2^{2^0 m}+1)(2^{2^1 m}+1)(2^{2^2 m}+1)\ldots(2^{2^k m}+1) = (2^{2^{k+1} m}-1)$ (equ. 2), since $(2^m-1)(2^{2^0 m}+1) = (2^{2^1 m}-1)$ (i.e., if k=0, we have 1 as a power of two after multiplying the 0-order conjugate modulus).

$\left|N_i^{-1}\right|_{m_i}$ is always a power of two.

For the first modulus, $N_1 = M/m_1$
is equal to: $N_1 = (2^{2^0 m}+1)(2^{2^1 m}+1)(2^{2^2 m}+1)\ldots(2^{2^k m}+1)$ (equ. 4)

Due to the fact that $\left|2^{jm}\right|_{2^m-1} = 1$, each factor of N_1 modulo m_1 is equal to two ($\left|2^{jm}\right|_{2^m-1} = \left|\left(2^m\right)^j\right|_{2^m-1} = \left|(1)^j\right|_{2^m-1}$=1; each term has an additional 1 added). As a result: $\left|N_1\right|_{m_1} = \left|2.2.2...2\right|_{2^m-1} = \left|2^{k+1}\right|_{2^m-1}$ (equ. 5).
Therefore, $\left|N_1^{-1}\right|_{m_1} = 2^{m-(k+1)}$ (equ. 6). This can be verified by writing $\left|N_1 \times \left|N_1^{-1}\right|_{m_1}\right|_{m_1} = \left|2^m\right|_{2^m-1} = 1$, from equ. 5.

For the rest of the moduli of the form $m_i = 2^{2^{i-2}m} + 1$ $2 \le i \le k+2$

$|N_i|_{m_j} = \left|(2^m - 1)(2^{2^0 m} + 1)(2^{2^1 m} + 1)..(2^{2^{i-3} m} + 1)(2^{2^{i-1} m} + 1)..(2^{2^k m} + 1)\right|_{m_j}$ (equ. 7) – (note the $(2^{2^{i-2} m} + 1)$ term was divided out).

If the binomials up to and including the i-3 term are multiplied together,

$|N_i|_{m_j} = \left|(2^{2^{i-2} m} - 1)(2^{2^{i-1} m} + 1)(2^{2^i m} + 1)..(2^{2^k m} + 1)\right|_{m_j}$ (equ. 8)

The first term of this can be reduced to:

$\left|(2^{2^{i-2} m} - 1)\right|_{m_i} = \left|2^{2^{i-2} m}\right|_{m_i} - 1\Big|_{m_i} = |(-1) - 1|_{m_j} = |-2|_{m_i}$, since $m_i = (2^{2^i m} + 1)$. (equ. 9).

The range of the rest of the terms in (8) is $i-1 \le j \le k$ and for the rest of the terms we can write

$\left|2^{2^j m} - 1\right|_{m_i} = \left|\left(2^{2^{j-2} m}\right)^{2^{j-(i-2)}} + 1\right|_{m_i} = \left|(-1)^{2^{j-(i-2)}} + 1\right|_{m_j} = |2|_{m_j}$ (equ. 10)

which is obtained by noticing that j>i-2, given the range under consideration.

Substituting (9) and (10) into (8) gives:

$|N_i|_{m_j} = |(-2)(2)(2)..(2)|_{m_i} = \left|(-2)2^{k-(i-2)}\right|_{m_j}$ given the range of twos is exclusive of i-2 of the first term in (8) (which is -2).

Thus $|N_i|_{m_j} = \left|-2^{k-i+3}\right|_{m_j}$ (equ. 11).

Therefore, for all m_i where $2 \le i \le k+2$, the multiplicative inverses are calculated as $\left|N_i^{-1}\right|_{m_i} = 2^{2^{i-2} m-(k-i+3)}$ (equ. 12).

This can be verified by writing $\left|N_i \times \left|N_i^{-1}\right|_{m_1}\right|_{m_1} = \left|-2^{2^{i-2} m}\right|_{m_j}$ where $m_i = 2^{2^{i-2} m} + 1$. For example, if i=2 at the beginning of this range for the rest of the moduli, $\left|-2^m\right|_{2^m+1}$, the modulus of this is (-8) mod 9 = 1, since -8 = 9(-1) + 1, where -1 is the quotient and +1 is the remainder. See Koren [4], pg 260 section 11.1.

Equations (6) and (12) show that the multiplicative inverses for this moduli set are always powers of two. This allows simplification in the CRT equation where multiplications can be replaced by simple shift-left operations.

Also, if i=2 in (12), $\left|N_2^{-1}\right|_{m_2} = 2^{m-(k-2+3)} = 2^{m-(k+1)} = \left|N_1^{-1}\right|_{m_1}$ from equ. (6) (this is equ. 13).

Note that the result of equ (2) shows that the final modulo-M operation can be replaced by an end-around carry operation, because bits in the next group of $2^{k+1}m$ bits are units in the modulus and the dividend can be partitioned by $2^{k+1}m$ bits when the modulus is $(2^{2^{k+1}m}-1)$; see Koren [4] pg 271 example 11.11.

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Two-moduli converter

When k=0, we have the S^0 moduli set = $\{2^m-1, 2^m+1\}$. This results in $M=2^{2m}-1$ and a number range of $[0, 2^{2m}-1)$, ie $[0, 2^{2m}-2]$.

The CRT in (3) reduces to:

$$\left|X\right|_M = \left|N_1\left|N_1^{-1}\right|_{m_1} x_1 + N_2\left|N_2^{-1}\right|_{m_2} x_2\right|_M \quad \text{(equ. 14)}$$

Substituting k=0 in (13), the multiplicative inverses $\left|N_1^{-1}\right|_{m_1}$ and $\left|N_2^{-1}\right|_{m_2}$ are both 2^{m-1}.

Substituting in (14), we have $\left|X\right|_M = \left|(2^m+1)2^{m-1}x_1 + (2^m-1)2^{m-1}x_2\right|_{2^{2m}-1}$ (equ. 15)

which can be rearranged into: $\left|X\right|_M = \left|2^{2m-1}(x_1+x_2) + 2^{m-1}(x_1-x_2)\right|_{2^{2m}-1}$ (equ 16).

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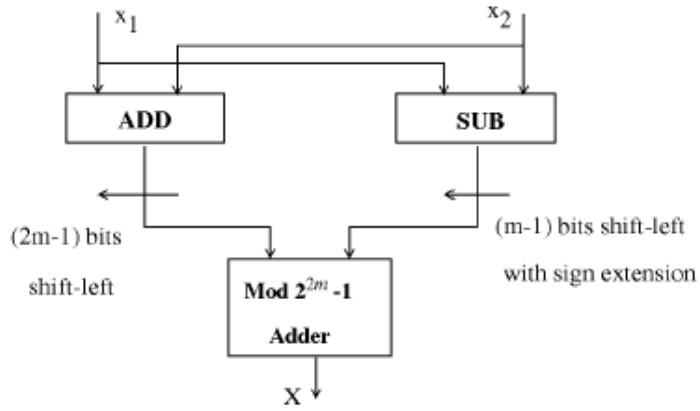
Hardware realization concept



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If m = 3, the S^0 moduli set = $\{2^3-1, 2^3+1\}$ and $M=2^6-1 = 63$ and a number range of $[0,63) = [0,62]$ results.
The CRT becomes

$$|X|_M = \left|2^5(x_1+x_2)+2^2(x_1-x_2)\right|_{2^6-1} \text{ (equ 17).}$$

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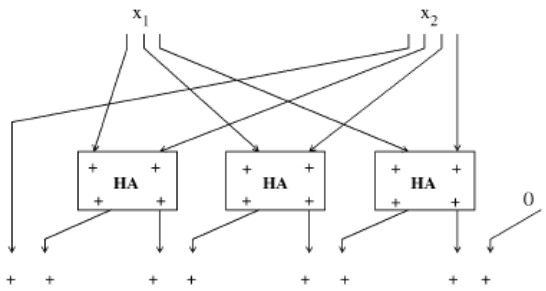
Developing the HW realization



The Add block

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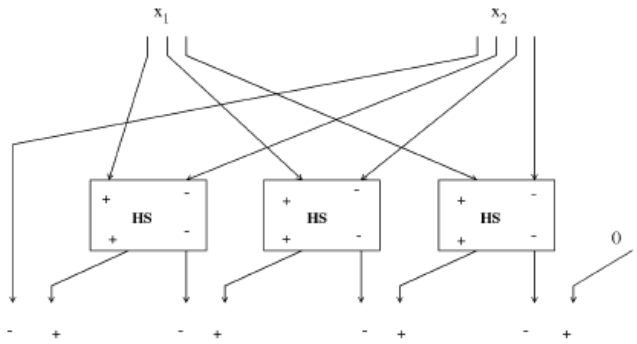

The Subtract block

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If $x_1 = a_2a_1a_0$ and $x_2 = b_3b_2b_1b_0$ the input bits can be arranged to have already their shifted-left positions of 5 bits shifted left for the sum and 2 bits shifted left for the difference as shown in Fig. 5. Notice the partitioning to the left of the sixth bit, i.e., between bits 5 and 6. The nature of the $2^6 - 1$ modulo process will result in those bits being moved around to the lowest-order position.

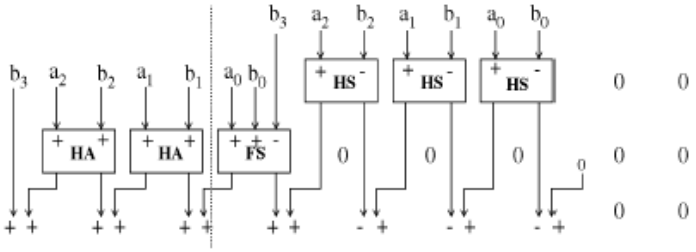

Fig 3.5. Results of the shift-left operation

Two-mod. HW - final

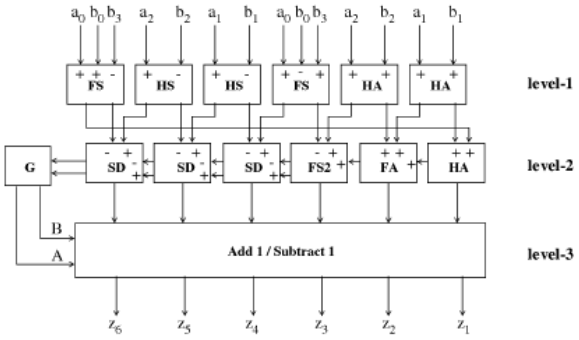

Fig 3.6. The two-moduli converter architecture.

What about without SDs?

•Attempting an implementation without signed digits might not result in any simplification.
•I have attempted one, using only Full and Half Adders and Subtractors.
•Subtractors take a positive difference and generate a negative borrow, which has to be subtracted from the next stage.

•HS: D = x'y + xy', B = x'y [Mano, Digital Design [35]]
•FS: D = x'y'z + x'yz' + xyz' + xyz, B = x'y + x'z + yz = x'(y + z) + yz, x is the minuend, y is the subtrahend, z is the Borrow in, D is the difference, and B is the borrow out.

•Note that the equations for the difference are the same as those for the sum in an adder, and that the equation for the borrow in the FS is very similar to the equation for the carry in a FA; the only difference being the minuend is complemented.

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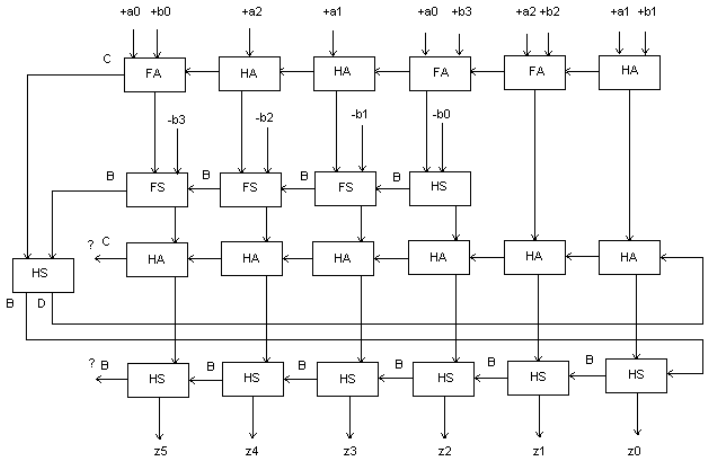
Attempt without SDs



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Three-Moduli Converter

When k=1, we have the S^1 moduli set = $\{2^m-1, 2^m+1, 2^{2m}+1\}$. This results in $M=2^{4m}-1$ and a number range of $[0, 2^{4m}-1)$, ie $[0, 2^{4m}-2]$.
The CRT in (3) reduces to:

$$|X|_M = \left| N_1 |N_1^{-1}|_{m_1} x_1 + N_2 |N_2^{-1}|_{m_2} x_2 + N_3 |N_3^{-1}|_{m_3} x_3 \right|_M \quad \text{(equ. 18)}$$

Substituting k=1 in (13), the multiplicative inverses $|N_1^{-1}|_{m_1}$ and $|N_2^{-1}|_{m_2}$ are both 2^{m-2}.

Substituting k=1 and i=3 in (12), $|N_3^{-1}|_{m_3} = 2^{2m-1}$.

Substituting in (18), we have $|X|_M =$

$$\left|(2^m+1)(2^{2m}+1)2^{m-2}x_1 + (2^m-1)(2^{2m}+1)2^{m-2}x_2 + (2^m-1)(2^m+1)2^{2m-1}x_3\right|_{2^{4m}-1} =$$

$$\left|(2^m+1)(2^{2m}+1)2^{m-2}x_1 + (2^m-1)(2^{2m}+1)2^{m-2}x_2 + (2^{2m}-1)2^{2m-1}x_3\right|_{2^{4m}-1} \quad \text{(equ. 19)}$$

which can be rearranged into: $|X|_M =$

$$\left|(2^{4m-1})x_3 + (2^{4m-2})(x_1+x_2) + (2^{3m-2})(x_1-x_2) - 2^{2m-1}x_3 + (2^{2m-2})(x_1+x_2) + (2^{m-2})(x_1-x_2)\right|_{2^{4m}-1}$$

(equ 20).

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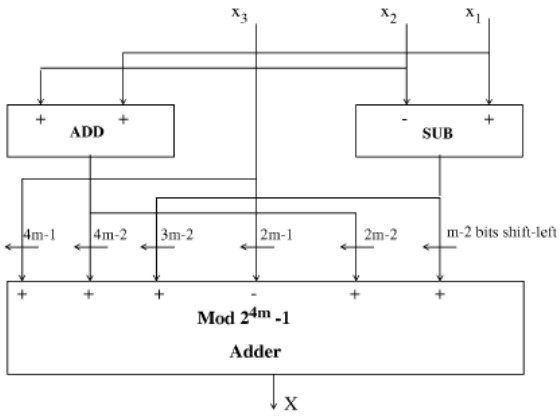
3-mod. HW realization concept



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If x1 = a2a1a0, x2 = b3b2b1b0, and x3 = c6c5c4c3c2c1c0, when m=3, Fig. 4.9 shows the shift-left concept.

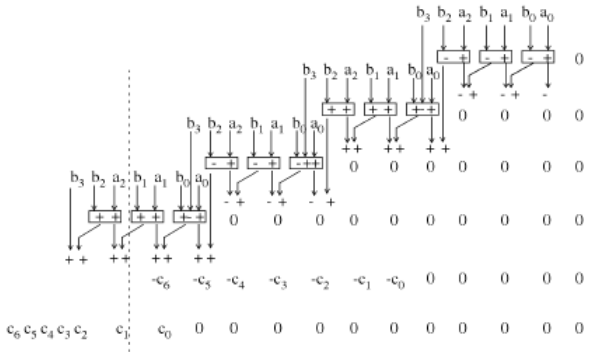

Fig. 4.9. Bits positioned already in their shifted-left positions

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A four-operand adder/subtractor is used to group the pre-shifted positions of the operand bits as shown in Fig. 4.10.

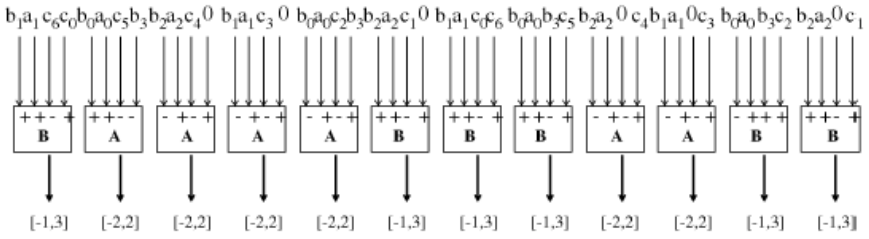

Fig. 4.10. Four-operand addition/subtraction

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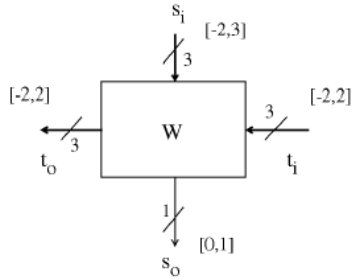
CPA level 2 of 3-mod converter

$s_i + t_i = 2\,t_o + s_o$



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Simulation

- The adder, subtractor, SD-to-binary and level-3 multiplexing blocks were simulated as C++ objects in Microsoft Visual C++ version 6.0.
- The truth tables and/or equations are given, as applicable

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Two-mod. simulation
SD HA Truth table

In1	In2	s	c
0	0	0	0
1	0	1	0
-1	0	-1	0
0	1	1	0
-1	1	0	0
1	1	0	1
0	-1	-1	0
1	-1	0	0
-1	-1	0	-1

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SD FA Truth table

In1	In2	c_{in}	s	c_{out}
0	0	0	0	0
1	0	0	1	0
0	1	0	1	0
1	1	0	0	1
0	0	1	1	0
1	0	1	0	1
0	1	1	0	1
1	1	1	1	1
0	0	-1	-1	0
1	0	-1	0	0
0	1	-1	0	0
1	1	-1	1	0

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SD HS Truth table

Subtrahend	Subtractor	Diff	c
0	0	0	0
1	0	1	0
0	1	-1	0
1	1	0	0

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SD FS Truth table

Subtrahend	Subtractor	c_{in}	Diff	c_{out}
0	0	0	0	0
1	0	0	1	0
0	1	0	-1	0
1	1	0	0	0
0	0	1	1	0
1	0	1	0	1
0	1	1	0	0
1	1	1	1	0

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SD FS2 Truth table

Subtrahend	"Subtractor"*	c_{in}	Diff	$-c_{out}$	$+c_{out}$
0	0	0	0	0	0
1	0	0	1	0	0
0	1	0	1	0	0
1	1	0	0	0	1
0	-1	0	1	1	0
1	-1	0	0	0	0
0	0	1	1	0	0
1	0	1	0	0	1
0	1	1	0	0	1
1	1	1	1	0	1
0	-1	1	0	0	0
1	-1	1	1	0	0
0	0	-1	1	1	0
1	0	-1	0	0	0
0	1	-1	0	0	0
1	1	-1	1	0	0
0	-1	-1	0	1	0
1	-1	-1	1	1	0

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SD-B and Carry-Multiplex blocks

- The SD–binary converter is used in two-mod. simulation level 2. The "–in" input has to be able to accept signed digits. It adds them in order to subtract them if they are negative. It adds the rest of the inputs, subtracting only the negative carry-in, which is defined to be positive. The truth table would have 24 rows (3 choices for "-in", 2 for "+in", 2 for "-cin" and 2 for "+cin") and is straightforward, and so is not given here.
- The GA block detects which if any of -cout or +cout results as the end-around carry and signals level 3 whether to add one, subtract one, or do nothing.

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Simulation of level 1 initial concept (see Fig 3.5)

Using the residues (5,7), which code for 61 in the (2^3-1, 2^3+1) (7, 9) moduli set, the initial concept of level 1 is demonstrated

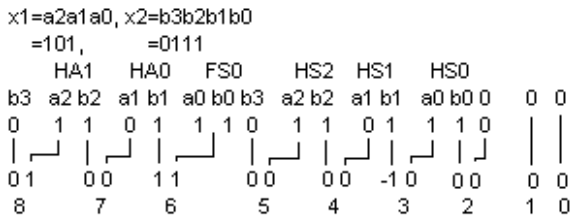

Fig. 5.1. Initial shift-left concept. ([1], Fig. 5)

It can easily be seen that this output equals 256 + 2x64 -8 = 376; $|376|_{63} = 61$

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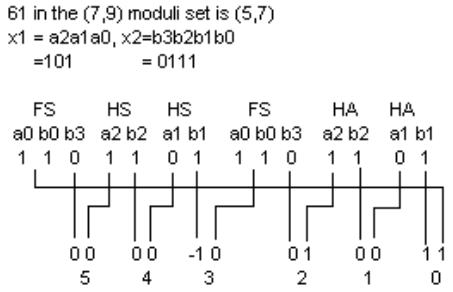
Level 1 simulation

Note that the inputs are preshifted, leaving only a possible end-around carry to be applied to level 2.



It can be seen that when the number's carries are added and the results are converted from signed digits, 1,1,1,1,1,0 with a -1 end-around carry will result, which will be 32 + 16 + 8 + 4 + 2 – 1 = 61

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Two-mod. entire simulation

- This simulation consists of feeding the output from level 1 into the SD, FS2 and adder blocks explained above.
- Level 2 subtracts the negative part of the number from the positive part, making the inputs to the FS2 and SD blocks positive in sense so that negative digits will naturally be subtracted.

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Three-moduli simulation

- The A and B four-input adder/subtractors are very simple; complexity lies in the bit-positioning of the inputs in order to achieve the required moduli.
- A simply subtracts the bit data on the subtracting inputs from that on the adding inputs, and B differs only in having only one subtracting input.
- CPA: W: $s_i + t_i = 2t_o + s_o$

  $s_o = \text{abs}(s_i+t_i) \bmod 2$, and $t_o = (s_i + t_i - s_o)/2$

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Simulation of removal of CPA

- The carry propagates can be eliminated, or at least reduced, by parallel calculation of the level 1 output data from blocks A and B, eliminating the block W, which is a type of CPA.
- A conditional-sum simulation is presented.
- Has complexities of its own, due to 5 different carry possibilities in the range [-2,2]
- the s_i plus the possible carries can be easily generated from $s_i + 2$ to $s_i - 2$, the potential s_o are the absolute value of those modulo 2 and the potential t_o are those minus the potential s_o, the result divided by 2.

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Performance Analysis

Two-Moduli converter

Block	Delay
HA	Δ
HS	Δ
FA	2Δ
FS	2Δ
FS2	2Δ
SD	3Δ
G	Δ

Table 6.1 Gate delays

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Two-mod. converter performance

- Note that the SD block has to perform two half-additions in parallel, and then a full-subtraction, yielding three gate-delays.
- Level 1 takes 2?, level 2 takes ?(G), 3m?(SDs), 2?(FS2), (m-2)2? (FAs) plus 1? for the one HA and then 2m2? (max) for the final end-around carry FAs of level 3
- This totals (9m+2)?.
- For the moduli set of {5, 17}, which provides the dynamic range of [0, 85), the FA-based RNS to binary converter reported by Stouraitis [2] has a delay of 51?. Using $m = 4$, the two-moduli set of $\{2^4 - 1, 2^4 + 1\}$ provides the dynamic range of [0, 255). Referring to Table 6.2, for $m = 4$, the two-moduli converter here imposes an operational delay of 38?, giving less delay for a greater dynamic range.

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Three-mod. converter performance

- Referring to Fig. 4.10, the blocks A and B have the same complexity and delay as of SD. The block W of Fig. 4.11 is a three-bit redundant adder introducing a delay of 5?. Here, the block G has a delay of 2?. The delays of the three conversion levels are:
- $D_1 = D_A = D_B = 3?$
- $D_2 = D_G + 4mD_W = 20m+2?$
- $D_3 + 4mD_{FA} = 8m?$

Resulting in a total delay of:

- $D = D_1+D_2+D_3 = (28m+5)?$

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Literature survey

- From about the time period of P. and Y. [1] (~1997)

Name (et. al.)	Reference	Year	Moduli set	Delay claimed
Stouraitis	[2]	1992	$\{m_1, m_2) = (5,17)$	51?
Gallaher	[3]	1997	$(2^k\text{-}1, 2^k, 2^k+1)$	13 FAs for k=32
Hiasat	[6]	1998	$(2^k, 2^k\text{-}1, 2^{k-1}\text{-}1)$	-of 1 (2k-1)-bit bin. adder
Skavantos	[7]	1998	$m_1 = 2^i$, ? $_{rest} = 2^a - 1$	5FA + 1 mod $(2^{4n}\text{-}1)$ CPA
Yuke Wang	[9]	1998	$(2^n\text{-}1, 2^n, 2^n+1)$	$t_{FA} + t_{inv} + 2t_{CPA2n}$
Yuke Wang	[12]	2002	$(2^n\text{-}1, 2^n, 2^n + 1)$	$t_{inv} + t_{MUX} + t_{FA} + 2t_{CPA(2n)}$
Cardarilli	[13]	1998	$(n\text{-}2^k\ n+2^k)$	Not reported
Wei Wang	[19]	1999	Same as Y&P [1]	(8m+6)?
Bhardwaj	[20]	1999	$(2^n\text{-}1, 2^n, 2^n+1, 2^{n+1}+1)$	10n+13 FA
Wei Wang	[21]	1999	$(2^k, 2^k\text{-}1, 2^{k-1}\text{-}1)$	$(3k+2)t_{FA}$
Wei Wang	[22],[23]	2000 -2002	$(2^k\ 2^k - 1, 2^{k-1} - 1)$	Critical path: $(3k + 2)\ t_{FA}$

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Name (et. al.)	Reference	Year	Moduli set	Delay claimed
Conway	[24]	1999	$(2^n\text{-}1, 2^n, 2^n+1)$	$t_{OR} + t_{FA} + t_{CPA(n)} + t_{ANDOR} + 2t_{MUX}$
Cao	[31]	2003	$(2^n\text{–}1, 2^n, 2^n+1, 2^{n+1}\text{-}1)$	HS: $(5n + l + 5)t_{FA}$ CE: $(11n + l + 5)t_{FA}$
Cao	[32]	2003	$(2^n\text{–}1, 2^n, 2^n+1, 2^{2n}\text{–}1)$	HS: $2t_{MUX} + t_{INV} + 2t_{NAND} + (2n+3)*t_{FA}$ CE: $t_{MUX} + t_{INV} + 2t_{NAND} + (8n+3)*t_{FA}$
Cao	[33]	2004	$(2^n\text{–}1, 2^n, 2^n+1, 2^{n+1}\text{-}1, 2^{n-1}\text{–}1)$	20-40ns for 20-150 bit ranges.
Lindstrom	[34]	2003	$(2^n - 1, 2^n, 2^n + 1)$	16 bits: 3.04 32 bits: 4.63 64 bits: 6.93ns

Literature survey pg. 2 of 2

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Conclusions

- The moduli set

$$S^k = \{2^m - 1,\ 2^{2^0 m} + 1,\ 2^{2^1 m} + 1\ 2^{2^2 m} + 1,\ \ldots,\ 2^{2^k m} + 1\}$$

was introduced.

- For this type of moduli, it was shown that the multiplicative inverses are powers of two.
- Therefore all the modulus operations can be replaced, not only by shift-left operations, but by strategic bit positioning, and only a final end-around carry.
- Residue to binary converter architectures based on the CRT, with respect to S^0 and S^1 (two and three) moduli sets, were developed.
- The conversion from R-B was performed in three stages, with SDs appearing to be very helpful in reducing hardware complexity.
- Simulation of both two and three-mod. converters was done, which establishes correctness of concept.
- Simulation of parallel computation of level 3 in the three-mod. converter was done, showing how the final W (CPA) blocks might be eliminated.
- An overview of the literature was presented, showing that the delays of these converters are O(log(n)) and that it is very difficult to make improvements.

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Thank you!

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